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Sulfurization of co-evaporated Cu(In,Ga)Se₂ as a post deposition treatment

J. K. Larsen, J. Keller, O. Lundberg, T. Jarmar, L. Riekehr, J.J.S. Scragg, and C. Platzer-Björkman

Abstract— It is investigated if the performance of Cu(In,Ga)Se₂ (CIGSe) solar cells produced by co-evaporation can be improved by surface sulfurization in a post deposition treatment. The expected benefit would be formation of a sulfur/selenium gradient resulting in reduced interface recombination and increased open circuit voltage. In the conditions used here it was, however, found that the reaction of the CIGSe layer in sulfur environment results in formation of a CuInS₂ (CIS) surface phase containing no or very little selenium and gallium. At the same time, a significant pile up of gallium was observed at the CIGSe/CIS boundary. This surface structure was formed for a wide range of annealing conditions investigated in this work. Increasing the temperature or extending the time of the dwell stage had a similar effect on the material. The gallium enrichment and CIS surface layer widens the surface band gap and therefore increases the open circuit voltage. At the same time the fill factor is reduced, since the interface layer acts as an electron barrier. Due to the balance of these effects the conversion efficiency could not be improved.

Index Terms— Cu(In,Ga)Se₂, surface treatment, post deposition treatment, alloying, thin film solar cells

I. INTRODUCTION

The high efficiencies of thin film solar cells have been achieved to a large extent due to the ability to introduce band gap gradients in the absorber. In state of the art Cu(In,Ga)Se₂ (CIGSe) solar cells the band gap gradient is obtained by establishment of a compositional gradient of Ga/In or S/Se. A Ga/In gradient is often implemented in co-evaporated CIGSe, while the use of a S/Se gradient is mainly used when Cu(In,Ga)(S,Se)₂ (CIGSSe) is produced by a two-step process. In the two-step process metal precursors are typically annealed in H₂Se followed by H₂S to create a sulfur rich surface [1, 2]. Solar Frontier has demonstrated a record conversion efficiency of 22.3% using this two-step process commonly abbreviated SAS (sulfurization after selenization) [3]. The benefit of the sulfur incorporation in the surface of

CIGSe is a band gap widening that reduces interface recombination. In this work we investigate if it is possible to obtain a benefit from a sulfur gradient in CIGSe absorbers deposited by co-evaporation as well. The aim is to develop a post deposition sulfurization treatment for co-evaporated CIGSe that yields an improved device performance. In order to avoid the toxic hydride gasses, the annealing is performed with elemental sulfur. Co-evaporated CIGS from an in-line process is sulfurized in a furnace to investigate the limitations and potential advantages. This additional step could be incorporated in an in-line process like the now commonly applied KF post deposition treatment.

In literature attempts to sulfurize the surface of CIGSe have shown both encouraging results as well as potential challenges. It has been demonstrated that sulfurization of coevaporated CIGSe in an H₂S atmosphere can result in formation of a S/Se graded CIGSSe and improved device performance from 15.6 to 17 % as a consequence [4, 5]. It has also been shown that an improvement from 14.5% to 16% efficiency can be obtained by annealing with elemental sulfur [6]. Among the explanations for the benefit of surface sulfurization are band gap widening of the surface [5] and passivation of deep defect states [6-8]. Annealing CIGSe in the presence of the metalorganic sulfur precursor ditertiarybutylsulfid has also been shown to result in formation of a S/Se surface gradient in coevaporated CIGSe [9]. In another study In₂S₃ was evaporated onto CIGSe at 580 °C at the end of a coevaporation process resulting in formation of a CIGSSe surface layer [6]. In both these studies an improvement of the device efficiency resulted from the surface sulfurization. Some challenges have been mentioned as well. It was for example noticed that sulfurization of coevaporated CIGSe in H₂S resulted in a non-uniform surface layer with presence of many different phases including CIGSe, CIGS and a Cu-Au ordered phase [10]. Device improvements have been reported for S/Se graded CIGSSe with low total sulfur content, but fill factor (FF) degradation has been observed for higher than 4% total sulfur content [11]. Further, the incorporation of sulfur in the CIGSe surface is strongly dependent on the composition of the absorber material. Sulfur inclusion is favoured in Cu-rich CIGSe compared to Cu-poor CIGSe [12]. The sulfur incorporation also depends on the presence of gallium in the sample. It has been found that CIGSe annealed in H₂S resulted in a graded CIGSSe alloy, while annealing of CIGSe under the same conditions resulted in phase separation into a CIGSe phase and a CIS surface layer [13].

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II. EXPERIMENTAL

Uniform CIGSe absorber material was co-evaporated on an about 1m^2 Mo-coated glass substrate at Solibro Research AB. After CIGSe deposition the layer was coated with CdS by chemical bath deposition to protect the absorber from degradation during storage. The substrate was cut into small $2.5 \times 2.5\text{cm}^2$ pieces for the experiments performed here. With this approach a large amount of uniform material is available to investigate the effect of subsequent annealing treatments. Immediately before the sulfurization experiments were performed the CdS capping layer was removed by etching in 2M HCl for one minute. The sulfurization annealing treatments were performed in a custom built furnace consisting of a 3 litre graphite reactor and a separately heated source used to dose chalcogen into the reactor. In this system the annealing is performed in a 50 mbar argon atmosphere and a controlled amount of chalcogen can be introduced at any stage of the annealing. For the experiments performed in this work the reactor is preheated to a set temperature before the sample sitting in a graphite carrier is introduced. Immediately after sample introduction 1g of sulfur is dosed into the preheated source at $550\text{ }^\circ\text{C}$ and brought into the reactor with a flow of argon carrier gas in the course of 1 minute. The reactor is then sealed for an annealing dwell step for a set time. After the dwell stage the heater in the reactor is turned off allowing the sample to cool naturally for 30 minutes in the sulfur atmosphere before the sample is taken out. Two series of experiments are presented. In a temperature series, the temperature was varied in the range $480 - 560\text{ }^\circ\text{C}$ while the dwell time was kept at 10min. In a time series the dwell time was varied between 1 second and 20 minutes and the temperature kept at $500\text{ }^\circ\text{C}$. It should be noted that the temperature is measured with a thermocouple a few centimetres from the sample. The reported temperature is therefore an estimated sample temperature. The sulfurized CIGSe samples were coated with about 60nm CdS by chemical bath deposition. Reference devices were prepared by deposition of CdS after a few minutes air exposure following CdS cap removal. To complete the devices an i-ZnO/ZnO:Al bilayer was deposited by sputtering. References were found to be very reproducible with standard variation of device parameters of 5 %, and an efficiency of 16%.

Raman measurements were performed with back scattering configuration in a Renishaw inVia system using a 532 nm laser. Grazing incidence x-ray diffraction (GIXRD) measurements were performed at 1 degree of incidence in Siemens D5000 system using a Cu K alpha source. Devices were studied with external quantum efficiency (EQE) measurements performed in a home-built setup. The illuminated current-voltage (JV) characteristics were measured with a tungsten halogen lamp as a light source at a cell temperature of $25\text{ }^\circ\text{C}$. The JV measurements were calibrated with short circuit (J_{SC}) values calculated from the EQE and AM1.5G standard spectrum.

Focused ion beam (FIB) cross-sectional lamellas for scanning transmission electron microscopy (STEM) analyses

were prepared with a FEI Strata DB235 and attached to a Mo lift out grid. The final polishing steps for the lamella included sputtering sequentially from both sides with a 5 kV Ga beam of 50 pA and the aid of XeF_2 , followed by sputtering with a 30 pA Ga beam at 5 kV for 30 s. The lamella was considered thin enough for STEM analyses after it showed transparency in the FIB scanning electron microscope (SEM) with a 3 kV electron beam.

STEM imaging and STEM energy dispersive X-ray spectroscopy (EDS) analyses were conducted on a C_s probe corrected FEI Titan Themis equipped with the FEI X-FEG operated at 200 kV accelerating voltage and the SuperX system for EDS measurements. The acquired spectra were deconvoluted and quantified with the ESPRIT software provided by Bruker.

III. RESULTS AND DISCUSSION

A. Materials characterization

Fig. 1 (a) shows Raman spectra measured on absorbers after sulfurization with different dwell times. Two peaks at 178 cm^{-1} and 290 cm^{-1} dominate the spectrum. These peaks are both ascribed to A1 modes, which result from vibration of the anions while the cations remain at rest. The peak at 178 cm^{-1} is associated with vibration of Se atoms in CIGSe[14, 15]. This mode is observed at 174 cm^{-1} in CuInSe_2 and 184 cm^{-1} in CuGaSe_2 [15], and shifts in an approximately linear fashion in $\text{CuIn}_y\text{Ga}_{y-1}\text{Se}_2$ alloys with the A1(Se-Se) peak position following $174 + 12.9y$ [14]. In Ga-free alloys with sulfur, $\text{CuIn}(\text{S}_x\text{Se}_{x-1})_2$, it is observed that the A1(Se-Se) peak shifts to

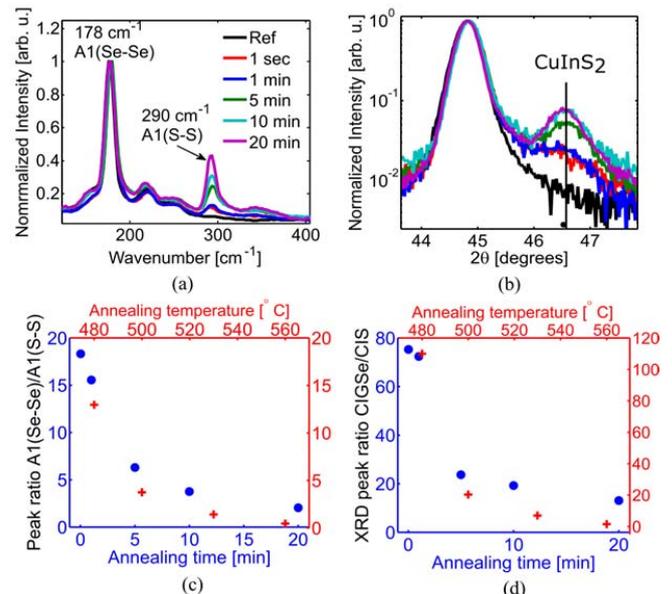


Fig. 1 (a) Raman spectra of CIGSe annealed in a sulfur containing atmosphere at $500\text{ }^\circ\text{C}$ for increasing durations. (b) GIXRD measurement performed at 1 degree of incidence of CIGSe of the same samples (same color code as in (a)). (c) Ratio of the Raman peaks A1(Se-Se) / A1(S-S) for samples annealed at different times (blue axes) and temperature (red axes). (d) Ratio of the XRD reflections of CIGSe and CIS reflections of the same samples.

higher frequencies and reduces in intensity with increasing x [16, 17]. At the same time, the sulfur related A1(S-S) mode observed in pure sulfide CIS at 290 cm^{-1} increases in intensity relative to the A1(Se-Se) mode. The ratio of the A1(S-S) and A1(Se-Se) modes correlates with the of the relative S/Se content in the CISSe material [17]. It is observed that the 290 cm^{-1} peak does not shift when alloying with different S/Se ratios, but this peak vanishes for low values of x [16]. It should be kept in mind that this is the behaviour seen in homogeneously mixed $\text{CuIn}(\text{S},\text{Se})_2$ crystals. Once a gradient in the S/Se content is present within the volume probed in the measurement, one would expect to observe a broadening of the A1(Se-Se) peak, but not the A1(S-S) [16, 18]. In Fig.1 it is seen that the A1(Se-Se) mode at 178 cm^{-1} remains unaltered in shape while the A1(S-S) mode at 290 cm^{-1} increases in intensity with annealing time. Since no broadening or shift is observed for the A1(Se-Se) peak, it is inferred that no S/Se alloy formation occurs. The increase in the A1(S-S) intensity instead relates to incorporation of sulfur in a new, Se-free phase forming at the surface. Since the A1(Se-Se) mode appears even for the 20 min sulfurization, this implies either that the new surface layer has incomplete surface coverage, or that it is thinner than the probing depth of the laser, which is about 100 nm [19].

The nature of the phase formed at the CIGSe surface is revealed by GIXRD studies. GIXRD measurements of the samples from the annealing time series are shown in Fig. 1 (b). A reflection at 44.8° is seen in the reference before sulfurization. This corresponds to the (220/204) reflection of CIGSe with about 30% Ga as expected from the starting material. When annealing the material in sulfur, a peak at 46.5° appears. This peak is ascribed to the (220/204) reflection of the Ga- and Se-free compound CuInS_2 (CIS) (JCPDS No. 085-1575). If an S/Se gradient had formed due to incorporation of sulfur in the surface, one would expect the CIGSe peak to asymmetrically widen towards higher angles. Instead, it is observed that the CIS peak grows in intensity, which demonstrates that the sulfur is not incorporated into the CIGSe lattice to form a graded S/Se alloy in the surface region. The result instead indicates the formation of a separate CIS phase with small or no Ga and Se content on the surface. This observation is in agreement with the result of the Raman measurements.

In order to quantify the thickness of the CIS surface layer the ratio of the S and Se-related Raman modes was calculated. After background correction, the A1(S-S) peak intensity is determined by integration over the range $270 - 340\text{ cm}^{-1}$, while the A1(Se-Se) peak intensity is measured by integration over the range $160 - 200\text{ cm}^{-1}$. The ratio of these integrals A1(Se-Se) / A1(S-S) yields a measure of thickness of the CIS surface layer. A similar quantification can be done using the GIXRD measurement by integration over the range of the CIGSe peak

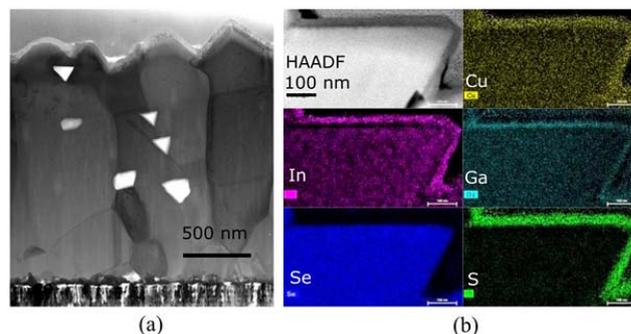


Fig. 2. (a) STEM micrograph of CIGS annealed in sulfur vapour at $500\text{ }^\circ\text{C}$ for 20 minutes. (b) Magnification of the surface region with corresponding elemental maps extracted from STEM EDS measurements.

($44 - 45.5^\circ$) and the range of the CIS peak ($45.9 - 47.5^\circ$) and calculation of the ratio of the two peaks. It was found that the Se/S ratios determined with these two approaches yield the same trends as shown in Fig. 1 (c,d) for the annealing time and temperature series. When increasing the temperature or time we do not create an S/Se gradient, but instead a thicker CIS surface layer is formed in both series. This results in a decrease of the A1(Se-Se) mode relative to the A1(S-S) mode. From the XRD measurements, the formation of the CIS layer is observed as a decrease of the (220/204) CIGSe peak relative to the (220/204) CIS peak.

The surface region of the CIGSe material after sulfurization was studied with STEM in order to verify findings from XRD and Raman measurements. Fig. 2 (a) shows a STEM bright field micrograph of a cross-section of a CIGSe sample after sulfurization for 20 minutes at $500\text{ }^\circ\text{C}$. The entire surface appears to be uniformly covered with a surface reaction layer. Fig. 2 (b) shows a STEM micrograph of the surface region with corresponding STEM EDS maps. A thin surface reaction layer with a darker contrast and a thickness of 35 nm is clearly visible in the high angle annular dark field (HAADF) image. For samples annealed for shorter duration at $500\text{ }^\circ\text{C}$ a thinner reaction layer covering the grain surfaces was observed (not shown here). In case of a 1s dwell time the thickness of the surface layer was estimated to 6 nm , while 21 nm was seen after 5 minutes of annealing. STEM EDS mapping reveals that the surface layer is enriched in Cu and In, while the Ga signal is strongly reduced. At the same time the surface layer contains only S while being depleted from Se, in agreement with the interpretation of the surface layer phase being pure CIS with little or no Se and Ga. Interestingly it is seen that the Ga displaced when forming the CIS surface layer accumulates at the phase boundary leading to formation of a Ga rich interlayer at the CIGSe/CIS interface. This effect was also observed in samples annealed at higher temperature (data not shown).

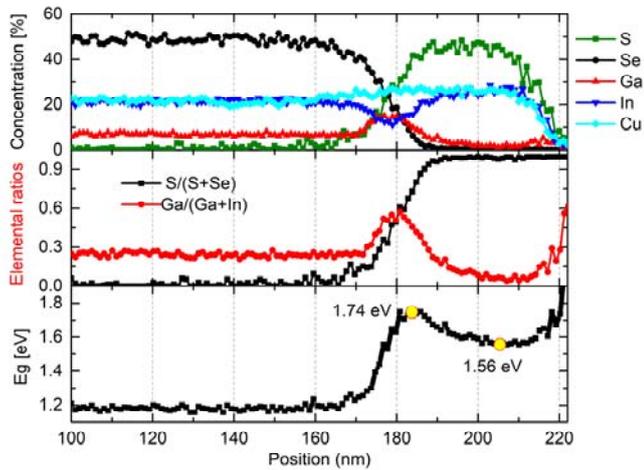


Fig. 3. STEM EDS linescan of the elemental composition in the near surface region of CIGSe after annealing in sulfur for 20 min at 500 °C. The surface of the grain is on the right.

A STEM EDS line scan is performed in order to extract the local chemical composition in the surface region as shown in Fig. 3. The aim of this measurement is to aid understanding of the local band gap variation. Based on the line scan the elemental ratios $[S]/([S]+[Se])$ and $[Ga]/([In]+[Ga])$ are therefore calculated. Since the lamella has a thickness of about 80 nm, a broadening can be expected in the elemental profiles due to the beam interaction volume. From the result it is clear that sulfur does not diffuse into the CIGSe layer. Instead a 37nm thick CIS layer with close to 25 % Cu content is formed. An about 10 nm thick interface layer enriched in Ga between the CIGSe and the CIS is clearly visible. In this interface layer the $[Ga]/([In]+[Ga])$ increases to 0.6, which is expected to increase the band gap. The band gap is calculated from the elemental composition based on the results of Bär et al. [20]. The result shows that a significant widening with up to 0.54 eV in the Ga enriched interfacial layer. The top surface CIS layer is expected to have a band gap widening of 0.36 eV compared to the CIGSe bulk. The increase in band gap has a strong effect on the device behaviour as discussed in section III-C.

B. Mechanism and driving force for surface layer segregation

The intention in these experiments was that S would replace Se near the CIGS surface, creating a smooth S-Se gradient. For this to occur, S atoms from the gas phase would have to diffuse into the CIGS lattice and replace Se atoms, with the latter diffusing out to the surface and evaporating. Clearly, this simple diffusion/replacement mechanism did not occur. One problem with the approach might be the different diffusion rates of cations versus anions in the CIGS lattice. Diffusion in the solid state is strongly enhanced by defects such as vacancies [21], and in Cu-poor CIGS, these are abundant in the cation sub-lattice (a high concentration of Cu vacancies) but negligible in the anion sub-lattice [22]. Thus, given a chemical driving force for diffusion, the cations could respond more easily than the anions. Formation of the observed $CuInS_2$

layer may therefore be due to out-diffusion of Cu and In, via Cu vacancies, to meet S adsorbed at the sample surface. By this mechanism, nucleation and growth of $CuInS_2$ occurs on the CIGS surface, forming a distinct layer of new material instead of a smooth concentration gradient within intact CIGS grains. Further reasons for the failure to form a mixed S-Se compound, as well as for the absence of Ga in the surface layer, can be seen from the relative stability of the phases in the Cu-In-Ga-S-Se system. From a detailed study of the ternary and quaternary phases [23], it was found that the tolerance to Cu off-stoichiometry (i.e. being Cu-poor) is lower for the sulfides compared to the selenides. For an annealing temperature of 800-850°C, the selenides $CuInS_2$, $CuGaSe_2$ and $Cu(In,Ga)Se_2$ can tolerate Cu/III ratios down to 0.80-0.85 without formation of secondary phases, with the lowest values found for the Ga-rich phases. On the other hand, the sulfides $CuInS_2$, $CuGaS_2$ and $Cu(In,Ga)S_2$ have minimum Cu/III ratios of 0.96-1.00. In the present case our initial (selenide) CIGS layer has a Cu/III ratio of 0.82, very close to the minimum value for the selenides and far below the range of stability for the sulfides. Thus, it would actually not be possible to directly convert this material to a sulfide without undergoing phase decomposition (at least, under equilibrium conditions). Instead, the out-diffusion of cations mentioned above makes possible the formation of a stable sulfide with near-stoichiometric Cu-content. This process leaves the original CIGS layer even further depleted of Cu than it was to start with, i.e. further reducing the Cu/III ratio. This could explain the preferential loss of In to the surface, since Ga-rich CIGS is able to tolerate lower Cu-content than In-rich CIGS.

C. Correlation of materials properties and device behaviour

Based on the materials characterization it is clear that the annealing conditions investigated here result in formation of a CIS surface layer rather than a S/Se gradient. In the following the impact of this layer on device parameters will be discussed. Fig. 4 shows correlations between the $A1(Se-Se)/A1(S-S)$ ratio determined from Raman measurements and the device open circuit voltage (V_{OC}) and fill factor (FF) for both the annealing temperature and time series.

A clear correlation between the device performance and Raman mode ratio $A1(Se-Se)/A1(S-S)$ is discovered. A decrease of the ratio $A1(Se-Se)/A1(S-S)$ relates to formation of a thicker and more covering CIS layer. The increased CIS layer thickness in turn results an increased open circuit voltage. This is explained by a widening of the surface band

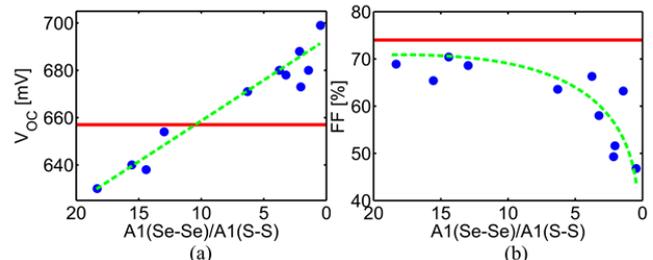


Fig. 4. Correlations between device parameters (A) V_{OC} and (B) FF for samples with different $A1(Se-Se)/A1(S-S)$ peak ratio calculated from Raman measurements. The red vertical line shows the device parameters for the reference device.

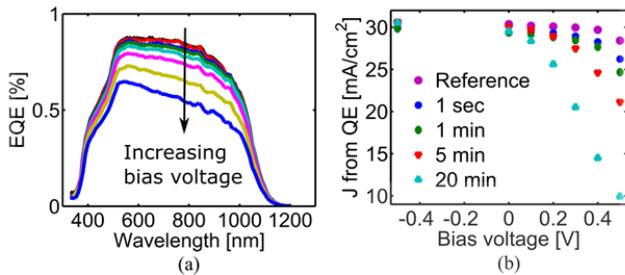


Fig. 5. (a) EQE of device (5 minutes at 500 °C sulfurization) measured under different bias voltages. (b) The current density extracted by integration of the measured EQE for different applied bias voltages.

gap by the Ga-rich interlayer and the CIS layer. It is noticed that the V_{OC} is reduced compared to the reference for samples with very small amount of CIS formation. There are several effects that could be the cause for this degradation. The CIS layer may not be growing uniformly in the beginning, causing areas with different diode properties. Other factors that can play a role in reducing the V_{OC} are changes in the back contact, redistribution of Na, and oxidation or introduction of impurities in the absorber surface. In STEM measurements not shown here we have observed that the $Mo(S,Se)_2$ layer increases in thickness at the back contact with increasing sulfurization time. In glow-discharge optical emission spectroscopy (GDOES) studies it was seen that the Na distribution in the surface region is modified and that the Ga gradient towards the back contact becomes less steep.

Fig. 4 (b) shows that the CIS layer formation is also accompanied with a reduction of the fill factor (FF). This can be explained by formation of a transport barrier for electrons at the interface. The band gap widening in the Ga-rich layer does not symmetrically move both conduction and valence bands. About 94% of the band gap increase is a result of the conduction band edge shifting up [24], which results in formation of a minority carrier barrier. The conduction band in the CIS layer is likewise expected to form a small spike of about 0.1 eV to the underlying CIGSe absorber. As the time or temperature is increased, the width of the CIS layer and concentration of interfacial Ga is increased. This leads to a more effective minority carrier barrier. The Ga accumulation increases the height of the barrier. The increased CIS thickness is likewise problematic, since the barrier moves toward the edge of the space charge region where the effective barrier increases due to the absence of an electric field.

A minor change was observed in the short circuit current (J_{SC}) of the devices after the sulfurization treatment. Samples with a small $A1(Se-Se)/A1(S-S)$ below 5, and therefore a thick CIS surface layer had J_{SC} of around 31 mA/cm². Samples with a thinner CIS layer and a $A1(Se-Se)/A1(S-S)$ ratio above 10

had a slightly lower J_{SC} of about 29.5 mA/cm². The combination of the losses in device parameters reduced the device efficiency from 15% of the untreated reference to 9.5-14% after sulfurization treatments.

In order to put presented interpretation to the test, EQE measurements were performed for different bias voltages as shown in Fig. 5(a). The dependence of the collection efficiency on bias voltage was quantified by calculation of the current density: $J = q \int QE(\lambda) \Phi_{AM1.5}(\lambda) d\lambda$. Fig. 5 (b) shows the result of the EQE integration for samples sulfurized for different durations. If the observed FF reduction would be caused by a diffusion length reduction, it would be expected that the integrated EQE is increased under reverse bias. As seen Fig. 5, this is not the case; hence a significant change in diffusion length is not affecting the FF . When measuring the EQE at forward bias it is seen that the integrated EQE is strongly reduced. It is noticed that the effect is stronger in devices with thicker CIS layers. This observation is in agreement with the idea that the FF reduction is caused by a photo carrier barrier. As the forward bias is increased or the CIS layer is extended the effective barrier increases, resulting in the drastic reduction in collection efficiency. The photo carrier barrier formed during the sulfurization treatment dominates these devices and leads to a reduced conversion efficiency.

D. SCAPS simulations of device behaviour

To support the explanation for the observed behaviour the device structure was modelled with the software SCAPS[25].

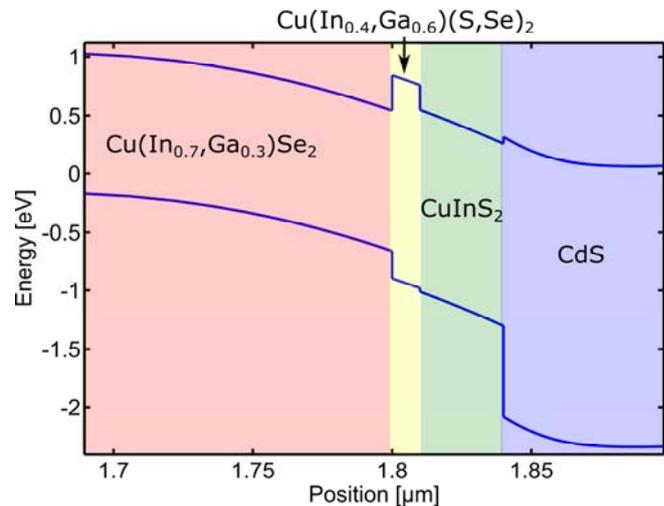


Fig. 6. SCAPS model of the band diagram of the interphase region between CIGSe and CdS.

TABLE I
SELECTED PARAMETERS FOR SCAPS MODEL

	$Cu(In_{0.7},Ga_{0.3})Se_2$	$Cu(In_{0.4},Ga_{0.6})(S,Se)_2$	$CuInS_2$	CdS
Band gap [eV]	1.2	1.74	1.56	2.4
Electron affinity [eV]	4.45	4.15	4.36	4.3
Thickness [nm]	1800	0* or 10	0 – 30	80
Doping density[cm ⁻³]	5E+16	5E+16	5E+16	2.5E+17

Some important modelling parameters used in this study. * A reference model is defined in which the Ga rich and CIS layers are left out.

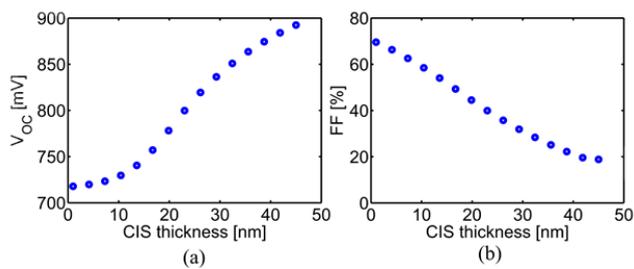


Fig. 7. SCAPS simulation of the (a) V_{OC} and (b) FF with increasing thickness of a CIS surface layer. The model includes a 10 nm thick Ga rich interlayer.

To simulate the device characteristics a model was defined based on commonly used materials parameters. In the CIGSe absorber a mid-gap defect is introduced to obtain a minority carrier diffusion length of 1.6 μm . In order to simulate the observed reaction layer the bulk CIGSe layer is split in three parts; bulk CIGSe, a thin Ga enriched layer, and a CIS surface layer. The only parameters changed in these surface layers are the band gaps and the electron affinities, as shown in table 1. The band gap was calculated from the measured chemical composition [20]. The electron affinities of the layers were estimated based on the assumption that 94% of the band gap widening of CIGSe when alloying with Ga originates from a shift of the conduction band edge [24]. When alloying CIGSe with S it is assumed that 43% of the band gap increase relates to the conduction band shift [24]. The resulting band diagram simulated with SCAPS is shown in Fig. 6. Especially the band gap widening caused by the Ga enrichment is expected to strongly affect the device characteristics.

In order to simulate the effect of the increasing annealing time or temperature, the model assumes a fixed Ga enriched layer, while the thickness of the CIS layer is varied. This is a simplification, since it is expected that both the magnitude of the Ga accumulation and CIS layer thickness both increase with annealing time. In spite of this simplification, it is possible to model trends that mirror the observed device behavior. Fig. 7 shows the effect of the increase of the CIS layer thickness on the V_{OC} and FF . Comparing this simulation to Fig. 4 it is clear that the qualitative trends are the same. The V_{OC} is increased due to the widened band gap. At the same time the FF is reduced since the effective barrier becomes larger as the conduction band step is pushed towards the edge of the space charge region.

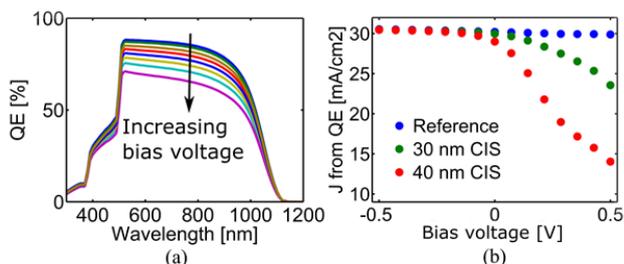


Fig. 8. SCAPS simulation of the effect of bias voltage on EQE. (a) Simulated EQE curves for bias voltages from -0.5 V to 0.5 V for a model with a 30 nm CIS surface layer. (b) The collection efficiency quantified by calculation of the current density via integration of the product of the EQE and the AM1.5 spectrum for a reference without Ga accumulation and CIS layer and two examples with a Ga pile up and different CIS layer thicknesses.

The idea that the barrier for charge carrier collection becomes more severe for thicker CIS surface layers was also put to the test by simulation of biased EQE. The current density is calculated with the same approach as the experimental biased EQE. The result shown in Fig. 8 should be compared to the experimental result shown in Fig. 5. Again it is seen that the trends observed experimentally are mirrored in the SCAPS model. For forward biases where the barrier is increased the collection efficiency drops significantly. This trend is clearly stronger for thicker CIS layers, while the effect is practically absent in a reference model, in which the surface layers were left out. These results support the idea that the devices are limited by formation of an electron barrier as a consequence of the sulfurization treatment.

One can speculate why the introduction of sulfur has a detrimental effect on the device performance when introduced in a post deposition step and a beneficial effect in the SAS process used for example by Solar Frontier [3]. Multiple effects could be responsible for this apparent discrepancy. Our samples did have a CdS coating that was subsequently etched off and a brief air exposure (2min) before the sulfurization treatment. Another possibility is that a part of the explanation relates to the Cu and Ga content in the surface, which impacts the sulfurization process [12]. Finally it should be kept in mind that the samples reacted here were fully selenized and crystallized before the sulfurization treatment. In the SAS process, on the other hand the sulfur is more easily introduced during the crystallization process [11]. This could be essential for successful sulfur gradient formation.

IV. CONCLUSIONS

The potential benefits from sulfurization of CIGSe in a post deposition treatment have been investigated. Instead of formation of a desired sulfur/selenium gradient, it is concluded that phase separation causes formation of a Ga- and Se-free CIS surface layer. The thickness of this layer increases with longer annealing time or higher temperature, but has not been avoided when only sulfur vapors are present in the annealing. When the CIS surface layer forms, Ga previously present in the CIGSe film, accumulates at the interphase between the CIGSe and CIS layers. The presence of these high band gap surface layers results in increased V_{OC} , but reduces FF because of hampered transport of electrons. As a result the device performance could not be improved by the sulfurization post deposition treatment in this study. In future studies it could be attempted to avoid formation of the Ga enriched layer by sulfurization of absorbers without Ga in the surface region. Annealing of CIGSe in both sulfur and selenium could also be investigated in an attempt to promote S/Se alloying instead of phase separation.

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