28 GHz circular polarized fan-out antenna array with wide-angle beam-steering

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Abstract

The article presents 28 GHz circular polarized antenna arrays designed in an embedded wafer level ball grid array (eWLB) package for 5G applications. The antenna arrays are realized on a re-distribution layer (RDL) in the fan-out region of the chip package. Two separate but identical arrays perform RX and TX operations where a crossed dipole is used as a building block of the array. These 4-element arrays have $\leq 10$ dB impedance bandwidth covering 25.3–29.8 GHz (4.5 GHz bandwidth) while presenting 10 dBi maximum realized gain. The measurement results show $<3$ dB axial ratio in the band 26–29.5 GHz, and the main beam can be steered in $\pm 50^\circ$ in the azimuth plane when array elements are fed by appropriate phases from the chip. The radio frequency module provides 31 dBm maximum equivalent isotropic radiated power (EIRP).

KEYWORDS

antenna array, antenna-in-package, beam-steering, crossed dipole, fan-out array

1 | INTRODUCTION

Millimeter wave (mm-wave) systems have gained more attraction in recent years because of advancements in cost effective process technologies and integration solutions.1 The relatively longer wavelengths in the microwave range ask for antenna array placement on a PCB separate from a radio frequency (RF) module, and the interface between the antenna array and RF module is normally made with connectors and RF cables. However, as the system size reduces at mm-wave frequencies, the performance is improved by reducing the distance between RF integrated circuit (RFIC) and the antenna array.2 The integration of antenna arrays with RFIC allows the antenna array to be placed inside the chip package, thus making an antenna in package (AiP) solution. Compared to traditional flip-chip and wire bonding, the fan-out wafer level packaging (FOWLP) has shown better electrical performance and higher design flexibility at mm-wave frequencies.3 Moreover, FOWLP minimizes 28 GHz interconnection losses of transition from chip to fan-out package to PCB, and small form factor AiP solutions are important prerequisites for 5G systems market.

Different fan-out (FO) antennas and antenna arrays are presented in the literature at 28,4–6 60,7–13 77,14–18 and above 100 GHz.19 Most of these designs use either double molding layers, multiple re-distribution layers (RDL), metallization on top mold, through mold VIAs, or
The variations make the package complex and thus cost-ineffective. Some of the designs implement only a single antenna element despite the small form factors at 60 GHz and 77 GHz. The package used in our work consists of 2×RDLs and a single mold compound (Figure 1) while four-element antenna arrays (Figure 2) are designed at RDL1 of the package. The antenna arrays cover the 28 GHz n257 frequency band (26.5–29.5 GHz). The article presents the measurement results for equivalent isotropic radiated power (EIRP), beam-steering in ±50° in the azimuth plane, axial ratio, polarization radiation pattern and error vector magnitude (EVM). These measurements are performed by having the antenna array integrated with an RFIC, and the measurements verify the simulations results.

2 | TRANSCIEVER CHIP AND PACKAGING TECHNOLOGY

The block diagram of the RFIC transceiver chip used in this work is shown in Figure 3. The chip is packaged using fan-out wafer level package (FOWLP) technology. The traditional packaging process involves dicing the dies from a wafer and then assembling them into a package. The fan-in wafer level package (FIWLP) however assembles a die into a package at the wafer level by using wafer fabrication tools and processes. An RDL is used to connect the I/Os of the chip to the bumps on top of the die surface. In the FIWLP, the final package is of the same size as the die itself, thus the technology produces true chip-scale package (CSP) which can be understood as a bumped die. This technique has advantages of good electrical performance, low cost and small size. However, a number of applications require high number of bumps under the chip, which becomes challenging for the FIWLP technology. The FOWLP technology solves this problem by introducing the fan-out region around the chip. FOWLP is an enhancement of standard WLPs where the chips are diced from a silicon wafer, precisely positioned on a carrier panel, and then molded. An RDL covers the die and the molded (fan-out) area, and the solder bumps are then connected on the RDL. The idea behind FOWLP is to introduce a bigger wafer beneath the actual wafer to create bigger die area which has more number of bumps for interconnections and also has a fan-out area that can be used to place the AiP. In comparison with an antenna array fabricated on an RF PCB, the
AiP not only results in reduced interconnection losses but is also a cost effective solution.

A cross-section of the 28 GHz transceiver chip packaging structure used in this work is presented in Figure 1. The 0.5 mm ball-grid array (BGA) package comprises three passivation layers (PSV1, PSV2, and PSV3), two RDL (RDL1 and RDL2) and a single mold layer. The antenna array is designed on RDL1 which radiates through the mold compound, whereas solder bumps connect the package with the PCB. The bumps right under the die are mainly used for baseband/RF signals, power and grounding, while the bumps on right, and left in the shown cross-section are mainly dummy and they are placed to ensure the mechanical stability of the package. The package is placed on a cost-effective FR-4 PCB whose thickness along with the prepreg is 1 mm. A metallic layer on other side of the prepreg acts as a reflector at λ/4 distance for the array in package which makes the antenna array more directive.

3 | ANTENNA ARRAY DESIGN

A crossed dipole antenna array is designed in this work on the RDL closer to the die (RDL 1) in the embedded wafer level ball grid array (eWLB) package. Figure 2 shows the top view of the package where a TX and an RX antenna arrays are placed at right and left of the die. The die is not exactly in the center because of which an extra line of solder bumps is placed towards the outer edge on the RX side. This has negligible impact on the performance of the array compared to the TX side. A differential pair is used to feed the crossed dipoles, which is more clearly presented in the zoom-in view. As we know from theory of a crossed dipole, each leg needs to be fed with a phase difference of 90° with respect to its neighbor legs. This can either be done by using four independent feed lines (one feeder for one leg) and providing 90° phase shift directly from the chip, or by feeding through a differential pair and adding a quarter wave long transmission line to feed the two opposite legs. However, because of space constraints in the fan-out area, circular polarization in this article is achieved by using different lengths of the two linear dipoles in a cross dipole, as suggested in Reference 22. Figure 4 shows the axial ratio at different frequencies in the band for varying length \( l_1 \) of the crossed dipole. It can be seen that the axial ratio gets better with increasing length of the longer dipole leg. \( l_1 = 1.45 \text{ mm} \) is used in the final design as this value also gives the best impedance matching for the whole band. The impedance bandwidth is considerably reduced for \( l_1 = 1.6 \text{ mm} \), though the axial ratio is better especially in the lower band. So \( l_1 = 1.45 \text{ mm} \) is a trade-off between axial ratio and impedance bandwidth. Moreover, the array is right hand circular polarized (RHCP) where broadside co- and cross-polarization levels are presented in Figure 5. The cross-polarization curve presents the left hand circular polarized (LHCP) power levels. The
cross-polarization rejection ratio (CPRR), that is, the difference between RHCP and LHCP, is maximum (26 dB) at 28 GHz. Besides, Figure 6 shows the active reflection coefficients for all eight ports on the RX side, where $\angle < -10$ dB impedance bandwidth ranges from 25.5 to 30 GHz. The array on the TX side shows similar impedance matching response.

The presence of dummy solder balls in the fan-out region has been investigated by simply simulating a microstrip patch antenna with and without the solder balls in the substrate. Adding these balls in the substrate does not affect the radiation pattern but causes a slight increase in the dielectric constant of the substrate. This increase in the dielectric constant is taken into account while designing the antenna array. Moreover, as shown in Figure 1, an aluminum heatsink is glued on top of the die with the help of a thermal conductive material to efficiently dissipate the heat. The die itself affects the radiation pattern in the elevation plane and makes the beam tilt away from the broadside, as shown by the red curve in Figure 7. Besides, adding heatsink further tilts the beam in the elevation plane, as shown by the blue curve. The same behavior is illustrated by peak gain curves for different frequencies in Figure 8 where the curves for broadside peak gain are lower in values than the curves related to the elevation plane. As the heatsink tilts the
main beam away from the broadside, the peak gain is higher at angles other than the broadside. The array has realized gain of more than 9 dBi from 25.5 to 29.5 GHz.

Figure 8 also shows the investigations in terms of peak gain for different values of pitch “p” between antenna elements. The upper curves in the plot, representing maximum realized gain in the entire elevation plane, are quite overlapping especially at lower end of the frequency band. The pitch cannot be increased more than 3.3 mm because of the package size. The gain is maximum in the band 26.75–29.5 GHz when p = 3.0 mm while it is slightly lower than maximum for the lower band. Besides, as gain is inversely proportional to the square of the wavelength \( G = 4\pi A_e / \lambda^2 \), the curves are going up with the frequency. Likewise, the lower curves in the plot represent the peak gain at broadside for different values of “p.” The gain remains minimum in the whole band for the lowest presented value p = 2.9 mm and increases with the pitch especially at the end of band. The value of pitch p = 3.0 mm is selected for final design which shows maximum gain in the elevation plane for higher frequency band. Though at broadside the gain is 0.2–0.4 dB lower for this value of p, it is finalized by keeping in view the impedance matching and axial ratio results. For this value of the pitch, peak realized gain lies in 8–10 dBi range.

As shown in Figure 1, a metallic reflector is used at a PCB thickness of 1 mm, which makes the distance from the dipole array approximately quarter wavelength when PCB-package airgap and PSV layers' heights are added up. The prepreg in place has similar properties as FR-4. The performance of the array is investigated for different values of the PCB height and the results show maximum realized gain, best impedance matching, and axial ratio performance for 0.730 mm FR-4 height.

4 | FABRICATION AND MEASUREMENT SETUP

The packaged chip with AiP is shown in Figure 9. Panel A shows the top view of the fabricated package where shining area in the middle is the die while black area in the surroundings is the molding compound used for packaging. Panel B of the figure shows the bottom side of the package where metallization on RDL1 and RDL2 is visible and the RX/TX antenna arrays can be seen on right/left in the panel, respectively. The solder bumps in these regions are mainly dummy and necessary for mechanical stability of the package, whereas the solder bumps present above the die, in the center up and the center down are mainly used for power, ground, and other signaling apart from mechanical support.

Figure 10A shows top view of the radio frequency module (RFM), where the package is mounted on the FR-4 PCB, while an aluminum heatsink is placed on top of the die and screwed with the PCB. A thermal interface material (TIM) is used between the die and the heatsink for efficient heat transfer. Panel B of the figure shows the back side of the PCB where an external local oscillator (LO) is placed along with other supporting electronics. A connector is also in place for connectivity with the evaluation board.

A passive antenna array structure is essentially required for complete characterization of the antenna array in terms of impedance matching and absolute gain. The manufacturing and then the measurement of this passive antenna array in the fan-out eWLB package is however an expensive and challenging option. Keeping this factor in view, final simulations results are made more reliable by incorporating all small details of the package/PCB.

A schematic diagram of the measurement setup is shown in Figure 11A. When testing the TX, 54 MHz baseband signal is generated by the signal generator which is passed through a 90° hybrid to generate I (in-phase) and Q (quadrature-phase) signals. These I and Q are then separately passed through 180° hybrids to get IP (in-phase positive), IN (in-phase negative), QP (quadrature-phase positive), and QN (quadrature-phase negative) signals to the evaluation board for 28 GHz module characterization. The device under test (DUT) is mounted on a gimbal which can rotate in both azimuth and elevation planes while receiver end is provided with a linear polarized (LP) horn antenna, fixed on a plate which can rotate in the plane perpendicular to the broadside direction of propagation. These rotations allow axial ratio and radiation pattern measurements of the circular polarized array. The power received by the LP horn antenna is then measured by a power meter. All components used in the measurements along with rotations on transmission and reception are controlled through MATLAB scripts. Figure 11B shows the actual setup where DUT is mounted on the gimbal placed on right side in the image and the LP horn antenna fixed on the other side.

5 | MEASUREMENTS

To measure the maximum EIRP of the module, the power sweep for five frequencies in the band is measured by progressively increasing the power of the baseband signal from −20 to 15 dBm. The measurements are made at broadside direction and results presented in Figure 12 show that the maximum EIRP ranges between 28.6 and 31.2 dB for the band 24–29.5 GHz and the value is
These results are in accordance with the simulations presented in Figure 8 (dark blue curve in the broadside peak gain bundle) as the peak realized gain also varies in 2.6 dB range for 24–29.5 GHz band and the gain is minimum for 24 GHz.

Figure 13 shows measured and simulated normalized radiation patterns in both azimuth and elevation plane at 28 GHz. The measured patterns agree fairly well with the simulations especially for azimuth plane. The elevation plane peak in the measurements appear at around 10° closer to the broadside in comparison with the simulations and the difference in the azimuth and elevation peaks is lower in the measurements compared to the simulations. This might be due to the measurement setup, as the radio frequency module is connected on top of the evaluation board which has a number of active electronic components along with a metallic support.

Furthermore, as chip is directly feeding the dipoles via the die pads, the phases of the RF signals can be changed to steer the beam in the azimuth plane up to ±50°. Figure 14A,B present simulation and measurement beam-steering results at 28 GHz. The measurements, shown in panel B, nicely follow the simulated patterns presented in panel A. The gain is slightly higher at ≈−50° compared with the opposite angle, that is, +50°, which is because of better impedance matching at −50°.

Axial ratio measurements are carried out by rotating the LP horn antenna around its axis in the plane perpendicular to the direction of propagation. At every 6° step, the rotation is stopped to measure the receive power which is recorded by MATLAB. Simulated and measured axial ratio for different frequencies are plotted in Figure 15 where measurements nicely agree with the simulations. Looking at the trend of the curve, it can be
said that axial ratio is less than 3 dB in the band 26–29.5 GHz. Figure 16A shows polarization radiation pattern at 28 GHz, which is measured is below steps:

1. DUT is placed at −90° azimuth angle from the broadside direction.
2. LP horn antenna is rotated around its axis in a complete circle in the plane perpendicular to broadside direction and measurements are made at every 6° steps. (Different circles in a column at −90° azimuth angle represent the power levels measured at these steps, shown in Figure 16A).
3. AUT is moved 4° toward the broadside (i.e., at −86° azimuth angle) and Step 2 is repeated.

The steps are repeated to get the polarization radiation pattern for all desired azimuth angles. The resolution of the pattern depends upon the step size used for DUT and for LP antenna. At any azimuth angles, the vertical range
of power levels defines the axial ratio at that azimuth angle, e.g., at $-90^\circ$, all different power levels lie between 0 and 10 dBm, so the axial ratio at $-90^\circ$ is 10 dB. Panel B of the figure shows a simpler presentation of the axial ratio in the azimuth plane. It compares the measurements with the simulations and the measurement curve can be seen to tally well with the simulations. The value of axial ratio is in the acceptable range in $-30^\circ$ to $+40^\circ$ range.

Figure 17 shows the error vector magnitude (EVM) measurements for an EIRP sweep from 10 to 30 dBm. The measurements are made with the help of Keysight
N9040B UXA Signal Analyzer (2 Hz–50 GHz) by using modulation and coding scheme 24 (MCS24) with 64 QAM (quadrature amplitude modulation). The 26.75 GHz curve achieves the 28 dBm EIRP for EVM < /C0 15 dB, which is in accordance with the EIRP results shown in Figure 12, as maximum EIRP is achieved at 26.75 GHz. While looking at all five frequency curves, the spread in power towards the higher EIRP values is around 4 dB at a fixed EVM.

6 | CONCLUSION

The article presents a crossed dipole fan-out antenna array designed at RDL1 in the eWLB package. The radio frequency module delivers 31 dBm maximum EIRP with the beam-steering in ±50° in the azimuth plane. The impedance bandwidth (−10 dB) covers 25.5–30 GHz band and the axial ratio is < 3 dB from 26 to 29.5 GHz. A comparison with the similar reported work at 28 GHz is presented in Table 1. The work reported in References 5,6,24 use multiple RDLs and double molding layers in comparison to this work which uses only 2 × RDLs and a single molding compound. Moreover, this work demonstrates the beam-steering capabilities of the circular polarized array in ±50° compared with Reference 26 which presents a linear polarized array with beam-steering only in ±35° in the azimuth plane. Keeping in view the performance of the array, the proposed solution is a good candidate for 28 GHz n257 (26.5–29.5 GHz) band.

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CONFLICT OF INTEREST

The authors have no conflict of interest to declare.

DATA AVAILABILITY STATEMENT

Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

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REFERENCES


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