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Vertical High-Voltage Transistors on Thick Silicon-on-Insulator

BY

ULRICH HEINLE

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ABSTRACT

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More and more electronic products, like battery chargers and power supplies, as well as applications in telecommunications and automotive electronics are based on System-on-Chip solutions, where signal processing and power devices are integrated on the same chip. The integration of different functional units offers many advantages in terms of reliability, reduced power consumption, weight and space reduction, leading to products with better performance at a hopefully lower price.

This thesis focuses on the integration of vertical high-voltage double-diffused MOS transistors (DMOSFETs) on Silicon-on-Insulator (SOI) substrates. MOSFETs possess a number of features which makes them indispensable for Power Integrated Circuits (PICs): high switching speed, high efficiency, and simple drive circuits. SOI substrates combined with trench technology is superior to traditional Junction Isolation (JI) techniques in terms of cross-talk and leakage currents.

Vertical DMOS transistors on SOI have been manufactured and characterized, and an analytical model for their on-resistance is presented. A description of self-heating and operation at elevated temperatures is included. Furthermore, the switching dynamics of these components is investigated by means of device simulations with the result that the dissipated power during unclamped inductive switching tests is reduced substantially compared to bulk vertical DMOSFETs.

A large number of defects is created in the device layer if the trenches are exposed to high temperatures during processing. A new fabrication process with back-end trench formation is introduced in order to minimize defect generation. In addition, a model for the capacitive coupling between trench-isolated structures is developed.

Ulrich Heinle, Department of Solid State Electronics, The Ångström Laboratory, Box 534, SE-75121 Uppsala, Sweden

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PREFACE

This thesis summarizes my work of the last five years at the Ångström Laboratory. I joined a project called "A'Capella", financed by the Swedish Foundation for Strategic Research (SSF), in 1997. The project was a collaboration of Chalmers Technical University, Gothenburg, Ericsson Microelectronics, Kista, and Uppsala University. This project's goal was to investigate and demonstrate the integration of high voltage devices and logic circuitry for telecommunications, i.e. subscriber line interface circuits.

The A'Capella project was superseded by the Auto-IC project in 2000. The academic partners were the same, and Volvo Technological Development Corporation and Volvo Car Corporation joined as industrial partners. This time the SSF provided the financial support as well. That project's goal was to investigate and demonstrate the integration of high voltage devices and logic circuitry for automotive electronics, for example electromechanical valve systems.

This thesis summarizes the following papers:

I **Integration of High Voltage Devices on Thick SOI Substrates for Automotive Applications**
U. Heinle and J. Olsson
Solid-State Electronics, **45** (2001) 629-632.

II **Vertical High Voltage Devices on Thick SOI with Back-End Trench Formation**
U. Heinle, K. Pinardi, and J. Olsson
Proc. 32nd ESSDERC (2002) 295-298.

III **Self Heating Effects of High Power SOI Vertical DMOS Transistor with Lateral Drain Contacts**
K. Pinardi, U. Heinle, S. Bengtsson, and J. Olsson
Physica Scripta, **T101**, (2002) 38-41

IV **Unclamped Inductive Switching Behaviour of High Power SOI Vertical DMOS Transistors with Lateral Drain Contacts**
K. Pinardi, U. Heinle, S. Bengtsson, J. Olsson, and J.-P. Colinge
Solid-State Electronics, **46** (2002) 2105-2110.

V **A Capacitance-Voltage Measurement Method for DMOS Transistor Channel Length Extraction**
J. Olsson, R. Valtonen, U. Heinle, L. Vestling, A. Söderbärg, and H. Norde
Proc. IEEE 1999 Int. Conf. on Microelectronic Test Structures **12** (1999)

135-140.

VI **Analysis of the Specific On-Resistance of Vertical High Voltage DMOSFETs on SOI**
U. Heinle and J. Olsson
Submitted to IEEE Transactions on Electron Devices (2002)

VII **Modeling and Characterization of Capacitive Coupling in Trench-Isolated Structures on SOI Substrates**
U. Heinle, L. Vestling, and J. Olsson
Submitted to Solid State Electronics (2002)

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CHAPTER 1

INTRODUCTION

The progress in microelectronics is normally illustrated using Moore's law [1]. He stated in 1965 that "the complexity of minimum component costs has increased at a rate of roughly a factor of two per year. ... there is no reason to believe that it [this rate] will not remain nearly constant for at least 10 years." This statement has become a self-fulfilling prophecy and is still valid. But Moore's law describes the progress in the digital world: memories and processors. Increasing the performance and density of these devices requires the shrinking of dimensions and as a consequence the reduction of the supply voltage. As consumers we are aware of this progress: our computers are always outdated and our mobile phones are always much bigger than those in the advertisements.

But there is at least one other world of microelectronics, which is not so popular but makes our lives a lot more comfortable: power electronics. Power electronic applications cover voltages from some ten volt up to several thousand volt. We are surrounded by power devices without noticing them. They are in our TV sets, audio amplifiers, lamps, toys, and cars; just to mention some application areas.

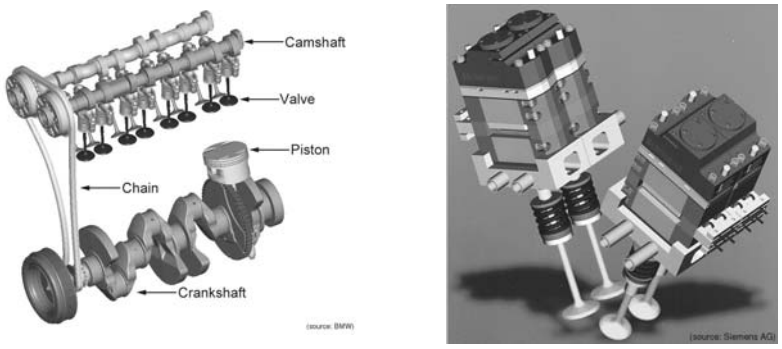
Power electronics has benefited from developments made in Very Large Scale Integration (VLSI) technology, i. e. fabrication of smaller and faster devices, whereas Power Integrated Circuits (PICs) additionally evolve towards greater flexibility. The System on Chip (SoC) concept combines signal processing parts and power actuators, leading to improved reliability, reduction of Electromagnetic Interference (EMI), and space and weight reduction [2]. A higher number of functions on a chip is superior to printed circuit boards because electrical connections on chips are more reliable than connections on circuit boards. However, technical feasibility turns into products only in conjunction with low costs.

Car manufacturers attach great importance to reliability and cost [3], especially for the emerging "x-by-wire" technologies, where x stands for steer or break. This concept is based on the idea of adding functionality and circumventing constrains of mechanical systems [4]. The cable connections between gas pedal and throttle and between clutch and gears will be replaced by electronic modules offering significantly greater flexibility [5].

Another example is the replacement of the camshaft itself and the associated valve drives by Electromechanical Valve (EMV) systems. The position of the valves in a conventional engine is determined in a highly symmetric way by the position of the pistons (see fig. 1.1(a)). This is because the camshaft, which opens the valves, is

connected to the crankshaft by a chain.

Variable valve timing is achieved by replacing the camshaft with electromagnets, shown in fig. 1.1(b). In this case the valves can be opened and closed independent of the pistons. The valve timing can be optimized with respect to fuel economy and emission at all engine speeds. As a result the fuel consumption can be reduced by at least 15% [6].



(a) (b)

Figure 1.1: a) The valves are opened and closed by the camshaft. b) The valves are opened and closed by electromagnets.

The average power requirement of an EMV system is approximately 100 $^{W}/_{cylinder}$, whereas the peak power requirement is substantially higher, approximately on the order of 1 $^{kW}/_{cylinder}$ [4].

Electronic devices with a high power handling capability are necessary to manage these power requirements. Furthermore, it is favorable to place the microcontrollers as close as possible to the sensors and actuators to meet the response times of these systems. This approach creates a number of new problems in cases like this where microcontrollers and actuators have to be placed in a harsh environment. It is important to maximize the reliability of the systems and the individual electronic control units as the complexity increases. One way of doing this is to reduce the number of discrete components in control units through high-level integration. An advantage of SoC solutions in this context is their reduced number of interconnections. Failure rates of material interfaces, like solder joints and packaging adhesives, dominate the total failure rate of electronic components in automobiles [7].

Silicon-on-Insulator (SOI) offers some advantages over conventional silicon, especially at elevated temperatures. The replacement of leaky pn-junction isolation makes it possible to raise the operating temperature of silicon-based electronics [8]. The higher price of SOI wafers and severe self-heating problems may delay or even inhibit the introduction of this technology.

In this thesis I will discuss issues related to high-voltage devices, isolation techniques, and integration of vertical Double Diffused Metal Oxide Semiconductor

(DMOS) transistors on SOI with a Complementary Metal Oxide Semiconductor (CMOS) compatible process.

CHAPTER 2

HIGH-VOLTAGE DEVICES

Power Integrated Circuit technology emerged in the late sixties when bipolar technologies, like voltage regulators and audio power amplifiers, could be integrated with logic circuitry. When consumer circuits were first developed, PIC technology quickly expanded to other areas such as the Subscriber Line Interface Circuits (SLICs) used in telephone switches. Bipolar power technology, however, has fundamental limitations, which narrow its usability. One of these is the phenomenon of second breakdown that limits the current capability. Another basic limitation of bipolar technology is that the driving power is far from negligible and cannot be reduced.

In the mid-80s the Bipolar-Complementary Metal Oxide Semiconductor-Double Diffused Metal Oxide Semiconductor (BCD) concept, which combines bipolar and Complementary Metal Oxide Semiconductor (CMOS) with Double Diffused Metal Oxide Semiconductor (DMOS) technology [9], was introduced . Bipolar devices were used for high power stages because of their high transconductance; CMOS was used for the logic because of its high layout density; DMOS Field Effect Transistors (FETs) were used for applications that require high output power and high switching speed [10]. The integration of control and protection circuits with vertical power devices lead to an increase of device reliability and performance. The main application fields were plasma display panels [9], switch mode motor drives [10], audio amplifiers [11], and automotive electronics, replacing mechanical relays and wire harnesses [12].

A variety of different devices has been used for integration, as can be seen in fig. 2.1. The following sections will give a brief overview of the most common gate controlled power devices.

2.1 VDMOS-Transistors

The invention of the power DMOS transistors in the 1970s [13] was partly driven by the limitations of Bipolar Junction Transistors (BJTs), which were the devices of choice in power electronics. In contrast to bipolar transistors DMOSFETs are majority carrier devices. Therefore, their switching speed is several orders of magnitude higher than that of bipolar transistors of similar size and voltage rating. They are superior to BJTs in high frequency applications, where switching power losses are important, and are able to withstand simultaneously high currents and voltages without undergoing destructive failure due to second breakdown. Power Metal Oxide Semiconductor Field

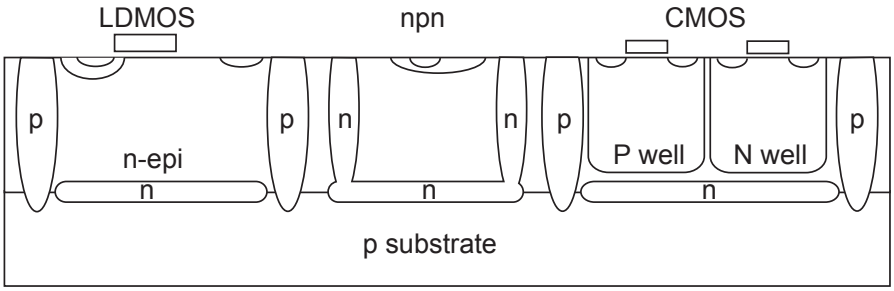


Figure 2.1: BCD structure with LDMOSFET, BJT, and CMOS transistors.

Effect Transistors (MOSFETs) are also immune to thermal runaway, since the forward voltage drop increases with increasing temperature, ensuring an even distribution of current among all cells.

DMOS transistors rely on control of lateral diffusion to achieve a short channel length. The term ”double-diffused” refers to the two consecutive ion implantation steps. For an n-channel device (fig. 2.2), the regions formed by double implant (self-aligned to the polysilicon gate) are first p-type and then n-type. The channel length is defined by the difference in their lateral diffusion. The p^+-area is created in a separate step.

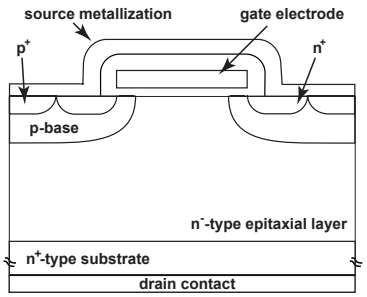


Figure 2.2: A DMOS is produced by first diffusing the p-base and then creating the source. The channel length depends on the lateral diffusion of the p-base and the source.

Applying a positive bias greater than the threshold voltage to the gate electrode, the silicon surface in the channel region will be inverted and a current starts to flow between the source and drain if a positive drain voltage is applied. The current flows first horizontally through the inverted channel and then vertically towards the drain contact. An important feature of the power MOSFET is the very high input impedance, which simplifies the gate drive circuitry, and reduces cost. It is a voltage-controlled device with no DC drive current-flow during operation.

The drift region has to meet two requirements. On the one hand it has to support the applied voltage in the OFF-state and on the other hand it has to carry the current in the ON-state. Here we are dealing with a trade-off as we will see in section 2.5 on page 8 because a higher breakdown voltage results in an increasing on-resistance.

2.2 LDMOS-Transistors

Lateral Double Diffused Metal Oxide Semiconductor (LDMOS) FETs [14], devices with gate, source and drain at the surface and with current flow parallel to the surface (see fig. 2.3), have been used for integration from the beginning of BCD technology [15]. Their use simplifies the manufacturing process because buried layers, which form the drain contact of vertical DMOSFET in BCD processes, are not necessary. It is

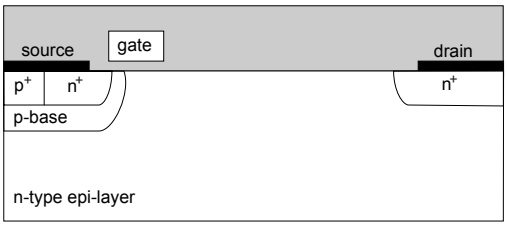


Figure 2.3: Schematic drawing of a lateral DMOS transistor.

possible to increase the breakdown voltage and reduce the on-resistance by modifying the surface charge in the drift region. This process, called Reduced Surface Field (RESURF) principle, will be discussed in more detail in section 2.6.3 on page 15. Devices with breakdown voltages of 1200 V have been demonstrated based on this technology [15, 16]. LDMOS transistors are used for telecommunication because of their short channel that is necessary for high operation speed and their good power handling capability. Power densities of 1 W/mm at 3.2 GHz [17] have been reached with a dual-layer RESURF drift region [18], see fig 2.4.

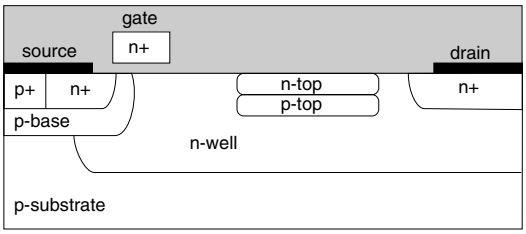


Figure 2.4: Lateral DMOSFET with a dual-layer RESURF drift region (courtesy of L. Vestling [19]).

2.3 IGBTs

The concept of a Metal Oxide Semiconductor (MOS)-controlled bipolar device was developed to overcome the limited current densities of MOSFETs and to get around the high base drive currents of BJTs [20]. This effort led to the Isolated Gate Bipolar Transistor (IGBT), shown in fig. 2.5 , a device that fundamentally changes the BJT current control into voltage control while maintaining the advantages of a minority carrier device. Electrons flow in the ON-state from the n^+-region through the channel into the

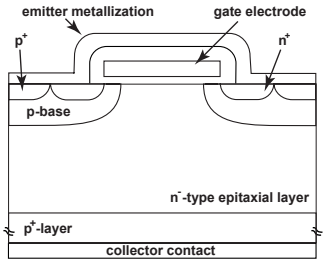


Figure 2.5: Schematic drawing of an IGBT.

drift region. This provides the base drive current of a wide-base pnp transistor. With increasing collector voltage the p^+-emitter injects holes into the n^--drift region until it exceeds the background doping level of the drift region. Compared to DMOSFETs this conductivity modulation leads to a tremendous reduction of the on-resistance [21].

During turn-off the huge amount of minority carriers has to be removed from the n^--drift region. This leads to a current flow after turn-off and also to lower switching speed and higher turn-off losses of the IGBT.

The Lateral Isolated Gate Bipolar Transistor (LIGBT) (see fig. 2.6) is used for high-voltage Integrated Circuits (ICs). Its on-resistance is about 5 to 10 times lower than that of a comparable LDMOSFET. LIGBTs are used for lamp-ballast, motor drives [22], and half-bridge inverter circuits [23].

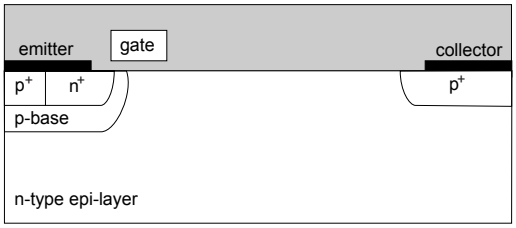


Figure 2.6: Schematic drawing of a lateral IGBT.

2.4 Super-Junction Devices

A new class of power devices, called super-junction devices, has been introduced theoretically in 1997 [24] and the first working transistors have been presented in 1998 [25].

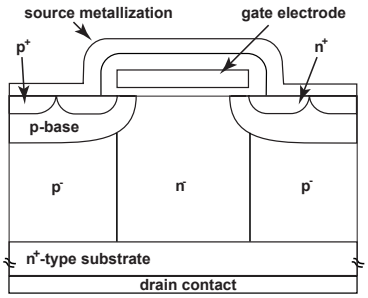


Figure 2.7: Cross section of a super-junction transistor.

A sequence of epitaxial depositions of lightly n-doped silicon and boron implantation steps is used to manufacture the devices, shown in fig. 2.7. The doping concentrations of the p^-- and n^--columns are optimized to deplete both columns horizontally at rather low voltages in the OFF-state. The drift region is then fully depleted and acts like a voltage sustaining layer of a pin-diode. The doping concentration of the current conducting n^--columns can be increased inverse proportional to their width [26]. Compared to conventional vertical DMOS transistors the conduction losses of a super-junction transistor can be reduced by a factor of 5 by increasing the drift region doping concentration by one order of magnitude [27]. Thus, the so-called silicon limit (section 2.5.2 on page 12) can be surmounted by this technique.

Single gate and double gate lateral versions of these devices were proposed in 1998 [28, 29]. Fig. 2.8 shows a cross-section of a 3D RESURF diode, which is sufficient to explain the operational principle of the device. The p-type and n-type silicon layers are deposited on an SOI substrate. The electric field of a conventional p^+n or n^+p-junction has its maximum at the physical junctions of the two materials. In case of a 3D-RESURF diode, the electrical field at these junctions is lowered because of a potential continuity at the p^-n^--junctions. This means that the potential lines are pushed to the center if the transverse pn-junctions are fully depleted in the OFF-state.

2.5 Common Parameters

The comparison of semiconductor devices can be based on many different parameters depending on the application they are designed for. The switching speed of transistors is most important for microprocessors and memories. The power dissipation is very important for devices of battery driven applications, like mobile phones and

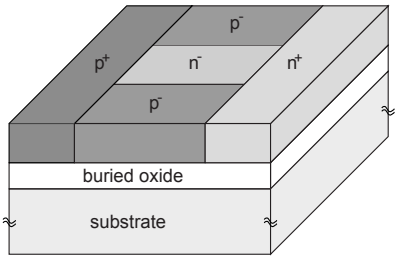


Figure 2.8: Schematic drawing of a 3D-RESURF diode.

notebooks. Two important parameters of power devices are breakdown voltage and on-resistance. The breakdown voltage defines the maximum voltage that can be applied to the device, and the on-resistance limits the current handling capability. The following two sections will show that these parameters cannot be designed independent of each other.

2.5.1 Breakdown Voltage

An important feature that all power devices have in common is their ability to block high voltages. The voltage is supported across pn-junctions, metal-semiconductor interfaces or MOS structures. The voltage handling capability is limited by material parameters and by the layout of the devices.

Avalanche Breakdown

The high electric field in the depletion region of a reverse biased pn-junction sweeps out any mobile carriers entering this region. Raising the applied voltage leads to an increase in the depletion layer width and a higher electric field that accelerates electrons and holes to higher velocities. If the electric field within the device exceeds a certain limit the charge carriers gain enough energy that they can excite electrons from the valence band to the conduction band by collisions, called impact ionization. The newly generated electron-hole pairs can in turn excite other electrons. Thus, we face a multiplicative process that creates a huge amount of mobile carriers. This condition is called avalanche breakdown if the impact ionization rate becomes infinite [30].

It is assumed that the depletion layer of an abrupt junction diode, formed by a n^+p-junction, extends only into the lightly doped side of the junction. Therefore, the Poisson's equation needs to be solved only for the p side of the structure in order to calculate the parallel plane breakdown voltage BV_{pp} [31]:

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{Q(x)}{\varepsilon_s} = \frac{qN_A}{\varepsilon_s} \tag{2.1}$$

where Q is the charge of the depletion layer, q the electron charge, ε_s the dielectric constant of silicon, and N_A the acceptor doping concentration. We can get the field

distribution by integrating eq. 2.1:

$$E(x) = \frac{qN_A}{\varepsilon_s} \cdot (W - x) \tag{2.2}$$

A second integration leads to the potential distribution:

$$V(x) = \frac{qN_A}{\varepsilon_s} \cdot (Wx - \frac{x^2}{2}) \tag{2.3}$$

Assuming that the number of generated electron-hole pairs becomes infinite, we can calculate the critical depletion layer width $W_{c,pp}$ at breakdown by correlating the electrical field with the ionization coefficient [32]:

$$\int_0^W 1.8 \cdot 10^{-35} \left[\frac{qN_A}{\varepsilon_s} (W - x) \right]^7 dx = 1 \tag{2.4}$$

$$W_{c,pp} = 2.67 \cdot 10^{10}\, N_A^{-7/8} \tag{2.5}$$

The breakdown voltage of the abrupt parallel plane junction is obtained by setting $x = W$ in eq. 2.3 and using $W = W_{c,pp}$:

$$BV_{pp} = 2.67 \cdot 10^{10}\, N_D^{-7/8} \tag{2.6}$$

These expressions are plotted in fig. 2.9. It can be seen that the breakdown voltage as well as the depletion layer width increases with decreasing doping concentration. This means that the on-resistance increases with growing breakdown voltage. Thus, it is important to design devices in such a way that the breakdown voltage is as close as possible to the theoretical maximum.

The above analysis has focused on parallel plane junctions, which can be described as a one-dimensional problem. In practical power devices, however, two- and three-dimensional effects associated with the diffused junctions result in field crowding near the junctions' cylindrical and spherical portion. This field crowding effect can greatly reduce the breakdown voltage from the parallel plane junction value given by eq. 2.6. As the diffused junction depth is decreased the field crowding becomes worse, which results in an even lower breakdown voltage. Analytical expressions for the breakdown voltage calculations of cylindrical and spherical junctions can be found in [30].

Surface Breakdown

The analysis of the previous paragraph was based on the assumption that there is no charge at the surface of the semiconductor above the depletion layer. The presence of positive surface charge will cause the depletion layer at the surface to extend further because it compensates for the negative charge of the depletion layer (of the lightly p-doped side; see fig. 2.10). The presence of negative charge has the opposite effect. It leads to an enhanced field crowding, resulting in a reduced breakdown voltage [33].

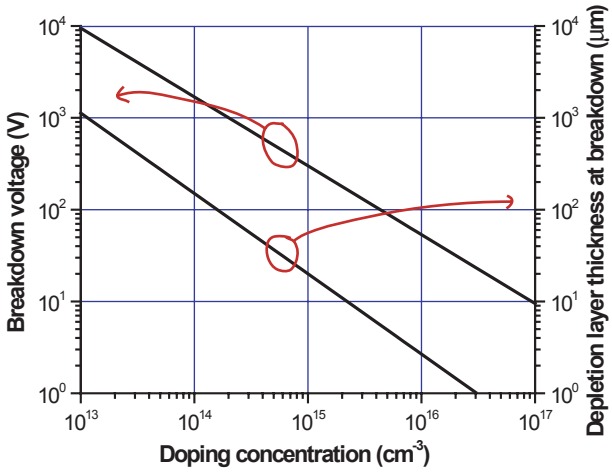


Figure 2.9: Breakdown voltage and depletion layer thickness for an abrupt parallel plane diode.

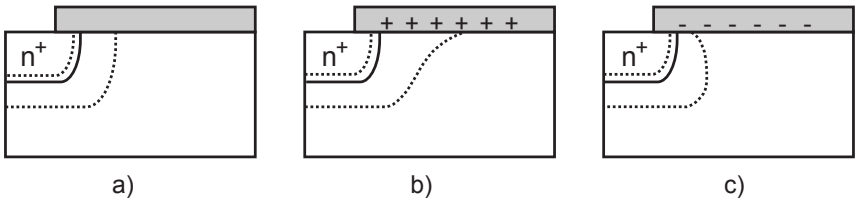


Figure 2.10: Dependence of the depletion layer on surface charge: a) no charge, b) positive charge, and c) negative charge.

Gate Oxide Breakdown

The breakdown mechanisms discussed in the previous paragraphs are normally non-destructive. This means that a device that experiences an avalanche breakdown will work in the expected manner if the applied voltage is reduced again. The gate oxide breakdown is one example of a destructive breakdown. This kind of defect can be created if too high voltages are applied to one or several of the device terminals. In this case a leakage path between the gate and the silicon is created and transistor action of the device is lost. Electrostatic discharge events very often trigger these kinds of events.

2.5.2 On-Resistance

The overall drain-source resistance in the ON-state, on-resistance R_{on}, determines the total current rating of a device. The conduction losses P_c are given by [34]

$$P_c = I_D \cdot V_D = I_D^2 \cdot R_{on} \tag{2.7}$$

The dissipated power cannot exceed a certain limit without leading to the destruction of the device. This means, that it is possible to increase the current handling capability by reducing the voltage drop of the device in the ON-state.

The on-resistance of a DMOSFET consists of several components, as shown in fig 2.11.

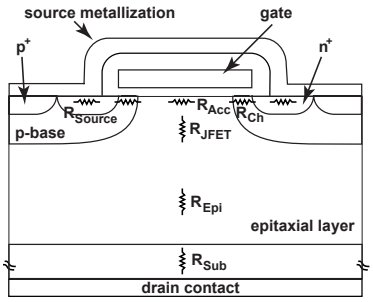


Figure 2.11: The total on-resistance of a DMOSFET consists of many parts.

The *source resistance* includes the highly doped n^+ area and the contact resistance. Its contribution to the total resistance is normally very small for high voltage devices. Its value can be reduced by using silicides and by a "smart" design of the device because the source resistance is dependent on the size of the contact.

The *channel resistance* R_{Ch} is dependent on the gate oxide thickness, the ratio of the channel length L_{Ch} and channel width W, the mobility, and the applied voltage at the gate electrode. Its value can be minimized by decreasing its length and increasing its width or by decreasing the gate oxide thickness. In the latter case, the gate-source voltage has to be reduced in order to avoid breakdown of the thinner gate oxide.

The *accumulation layer resistance* R_{Acc} is dependent on the charge in the accumulation layer and the surface mobility of the charge carriers. Its value can be lowered by decreasing the gate length or by adjusting the surface doping concentration.

The contribution of the *Junction Field Effect Transistor (JFET) resistance* R_{JFET}, the resistance of the region between the p-base diffusions, depends on the spacing and depth of the p-base diffusions (i.e. gate length) and the doping concentration of the drift region. Its value can be decreased by increasing the gate length or by raising the doping concentration.

The *resistance of the epi-layer* R_{Epi} is dependent on its doping concentration and its thickness. Its value can be lowered by increasing the doping concentration or by decreasing the thickness of the epi-layer.

The *resistance of the substrate*R_{Sub} is dependent on its doping concentration and its thickness. Its contribution to the total on-resistance is only significant in low voltage devices. Its value can be lowered by increasing the doping concentration or by decreasing the thickness of the substrate.

The relative contributions of the different resistive parts can be seen in fig. 2.12. The resistance of the epitaxial layer dominates R_{on} for high voltage devices. Thus, the

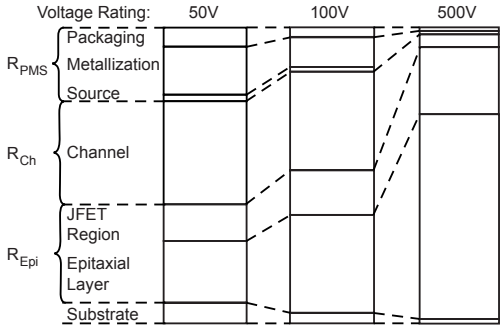


Figure 2.12: Relative contributions to the on-resistance by its different components for different voltage ratings [34].

modification of the drift region resistance should have a significant effect on the total on-resistance. We are dealing with a trade-off here because a desired high breakdown voltage requires a thick, lightly doped epi-layer. Consequently, the on-resistance will increase. The dependency of R_{on} on BV can be expressed by the following law, called "silicon limit" [35]:

$$R_{on} \propto (BV)^{2.4-2.6}. \tag{2.8}$$

2.6 Junction Termination

In section 2.5.1 on page 9 we have calculated the breakdown voltage of parallel plane junctions. In real devices we are facing junctions that are not plane because they have

to terminate somewhere. Cylindrical junctions will be formed at edges of implantation windows and spherical ones at their corners [36]. The 2D and 3D nature of the electric field gradient in the periphery of the implanted areas leads to a lower breakdown voltage. The goal of junctions terminations is to create a potential distribution that is similar to that of the parallel plane junction.

2.6.1 Field Plates

One method for reducing the depletion region curvature is by altering the surface potential, as we have seen in section 2.5.1 on page 10. This can be achieved by extending the junction metalization over the oxide. A depletion layer forms under the field plate since the same voltage is applied to it as to the main junction. The result is a reduction of the field crowding at point A. A high electric field can occur at point B depending on the oxide thickness and the depth of the junction [37].

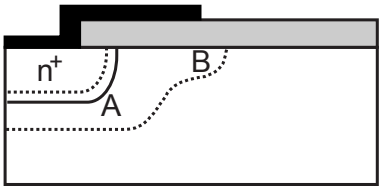


Figure 2.13: Planar junction with field plate.

2.6.2 Field Rings

A second approach to reduce the electric field at the junction edges is to implant rings surrounding the main junction as illustrated in fig. 2.14. These rings and the main junction can be implanted simultaneously and must not be contacted. The potential of

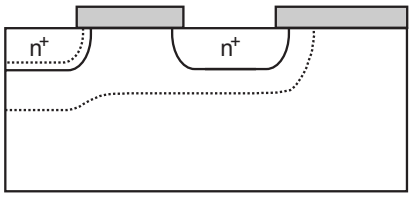


Figure 2.14: Edge termination with a floating field ring.

these floating field rings lies at an intermediate value between the applied voltage at the main junction and zero when the rings are placed within a depletion layer thickness from the main junction.

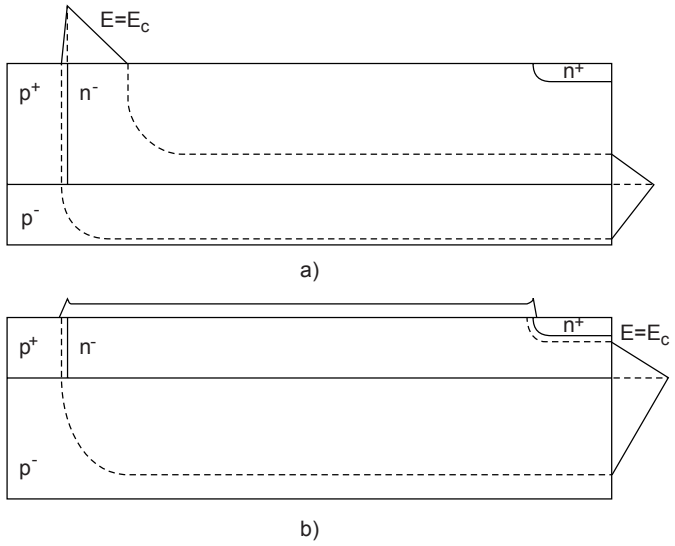


Figure 2.15: Depletion layer and electric field distribution for two diode structures.

The effectiveness of the floating field ring depends upon its exact spacing from the main junction. Another important design parameter is the width of the field ring. It can become ineffective when its width is too small. It is common to use several field rings in conjunction with field plates in order to achieve high breakdown voltages. The field plates reduce the field crowding at each field ring and prevent that charges at the surface alter the surface potential. Analytical expressions for the design parameters can be found in [30].

2.6.3 RESURF-Termination

A higher breakdown voltage can be achieved by a Reduced Surface Field effect [38]. The principle of operation is explained with the help of a diode (see fig. 2.15) consisting of an epitaxial n^- layer on top of a p^- substrate. The diode consists of a lateral p^+/n^--junction and a vertical n^-/p^--junction. In the case of the thick device layer the maximal electric field occurs at the surface, i. e. at the p^+/n^--junction, which has a lower breakdown voltage than the vertical n^-/p^--junction. In the case of the thin device layer the maximal electric field occurs at the vertical n^-/p^--junction because the lateral depletion layer is superimposed by the vertical depletion layer. This 2-D effect causes a reduction of the surface field, while the highest electric field is found at the n^-/p^--junction. The RESURF principle can be used for vertical high voltage transistors to decrease the electrical field at the devices' periphery. The transistor in fig. 4.8 on page 28 has a p-type junction termination extension that causes a very uniform spreading of the potential lines. If the dose of the implanted charge is too low it will have

little influence on the electric field distribution and the maximum electric field will occur at the edge of the source region. If the dose is too high the breakdown will have simply shifted to the edge of the p^- region.

To obtain a considerable reduction of the electric field it is essential that the implanted region is completely depleted under reverse bias. When regarding Gauss´s law an expression for the implanted dose can be derived:

$$\oint \vec{E} d\vec{A} = \frac{1}{\varepsilon} \int \rho dV \tag{2.9}$$

$$E = \frac{1}{\varepsilon} \cdot \frac{Q}{A} = \frac{q}{\varepsilon} \cdot \text{implanted dose} \tag{2.10}$$

where E is the magnitude of the electric field, ε the dielectric permittivity, ρ the charge density, Q the total integrated charge, q the elementary charge, and A the area.

The lateral extension of the RESURF termination can be reduced by using a step doping profile [39]. A second implantation step with a lower dose is needed for this technique and requires an additional mask step. A second approach to decrease the dimensions of the termination is the lateral variation of the doping profile [40]. A decreasing doping concentration is achieved with a single implantation step by reducing the width of the mask openings with increasing distance from the main junction.

CHAPTER 3

ISOLATION TECHNIQUES

The most important feature of intelligent power ICs is that a large power can be controlled by logic level input signals and that all power circuits, such as driving circuits, sense circuits, and protection circuits, are isolated from the logic circuitry. The isolation techniques can be roughly divided in two categories: Junction Isolation (JI) and Dielectric Isolation (DI). JI is a method that uses reverse-biased pn-junctions to isolate different devices. It is a well established and mature technique. Compared to traditional JI techniques dielectric isolation offers many advantages, but high production cost has impeded the introduction of this method.

3.1 Junction Isolation

Junction Isolation is the most common isolation technique and has been used for a long time. Fig. 3.1 shows a typical junction isolation structure. An n-type epitaxial layer is grown on top of a p-type silicon substrate. P-type sinker plugs are created by a diffusion step, so that they reach the substrate. The resulting n-type islands are isolated from each other by keeping the substrate potential on the lowest level, so that the pn-junctions will be reverse-biased.

High voltage ICs require thick device layers, which in turn need deep sinker plugs. Deep diffusion goes hand in hand with large lateral diffusion, resulting in a large isolation area. But that is not the only disadvantage of this technology. The leakage currents related to the reverse-biased pn-junctions grow exponentially with temperature [41] and can trigger parasitic bipolar devices.

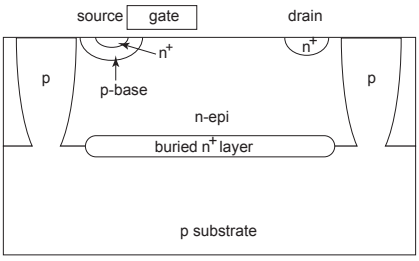


Figure 3.1: Typical junction isolation structure.

3.2 Silicon-on-Insulator

SOI technology, more specifically Silicon-on-Sapphire (SOS), was originally invented for the niche of radiation-hard circuits. Improved radiation hardness is achieved by eliminating the space charge regions of reversed biased pn-junctions. A variety of SOI structures have been developed with the aim of dielectrically separating the active device layer from the silicon substrate by a Buried Oxide (BOX). SOI offers several advantages for IC manufacturing: it suppresses leakage currents, reduces power consumption and increases significantly the speed of CMOS applications. The demand for high performance microprocessors and low power portable devices has created a much larger market for SOI technologies. This development has led to a decrease of the wafer price.

A number of different ways to produce SOI wafers have been invented:
Separation by Implantation of Oxygen (SIMOX) is based on the internal oxidization of silicon. Oxygen is implanted with a dose of $1.4 \cdot 10^{18}$ cm^{-2} to form a 400 nm thick oxide layer [42]. It is necessary to employ a high temperature anneal at 1300 °C for 6 hours to recover a high crystalline quality of the silicon surface layer. High current (80-100 mA) implanters are available to produce 300 mm wafers [43] with good thickness uniformity, low defect density, sharp Si-SiO_2 interface, robust BOX, and high carrier mobility.

SMART CUT uses the deep implantation of hydrogen into an oxidized silicon wafer [44]. After bonding this wafer A to a second wafer B and subsequent annealing to enhance the bonding strength, the hydrogen-induced microcavities coalesce and the two wafers separate at a depth defined by the location of hydrogen microcavities. The process is completed by polishing the thin silicon layer to achieve a uniform layer thickness. The thickness of the silicon film and/or buried oxide can be adjusted to match several device configurations (ultra-thin CMOS or thick-film power transistors and sensors).

Epitaxial deposition of silicon is necessary for both processes, SIMOX and SMART CUT, in order to obtain thick device layers.

ELTRAN technology is based on the splitting of porous silicon layers with a water-jet [45]. A seed wafer is anodized and two silicon layers with different porosities are formed. A single-crystal silicon layer is epitaxially grown and thermally oxidized to form an insulating layer. The seed wafer is bonded to a handle wafer and a water-jet is used to split the wafer at the interface of the two porous silicon layers. The remaining porous silicon on top of the silicon dioxide is etched and the surface is smoothed in a hydrogen anneal.

BESOI, Wafer Bonding and etch-back, stands as a rather mature SOI technology [46]. An oxidized wafer is mated to another SOI wafer. The challenge is to drastically thin down one side of the bonded structure in order to reach the targeted thickness of the silicon film. The advantage of wafer bonding is to provide unlimited combinations of BOX and film thicknesses.

3.3 Trench Isolation

The area consumed by the lateral isolation structures can be reduced tremendously by the use of deep trench technology. Plasma etch processes offer the possibility to etch deep trenches with vertical sidewalls. Reactive Ion Etching (RIE) [47], Electron Cyclotron Resonance (ECR) [48], and Inductively Coupled Plasma (ICP) [49] sources have been used for this purpose. ICP tools have the advantage that high plasma densities can be achieved at low pressures. The high plasma densities are needed to obtain high etch rates and a low pressure operation reduces electron scattering and consequently improves the control of etch profiles.

Chlorine based gases are used in RIE systems. Ion bombardment is necessary in these processes because chlorine radicals cannot etch silicon without ion assistance. Anisotropy of the etch process is achieved by the perpendicular impact of the ions on the surface. Chlorine was replaced by fluorine in order to obtain higher etch rates. Fluorine radicals etch silicon spontaneously without ion assistance, thus the etch process is isotropic. A passivation of the trench sidewalls is necessary for an anisotropic etch process in this case. The Bosch approach [50, 51] is based on a sequence of alternating etch and passivation steps. During the passivation step C_4F_8 is used and a fluorocarbon polymer is deposited on all surfaces. The passivation step is followed by a etch step with SF_6. The passivating film is removed from horizontal surfaces by ion bombardment whereas the vertical trench sidewalls are still covered by the polymer. The bare silicon surface in the trenches is etched isotropically for a short time. Highly anisotropic profiles can be achieved as the vertical etch rate is higher than the lateral etch rate [52], see fig. 3.2.

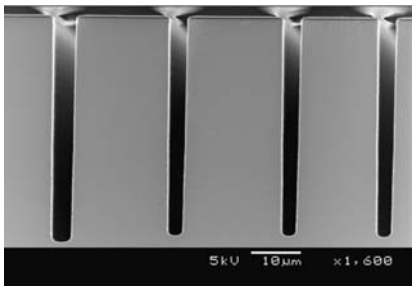


Figure 3.2: 4 µm and 5 µm wide trenches etched with the Bosch process.

The original Bosch process cannot be used on SOI wafers because of a lateral etching effect at the Si/SiO_2 interface, which is called notching (see fig. 3.3(a)). The undercutting is related to a accumulation of positive charges in the buried oxide, deflecting incoming ions to the trench sidewalls (see fig. 3.3(b)) [53, 54]. The first attempt to circumvent this problem was to use the conventional ICP etch process and switch to a second process with modified parameters right before reaching the buried oxide. The big problem of this two-step approach is to define the right point of time to end the first etch process (see fig. 3.4).

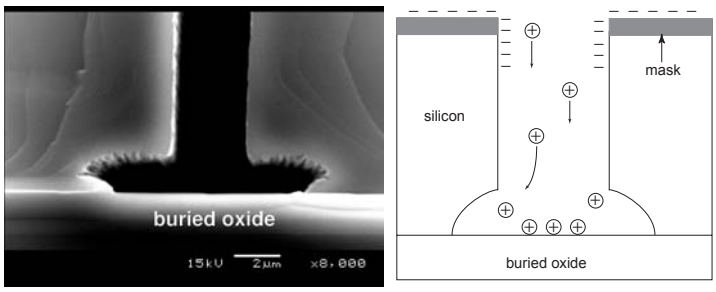


Figure 3.3: a) Lateral etching at the Si/SiO_2 interface. b) Positive charges at the base of the trenches deflect incoming ions to the trench sidewalls.

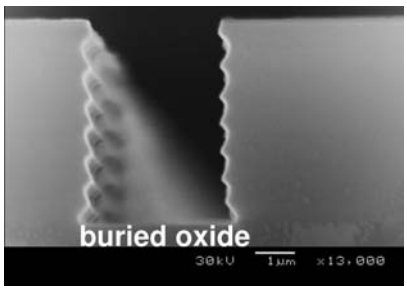


Figure 3.4: Etched trench on SOI without notching. The ripples come from the alternating etch and passivation steps.

A second, more practicable attempt uses an operating frequency of 380 kHz instead of 13.56 MHz. At this frequency the ions respond to a greater extend to potential variations, resulting in a larger number of low energy ions compared to the high frequency case. These low energy ions can neutralize the negative charge at the top of the trenches. Electrons can now reach the bottom of the trenches and neutralize the positive charge in the buried oxide [53, 54].

The ripples at the trench walls in fig. 3.4 are very pronounced. This can be avoided by decreasing the time of the etch cycles. The breakdown characteristics of the trenches can be improved by oxidizing them and removing the oxide. This will smooth out the ripples, which can cause field crowding at their tips. The trenches will be filled with silicon dioxide and polysilicon. The excess polysilicon at the surface is removed in a Chemical-Mechanical Polishing (CMP) step. Fig. 3.5 shows 50 µm deep trenches filled with silicon dioxide and polysilicon. A slightly V-shaped form of the trenches is necessary for a void-free filling.

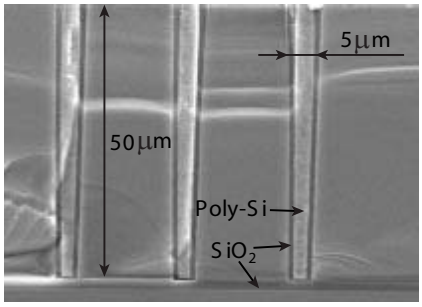


Figure 3.5: Trenches on SOI filled with 0.8 µm silicon dioxide and 3.4 µm polysilicon.

CHAPTER 4

INTEGRATION OF VDMOSFETS ON THICK SOI

This chapter will present the processes we have developed and some of the key results we have achieved within the A'Capella and Auto-IC projects. A more detailed discussion can be found in the attached publications.

I have used starting material from BCO Technologies to produce vertical DMOS transistors on SOI. The device layer is 50 µm thick, has a doping concentration of $4{\cdot}10^{14}$ cm^{-3} and the buried oxide is 2µm thick. Arsenic has been implanted into the backside of the device layer prior to bonding with a dose of $5{\cdot}10^{15}$ cm^{-2} and an energy of 80 keV. BCO Technologies etched and refilled the trenches of the first batch. The trenches of the back-end trench formation process have been etched at QinetiQ and refilled in Uppsala. A schematic drawing of our devices is given in fig. 4.1

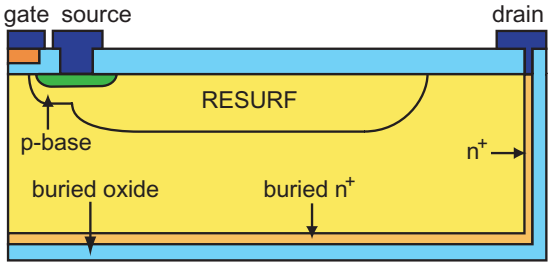


Figure 4.1: Schematic drawing of a DMOSFET on SOI with trench isolation.

We have included a great number of different devices in our mask-set in order to demonstrate the CMOS compatibility of our process: VDMOSFETs, LDMOSFETs, nMOS and pMOS transistors, BJTs, and diodes. Fig. 4.2 shows a device with 267 cells.

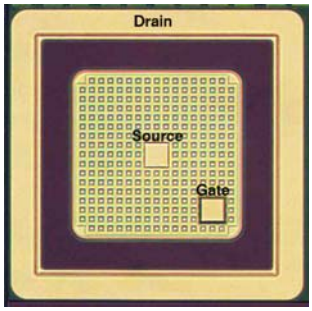


Figure 4.2: Top view of a DMOSFET with 267 cells.

4.1 Process Description

Extended process simulations have been carried out with the device simulators Athena from Silvaco International and Dios from ISE. The purpose of these simulations is to save time and money in the lab. This requires that the simulators have to be calibrated with the real processes.

The following process flow was used for the first batch:

- Arsenic implantation into the backside of the device layer and bonding
- Trench etching, phosphorous diffusion into the trench side-walls, Chemical Vapor Deposition (CVD) oxide deposition (0.8 µm), polysilicon deposition, CMP
- Boron implantation of $2.8 \cdot 10^{12}$ cm^{-2} followed by a high temperature anneal (1200 °C, 15 h) to form the RESURF termination
- Gate oxide growth (500 Å)
- Polysilicon deposition and gate etch
- p-base implantation (boron, $6 \cdot 10^{13}$ cm^{-2}) and anneal (1100 °C, 120 min)
- Contact implantations
- CVD oxide deposition and contact hole etch
- Metalization

4.1.1 Defect Generation

After the high temperature anneal at 1200 °C we could see defects spread over the whole surface of the wafers (see fig. 4.3). These defects originate from slip dislocations [55] and are normally generated along (111) planes [56]. The defect generation is dependent on the doping concentration. This is the reason why there are no defects

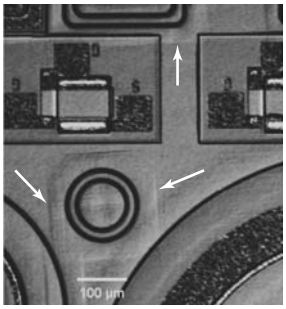
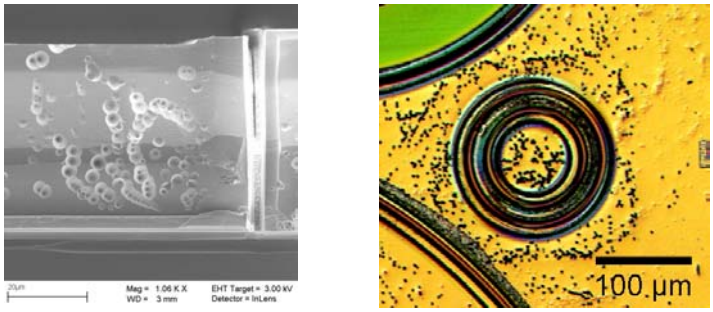


Figure 4.3: Defects at the surface of the wafer originating from slip dislocations.

close to the trench or buried oxide. The defects can be visualized by cleaving the wafer and etching it with an decorative etch solution (Secco etch [57]). The defects can be seen clearly in fig. 4.4(a). Even at the surface a huge amount of defects is visible (fig. 4.4(b)) after the decorative etch.



(a) (b)

Figure 4.4: Defects in the device layer and at the surface originating from slip dislocations.

We have performed stress simulations to investigate the formation of slip dislocations. The result was that the defect generation is avoided if we move the trench formation step to the end of the fabrication process. Fig. 4.5(a) shows two spots of high stress: at the top and at the bottom of the trench. The simulations of the new process (Fig. 4.5(b)) do not show the high stress region at the bottom at all and the stress at the top is clearly reduced.

Based on these simulations we have modified the process flow by moving the trench formation towards the end of the process:

- Arsenic implantation into the backside of the device layer and bonding

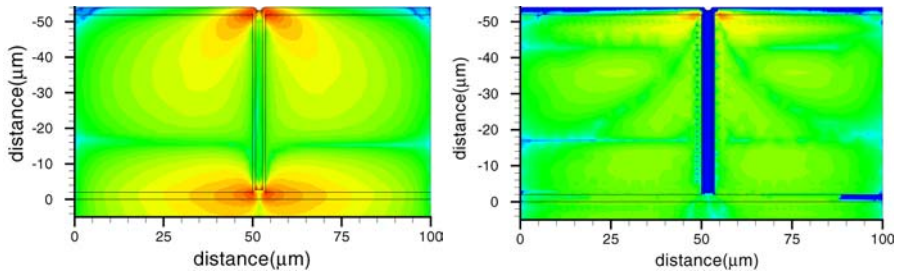


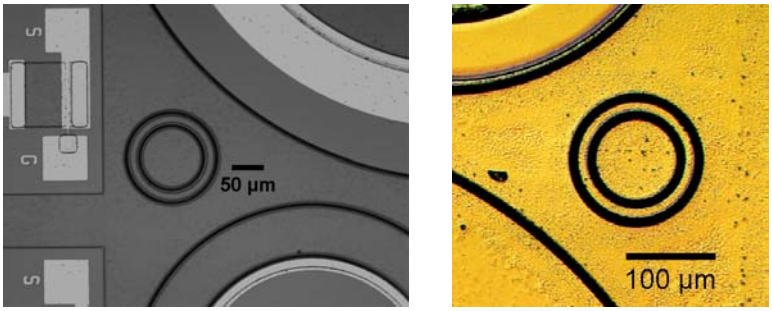
Figure 4.5: Stress simulations of the front-end and back-end trench formation process. a) High stress regions occur at the top and bottom of the trench. b) The stress is significantly reduced by moving the trench fabrication to the end of the process.

- Boron implantation of $2.8 \cdot 10^{12}$ cm^{-2} followed by a high temperature anneal (1200 °C, 15 h) to form the RESURF termination
- Gate oxide growth (500 Å)
- Polysilicon deposition and gate etch
- p-base implantation (boron, $6 \cdot 10^{13}$ cm^{-2}) and anneal (1100 °C, 120 min)
- Contact implantations
- Trench etching, phosphorous diffusion into the trench side-walls, CVD oxide deposition (0.8 µm), polysilicon deposition, CMP
- CVD oxide deposition and contact hole etch
- Metalization

The main advantage of this process is that the trenches are not exposed to the very high temperatures of the RESURF and p-base anneals. After the processing we could not see any slip lines at the surface, and even after the Secco etch the number of defects was very low (see fig. 4.6). The biggest part of the cross-section was defect-free (fig. 4.7(a)). But smaller structures (the structure shown in fig. 4.7(b) is roughly 120 µm wide compared to 800 µm of the structure aside) do show defects originating from the top corner of the trenches. But even in this case the high stress region at the bottom of the trenches disappeared.

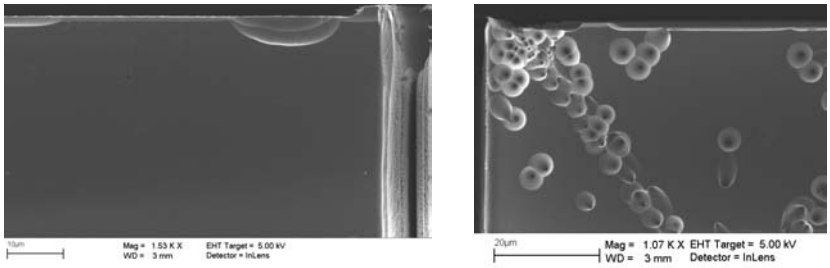
4.1.2 Trench Breakdown Characteristics

The purpose of the trenches is to block leakage currents between different parts of the chip and to withstand high voltages, applied to the power transistors during operation.



(a) (b)

Figure 4.6: Wafer surface after the back-end process. a) No slip lines are visible at the end of the process. b) Hardly any defects are visible after the Secco etch.



(a) (b)

Figure 4.7: Device layer of the back-end process. a) Large trench areas are defect free. b) Defects are created in small ($<$ 120 µm) trench areas.

We have measured the breakdown voltage of the trenches (see Paper I), but it turned out to be quite difficult to determine whether we are dealing with a surface effect or a bulk breakdown. Table 4.1 summarizes the measurements. The distance between trenches of the double and triple structures is 15 µm. We measured first the breakdown voltage of trenches covered only by silicon dioxide. The created defects indicated a surface breakdown. We then repeated the measurements with samples that had been covered with an additional layer (6 µm thick) of a polymer. We observed a substantial increase in the breakdown voltages in this case. The breakdown does still occur close to the surface and could be seen with a regular light microscope.

Table 4.1: Breakdown voltages (BV) of different 5 µm wide trench structures covered with silicon dioxide and silicon dioxide plus an additional polymer layer.

trenches covered with	BV of a single trench (V)	BV of a double trench (V)	BV of a triple trench (V)
silicon dioxide	440	590	730
silicon dioxide plus polymer	500	860	1150

4.1.3 Determination of the Channel Length

We have seen in chapter 2 on page 4 that the channel length of DMOS transistors is not defined by the mask layout, but by two consecutive diffusion steps. The channel length can be determined by process simulations, which are of course dependent on an accurate calibration of the simulator. Other methods used are destructive, like doping selective etching and scanning electron microscopy (SEM), and are difficult to apply in this context because of the low doping concentration of the p-base region. Recent methods, Scanning Capacitive Microscopy (SCM) [58] and Scanning Spreading Resistance Microscopy (SSRM) [59], developed for the characterization of sub-µm MOSFETs, are still destructive. We have developed a non-destructive, electrical method for the determination of the channel length of DMOS transistors (see Paper V). The method is based on capacitance-voltage measurements of the gate-source, gate-p-base, and gate-drain capacitances. The method has been verified for sub-µm LDMOS transistors with SCM data. We were able to determine the channel length of the vertical high-voltage transistors to 1.3 µm, which is in good agreement with process simulations.

4.2 Device Characteristics

Device simulations have been performed with the device simulators Atlas from Silvaco International and Dessis from ISE. Fig. 4.8(a) shows the potential distribution of a vertical DMOS on SOI with RESURF termination at an applied voltage of 515 V. The optimized p^- area modifies the surface field and leads to a uniform distribution of the potential. We have fabricated devices with three different RESURF doping profiles, i. e. uniform doping profile, step doping profile, and graded doping profile. They differ in their lateral extension, and have therefore an impact on the specific on-resistance (compare table 1 in Paper II). The simulated Direct Current (DC) characteristics is shown in fig. 4.8(b). The breakdown of the device occurs at above 500 V.

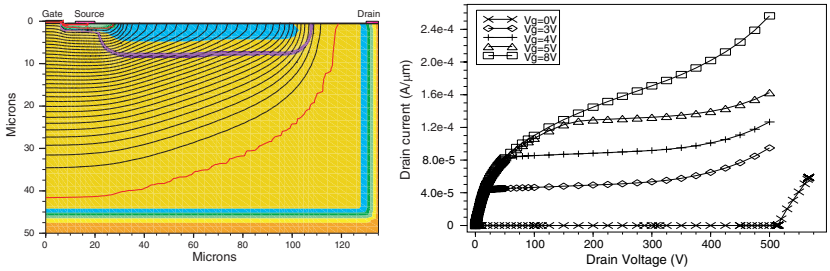


Figure 4.8: a) Uniform distribution of the potential lines due to an optimized RESURF termination. b) Simulated DC characteristics of a device with a breakdown voltage of 500V.

4.2.1 DC Characteristics

The measured IV-characteristics of a 30 mm device with a gate length of 12 µm is shown in fig. 4.9. The specific on-resistance is 0.17 $m\Omega cm^2$ and the breakdown voltage is 480 V. We have also measured the breakdown voltages of RESURF-n^- diodes. The breakdown of these devices occurs at 600 V. Thus, we can conclude that the breakdown of the transistors occurs at the curvature of the p-base.

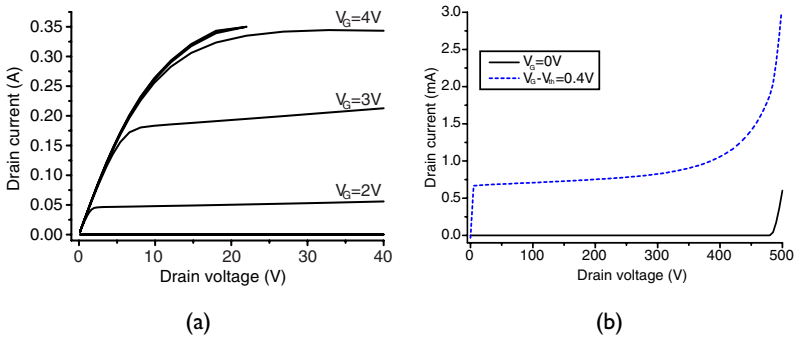


Figure 4.9: a) Measured IV-characteristics of a 30 mm wide device. b) Breakdown occurs at 480 V.

We can see from fig, 4.9 that the drain current of our devices does not saturate for higher gate voltages. This quasi-saturation behavior is caused by the saturation of the electron drift velocity in the drift region, which leads to a higher voltage drop in the drift region and lowers the potential at the drain end of the channel region [60]. A similar effect has been observed for LDMOS transistors [17]. This effect limits the current handling capability of our devices, and its dependency on the layout is

discussed in more detail in Paper II.

4.3 Modeling the On-Resistance

We have seen in fig. 2.2 on page 5 that the total resistance of a vertical DMOSFET consists of many different parts. In the case of a vertical DMOSFET on SOI we get additional resistive elements due to the buried n^+ layer and the highly doped trench sidewalls. These layers are necessary to create a low resistive current path from the drift region to the drain contact. Due to these highly doped layers the voltage drop of the current from a cell in the center of the device is not the same anymore as from a cell in the periphery because the current of a cell in the center of the device has to travel a longer distance to the drain contact than the current of a cell in the periphery of the device. This is different in the case of a conventional vertical DMOS transistor, where the voltage drop is the same for all cells.

The specific on-resistance of our devices has been modeled with a simple resistor model, shown in fig. 4.10. A detailed discussion of the model is presented in Paper VI. The model is based on the following assumptions, which have been confirmed by

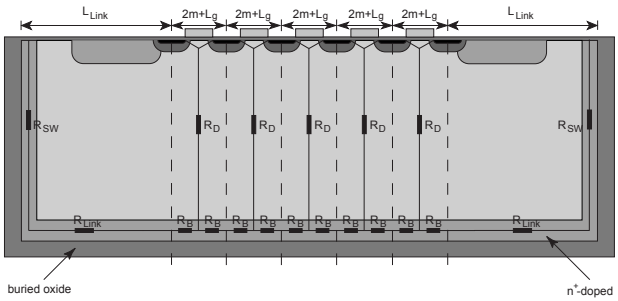


Figure 4.10: Simplified resistor model of a VDMOSFET on SOI.

device simulations: a) the overwhelming part of the voltage drop occurs in the drift region and b) the current spreads vertically down to the buried n^+ layer and is equally distributed between the different gate fingers.

An analytical expression for $R_{on,spec}$ can be derived:

$$R_{on,spec} = R_{n,tot} \cdot L_{tot} \tag{4.1}$$

with $R_{n,tot}$ and L_{tot} given by:

$$R_{n,tot} = (R_n + R_B + R_{Link} + R_{SW})/2 \tag{4.2}$$

$$L_{tot} = (2n+1) \cdot (2m + L_g) + 2 \cdot L_{Link} \tag{4.3}$$

where R_{SW}, R_B, and R_{Link} are resistive elements of the buried n^+ layers and the trench sidewalls. m, L_g, and L_{Link} are lengths shown in fig. 4.10. The on-resistance $R_{n,tot}$ can

be calculated with the help of a recursive formula based on the drift region resistance R_D and R_B:

$$\begin{aligned} R_0 &= 2R_D \\ R_1 &= \frac{(R_0+2R_B)\cdot R_D}{R_0+2R_B+R_D} \\ R_2 &= \frac{(R_1+2R_B)\cdot R_D}{R_1+2R_B+R_D} \\ &\vdots \\ R_n &= \frac{(R_{n-1}+2R_B)\cdot R_D}{R_{n-1}+2R_B+R_D} \end{aligned} \tag{4.4}$$

The specific on-resistance is plotted as a function of the number of cells in fig. 4.11. It can be seen that an optimum device size exists. After an initial fast decrease, $R_{on,spec}$ reaches its minimum and then increases again slowly. The increase after the minimum is based on a linear increase of the area with the number of cells (the total length increases by $2m+L_g$ for each new cell), and the fact that the on-resistance $R_{n,tot}$ approaches a constant value (This is in contrast to conventional VDMOSFETs, where $R_{n,tot}$ approaches zero). The resistor elements R_B, which are absent in conventional devices, are the reason for this behavior. The strong decrease of $R_{on,spec}$ for a small number of cells is due to the fact that more cells have to share the big termination area. The results of the analytical expression have been confirmed by numerical simulations,

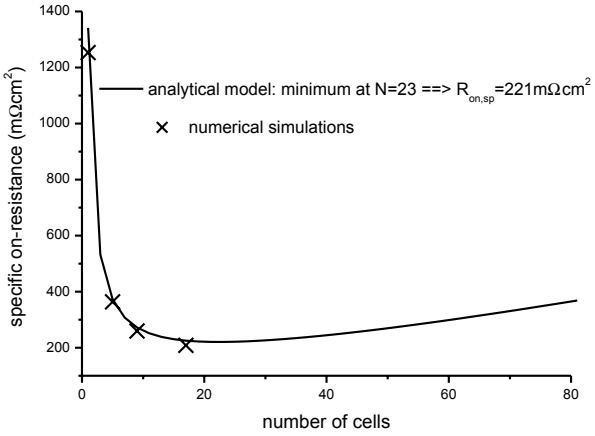


Figure 4.11: Specific on-resistance as function of the number of cells. The crosses are results from numerical device simulations.

also shown in fig. 4.11.

4.4 Capacitive Coupling

Considering fig. 4.1, it can be concluded that the buried oxide and the trench structures will significantly contribute to the drain capacitance of the DMOS transistor. This increased drain capacitance will induce displacement currents in the substrate and in the adjacent cells through the buried oxide capacitance and the trench capacitance resulting in cross-talk related noise. The capacitive coupling between neighboring trench isolated structures has been modeled in Paper VII. We have set up equivalent circuit models for single and double trench structures and have compared their results with simulated data. In the case of the double trench structure we have compared the model with measured data.

Fig. 4.12 shows the trench and double trench structures used for the simulations of the trench capacitances and the corresponding equivalent circuits. The buried oxide and the trenches have been treated as simple parallel plate capacitors, where the capacitance is given by $C = \varepsilon A/d$. The parameter values for the resistors are extracted by using the capacitance values calculated from the parallel plate case and a direct extraction method [61]. The results are shown in fig. 4.13(a), where the model is com-

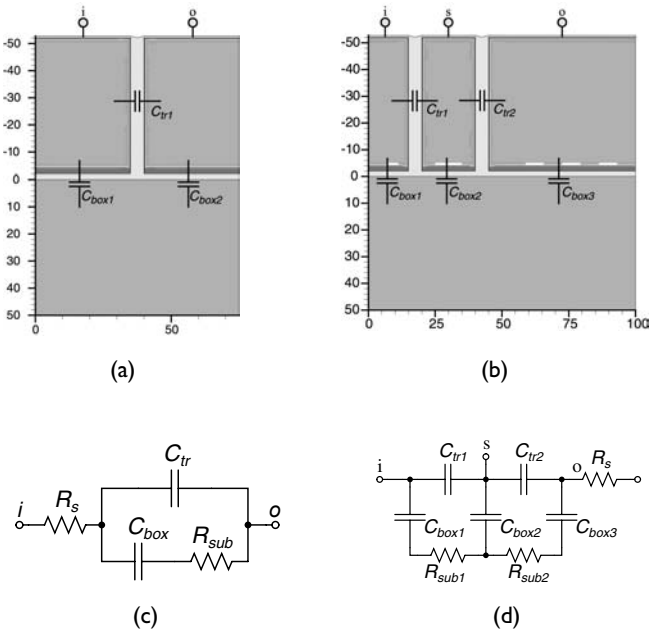
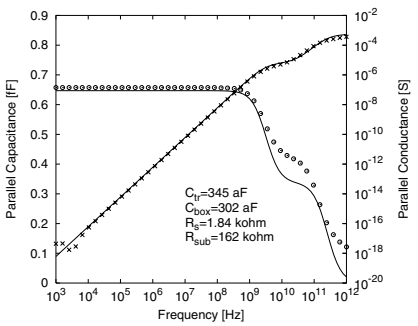


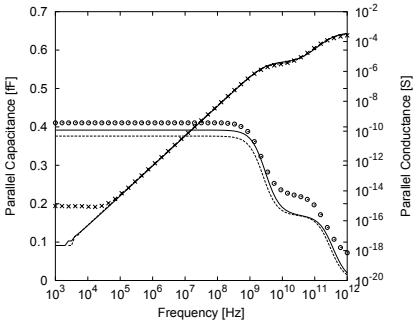
Figure 4.12: Single trench and double trench structures used for the simulations of the trench capacitances and the corresponding equivalent circuits.

pared to the simulated data. A good agreement between the model and the simulated data can be seen, especially for frequencies up to 1 GHz. The reduction of the capaci-

tance, at frequencies around 1 GHz and 100 GHz, is also predicted by the model. The



(a) Single trench model (—)



(b) Single trench model (- -) and double trench model (—)

Figure 4.13: Simulated capacitance (○) and conductance (×) of a) a single trench and b) a double trench structure.

coupling between neighboring cells can be reduced by using several trenches. The double trench structure of fig. 4.12(b) has been modeled with the simple model of the single trench case (fig. 4.12(c)) and with the extended model of fig. 4.12(d). The results are plotted in fig. 4.13(b). It can be concluded that the extended equivalent circuit provides an accurate description of all capacitances. The trench structures have been fabricated with the process described in section 4.1 on page 23. A top view of a double-trench structure with pads designed for 1-port *S*-parameter measurements is shown in fig. 4.14(a). The area between the trenches is floating, i.e. no 's' electrode is present. The capacitances are calculated using the parallel plate formula. The polysilicon in the trenches is treated as a conductive layer, i.e. only the oxide contributes to the capacitance. A very good agreement between the measured and modeled data can be observed in fig. 4.14(b).

4.5 Unclamped Inductive Switching

Many smart power applications require the switching of inductive loads. One example is the switching of injection valves in car engines [62]. Ruggedness and reliability are important characteristics of power devices in this context. Unclamped Inductive Switching (UIS) is a measure for the ability of a device to absorb a high level of energy prior to destructive breakdown. During an UIS test all the energy stored in an inductor is dumped directly into the device when it is turned off. During this test the device is simultaneously stressed by high current and high voltage, leading to a high power dissipation.

The setup of the UIS test is shown in fig. 4.15. The energy stored in the load inductor must be dissipated into the Device Under Test (DUT) since there is no freewheeling

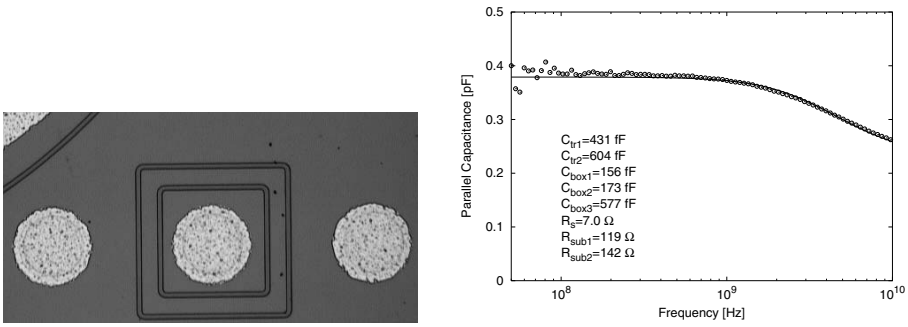


Figure 4.14: a) Top view of a double trench one-port test structure. b) Measured (○) and modeled (—) capacitance data of the test structure shown in a).

diode to discharge the inductor. The behavior of the vertical DMOSFET on SOI has been simulated with the mixed device and circuit simulator DESSIS. Only the thermal equilibrium of the device has been considered in the simulations without taking into account carrier and lattice temperature. The simulated UIS waveforms for the

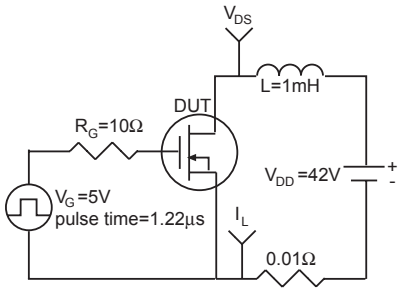


Figure 4.15: UIS circuit used for the mixed mode simulations.

parameter set of fig. 4.15 are shown in fig. 4.16.

It should be noted that in the case of our device peak voltage and peak current are separated in time. This result is unexpected and cannot be observed for bulk VDMOS transistors. This behavior is caused by the capacitor formed of the device layer, buried oxide, and substrate. This capacitor induces a second current path from the inductor to the ground as soon as the device is turned off. The energy stored in the inductor is partly released into the device and the other part is stored in the capacitor. The power dissipation of our device is compared with a similar device on bulk silicon in fig. 4.17. It can be seen that the power dissipated in the vertical DMOS on SOI is almost 50%

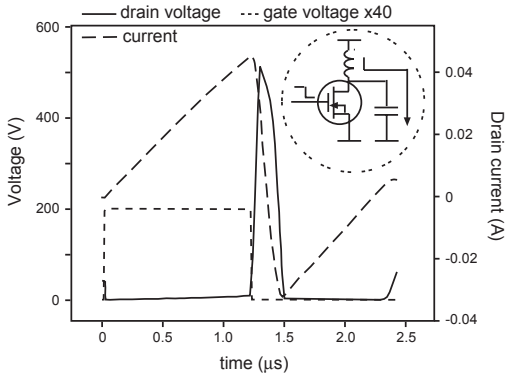


Figure 4.16: Simulated UIS waveforms for a VDMOSFET on SOI. The insert shows a second current path during the turn-off.

lower than that of a conventional device. A detailed discussion of this phenomenon is presented in Paper IV.

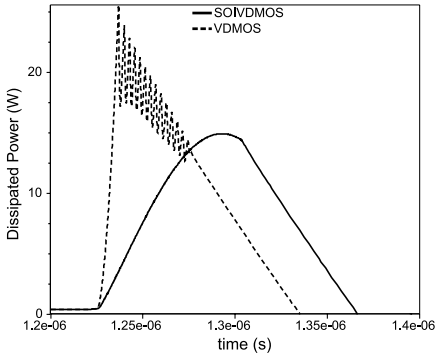


Figure 4.17: Power dissipation for a VDMOS on SOI and a bulk VDMOS. (The oscillations may indicate a numerical instability during the simulation.)

4.6 Self-Heating

Many applications require the operation of PICs at elevated temperatures. The operation temperature of electronic devices in automobiles, for example, is much higher than the conventional 125 °C [63]. The impact of high ambient temperatures is amplified by self-heating effects within the devices. BJTs, for example, can suffer from thermal runaway because the current increases with rising temperature [64]. In the case of MOSFET the output characteristics show a negative differential resistance, i. e. the

current decreases with increasing temperature [65]. Thermal effects in devices on SOI substrates with trench isolation are even more pronounced due to the low thermal conductivity of silicon dioxide.

The self-heating effects of vertical DMOSFET on SOI are presented in Paper III. The IV-characteristics[1] of simulations with and without the drift-diffusion model, which is necessary for the simulation of self-heating, are compared in fig. 4.18. The expected negative differential resistance is seen in fig. 4.18(b). The current decreases for a given gate voltage with rising drain voltage because of mobility degradation in the channel. Fig. 4.19 shows the drain current for V_G=5 V at different tempera-

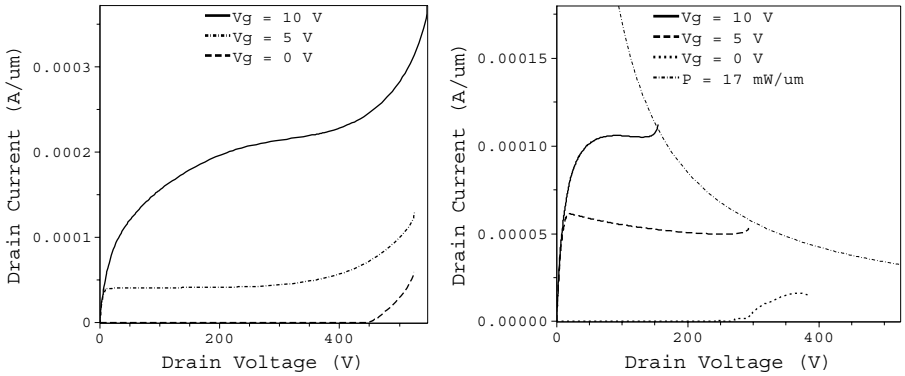


Figure 4.18: IV-characteristic simulated a) without self-heating and b) with self-heating.

tures. The on-resistance consists of different parts as we have seen in section 2.5.2 on page 12. The positive temperature coefficient of the mobility leads to an increase in on-resistance at higher temperatures [66]. In addition to the increasing on-resistance a snapback can be seen in the same figure. The simulations show that the snapback occurs at a constant power of 17 $^{W}/_{\mu m}$. The devices' breakdown voltage decreases significantly when the ambient temperature is raised from room temperature to 100 °C because as the junction temperature rises the temperature difference between the ambient temperature and the critical temperature gets smaller. Thus, the power required to reach the critical temperature is reduced. This behavior has been observed in bulk LDMOS transistors as well [67]. The pronounced self-heating effects have not been verified by our measurements. The IV-characteristics of our devices do not show the negative differential resistance, as can be seen in fig. 4.9. We could, however, observe a snapback similar to that of the simulations. We have not been able yet to identify the reason for the discrepancy between measurements and simulations. The decrease in threshold voltage, which occurs when the temperature rises, is normally compen-

[1]The figures got mixed up in Paper III: fig. 4.18(b) is shown twice and fig. 4.18(a) is missing.

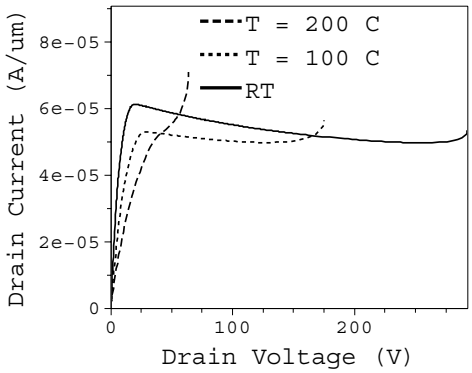


Figure 4.19: IV characteristics at different temperatures for a gate voltage of 5 V.

sated by an increasing channel resistance. But a parasitic hole current in the p-base of our devices would raise the p-base potential resulting in an additional decrease of the threshold voltage. Another reason could be that the simplified structure used in the simulations does not represent our devices accurately. In the simulations a structure with only one gate finger is used in order to reduce the number of grid points. It is possible that this simplification is not sufficient to approximate the mesh structure of our devices.

CHAPTER 5

CONCLUSIONS

Within the framework of this thesis the integration of vertical DMOS transistors on SOI and CMOS devices has been demonstrated. We have manufactured fully functional transistors with a breakdown voltage of 480V and diodes with a breakdown voltage of 600V.

The defect generation has been reduced significantly by a new process with back-end trench formation. This new process has been developed in order to reduce the number of defects created after the trench formation. This has been achieved by moving the trench formation steps towards the end of the process such that the trenches are not exposed to high temperatures.

An analytical model has been developed for the specific on-resistance of vertical high-voltage DMOS transistors on SOI substrates. The model accurately predicts the dependency of the specific on-resistance on the device size. In addition, it is shown that a minimal specific on-resistance is achieved for an optimal device size. The model has been verified through comparison with 2D numerical device simulations.

Capacitive coupling between trench-isolated structures on SOI substrates has been modeled by equivalent circuits consisting of capacitive and resistive elements. The models have been used successfully to describe the frequency behavior of single and double trench structures. The comparison with numerical simulations and measured data shows that the models have good accuracy in a wide frequency range. Furthermore, it has been shown that calculated capacitance values, which are based on the simple parallel plate capacitor formula, are sufficient to obtain a high accuracy.

Unclamped Inductive Switching simulations have shown that the power dissipated in our device is almost 50% lower than that in a conventional DMOSFET. This unexpected result is based on a capacitor that consists of device layer, buried oxide, and substrate. This capacitor induces a second current path from the inductor to the ground as soon as the device is turned off. The energy stored in the load inductor is released partly into the device, while the other part is stored in the capacitor.

Self-heating simulations have been performed and they show the expected impact of the higher temperatures on the on-resistance, saturation current, and breakdown.

So, what's left?

The results of the UIS test have not been verified yet. We have problems with bonding and packaging the devices, and "on chip" switching measurements are not possible.

The fact that our devices do not show a pronounced self-heating effect has to be investigated in more detail. It has to be clarified if the device suffers from parasitic transistor action. The problems with the simulations are based on the huge size of our structures. We are dealing with a tradeoff because we have to reduce the number of nodes without losing accuracy.

Furthermore, the functionality of the concept has to be proven within a real circuit application. We have only demonstrated the integration with a CMOS compatible process.

APPENDIX A

LIST OF ACRONYMS

AC Alternating Current

BCD Bipolar-Complementary Metal Oxide Semiconductor-Double Diffused Metal Oxide Semiconductor

BJT Bipolar Junction Transistor

BOX Buried Oxide

CMOS Complementary Metal Oxide Semiconductor

CMP Chemical-Mechanical Polishing

CVD Chemical Vapor Deposition

DC Direct Current

DI Dielectric Isolation

DMOS Double Diffused Metal Oxide Semiconductor

DUT Device Under Test

ECR Electron Cyclotron Resonance

EMI Electromagnetic Interference

EMV Electromechanical Valve

FET Field Effect Transistor

IC Integrated Circuit

ICP Inductively Coupled Plasma

IGBT Isolated Gate Bipolar Transistor

JFET Junction Field Effect Transistor

JI Junction Isolation

LDMOS Lateral Double Diffused Metal Oxide Semiconductor

LIGBT Lateral Isolated Gate Bipolar Transistor

MOS Metal Oxide Semiconductor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

PIC Power Integrated Circuit

RIE Reactive Ion Etching

RESURF Reduced Surface Field

RF Radio Frequency

SCM Scanning Capacitive Microscopy

SIMOX Separation by Implantation of Oxygen

SLIC Subscriber Line Interface Circuit

SoC System on Chip

SOI Silicon-on-Insulator

SOS Silicon-on-Sapphire

SSF Swedish Foundation for Strategic Research

SSRM Scanning Spreading Resistance Microscopy

UIS Unclamped Inductive Switching

VDMOS Vertical Double Diffused Metal Oxide Semiconductor

VLSI Very Large Scale Integration

BIBLIOGRAPHY

[1] G. E. Moore, “Cramming More Components onto Integrated Circuits,” *Electronics*, vol. 38, April 1965.

[2] C. Contiero, A. Andreini, and P. Galbiati, “Roadmap Differentiation and Emerging Trends in BCD Technology,” *Proc. ESSDERC*, pp. 275–282, 2002.

[3] J. C. Erskine et al., “High Temperature Automotive Electronics: An Overview,” *Trans. 3rd Intl. High-Temperature Electronics Conference*, vol. 1, pp. XIII–21–XIII–31, June 1996.

[4] J. G. Kassakian and D. J. Perreault, “The Future of Electronics in Automobiles,” *Proc. ISPSD*, pp. 15–19, 2001.

[5] M. Lenz, “Systems on Silicon for the System Automobile,” *Components*, no. 1, pp. 17–20, 1999, Siemens AG.

[6] J. König, “Benzin sparen - auf Nockenwelle verzichten,” *http://idw-online.de/public/pmid-14030/zeige˙pm.html*, 1999.

[7] M. A. Tamor, “High-Temperature Electronics for Automobiles,” in *High-Temperature Electronics*, R. Kirschman, Ed. IEEE Press, 1998, pp. 153–160.

[8] D. Flandre, “Silicon-on-Insulator Technology for High Temperature Metal Oxide Semiconductor Devices and Circuits,” *Materials and Science Engineering*, vol. B29, no. 1-3, pp. 7–12, January 1995.

[9] S. Krishna, J. Kuo, and I. S. Gaeta, “An Analog Technology Integrates Bipolar, CMOS, and High-Voltage DMOS Transistors,” *IEEE Trans. on Electron Devices*, vol. ED-31, no. 1, pp. 89–95, Jan. 1984.

[10] A. Andreini, C. Contiero, and P. Galibiati, “A new Integrated Silicon Gate Technology Combining Bipolar Linear, CMOS Logic, and DMOS Power Parts,” *IEEE Trans. Electron Devices*, vol. ED-33, no. 12, pp. 2025–2030, Dec. 1986.

[11] B. Murari, “Smart Power Technology and the Evolution from Protective Umbrella to Complete System,” *IEDM Tech. Dig.* , pp. 9–15, 1995.

[12] R. S. Wrathall, “The Design of a High Power Solid State Automotive Switch in CMOS-VDMOS Technology,” *IEEE 16th Power Electronics Specialists Conf.*, pp. 229–231, 1985.

[13] Y. Tarui, Y. Hayashi, and T. Sekigawa, "Diffusion self-aligned MOST: a new approach for high speed device," *Proc. 1st Conf. on Solid State Devices*, 1969.

[14] H. Sigg et al., "DMOS Transistor for Microwave Applications," *IEEE Trans. Electron Devices*, vol. ED-19, pp. 45–53, 1972.

[15] M. Chang et al., "Lateral HV-IC with 1200V Bipolar and Field-Effect Devices," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 1992–2001, 1986.

[16] A. W. Ludikhuize, "A Versatile 700-1200V IC Process for Analog and Switching Applications," *IEEE Trans. Electron Devices*, vol. ED-38, no. 7, pp. 1582–1589, July 1991.

[17] J. Olsson et al., "1 W/mm RF power density at 3.2 GHz for a dual-layer RESURF LDMOS transistor," *IEEE Electron Device Lett.*, vol. EDL-23, no. 4, pp. 206–208, April 2001.

[18] L. Vestling, J. Olsson, and K. H. Eklund, "Drift Region Optimization of Lateral RESURF devices," *Solid-State Electronics*, vol. 46, pp. 1177–1184, 2002.

[19] L. Vestling, "Design and Modeling of High-Frequency LDMOS Transistors," Ph.D. dissertation, Uppsala Universitet, Sweden, 2002.

[20] B. J. Baliga et al., "The Insulated Gate Transistor: A New Three-Terminal MOS-Controlled Bipolar Power Device," *IEEE Trans. Electron Devices*, vol. ED-31, no. 6, pp. 821–828, 1984.

[21] M. N. Darwish and M. A. Shibib, "Lateral MOS-Gated Power Devices - A Unified View," *IEEE Transactions on Electron Devices*, vol. ED-38, no. 7, pp. 1600–1604, 1991.

[22] M. Stoisiek et al., "A Dielectric Isolated High-Voltage IC-Technology for Off-Line Applications," *Proc. 7th ISPSD*, pp. 325–329, 1995.

[23] K. -G. Oppermann and M. Stoisiek, "Optimization of LIGBTs in a Dielectric Insulated IC-Technology Using a "Switched Anode"," *Proc 8th ISPSD*, pp. 239–242, 1996.

[24] T. Fujihira, "Theory of Semiconductor SuperJunction Devices," *Jpn. J. Appl. Phys.*, vol. 36, no. 10, pp. 6254–6262, Oct. 1997.

[25] G. Deboy, "A New Generation of High Voltage MOSFETs Breaks the Limit Line of Silicon," *IEEE IEDM Tech. Dig.*, pp. 683–685, 1998.

[26] T. Fujihira and Y. Miyasaka, "Simulated Superior Performance of Semiconductor Superjunction Devices," *Proc. 10th ISPSD*, pp. 423–426, 1998, p292.pdf.

[27] L. Lorenz et al., "COOLMOS^{TM} - a new Milestone in High Voltage Power MOS," *Proc. 11th ISPSD*, pp. 3–10, 1999.

[28] F. Udrea, A. Popescu, and W. I. Milne, "A New Class of Lateral Power Devices for HVIC's Based on the 3D RESURF Concept," *Proc. IEEE BCTM*, pp. 187–190, 1998.

[29] ——, "3D RESURF Double-Gate MOSFET: A Revolutionary Power Device Concept," *Electronics Letters*, vol. 34, no. 8, pp. 808–809, 1998.

[30] B. J. Baliga, *Power Semiconductor Devices*. Boston: PWS Publishing Company, 1996.

[31] B. J. Baliga and S. K. Ghandhi, "Analytical Solutions for the Breakdown Voltage of Abrupt Cylindrical and Spherical Junctions," *Solid-State Electronics*, vol. 19, no. 9, pp. 739–744, 1976.

[32] W. Fulop, "Calculation of Avalanche Breakdown of Si p-n Junctions," *Solid-State Electronics*, vol. 10, pp. 39–43, 1967.

[33] A. S. Grove, O. Leistiko, and W. W. Hooper, "Effect of Surface Fields on the Breakdown Voltage of Planar Silicon p-n Junctions," *IEEE Trans. Electron Devices*, vol. 14, no. 3, pp. 157–162, Mar. 1967.

[34] D. A. Grant and J. Gowar, *Power MOSFETs*. New York: Wiley-Interscience, 1989.

[35] C. Hu, "Optimum Doping Profile for Minimum Ohmic Resistance and High Breakdown Voltage," *IEEE Trans. Electron Devices*, vol. ED-26, no. 3, pp. 243–244, 1979.

[36] G. Charitat, "Voltage Handling Capability and Termination Techniques of Silicon Power Semiconductor Devices," *IEEE BCTM Conf. Proc.*, pp. 175–183, 2001, p288.pdf.

[37] F. Conti and M. Conti, "Surface Breakdown in Silicon Planar Diodes Equipped with Field Plate," *Solid-State Electronics*, vol. 15, pp. 93–105, 1972.

[38] J. A. Appels and H. M. J. Vaes, "High Voltage Thin Layer Devices (RESURF Devices)," *IEEE IEDM Tech. Dig.*, pp. 238–241, 1979.

[39] R. Sunkavalli, A. Tamba, and B. J. Baliga, "Step Drift Doping Profile for High Voltage DI Lateral Power Devices," in *Proc. IEEE Int. SOI Conf.*, 1995, pp. 139–140.

[40] R. Stengl et al., "Variation of Lateral Doping as a Field Terminator for High-Voltage Power Devices," *IEEE Trans. Electron Devices*, vol. ED-33, no. 3, pp. 426–428, March 1986.

[41] C. Harendt et al., "Bonded-Wafer SOI Smart Power Circuits in Automotive Applications," *2nd Int. Symp. Semiconductor Wafer Bonding*, pp. 129–143, 1993.

[42] A. Plößl and G. Kräuter, "Silicon-on-Insulator: Materials Aspects and Applications," *Solid-State Electronics*, vol. 2000, no. 44, pp. 775–782, 2000.

[43] K. Mera, H. Tomita, and K. Tokiguchi, "High Current Ion Implanter for 300 mm SIMOX Wafer Production," *Hitachi Review*, vol. 51, no. 4, pp. 113–117, Oct. 2002.

[44] M. Bruel, "Silicon on Insulator Material Technology," *Electronics Letters*, vol. 31, no. 14, pp. 1201–1202, 1995.

[45] M. Ito et al., "Scalability Potential in ELTRAN SOI-Epi Wafer," *Proc. IEEE Int. SOI Conf.*, pp. 10–11, 2000.

[46] J. B. Lasky, "Wafer Bonding for Silicon-on-Insulator Technologies," *Appl. Phys. Lett.*, vol. 48, pp. 78–80, Jan. 1986.

[47] J. W. Coburn and H. F. Winters, "Ion- and Electron-Assisted Gas-Surface Chemistry – An Important Effect in Plasma Etching," *J. Appl. Phys.*, vol. 50, pp. 3189–3196, 1979.

[48] H. Morioka, D. Matsunaga, and H. Yagi, "Suppression of Notching by Lowering the Bias Frequency in Electron Cyclotron Plasma with a Divergent Magnetic Field," *J. Vac. Sci. Technol. A*, vol. 16, no. 3, pp. 1588–1593, May/June 1998.

[49] C. Gormley et al., "State of the Art Deep Silicon Anisotropic Etching on Silicon-On-Insulator Bonded Substrates for Dielectric Isolation and MEMS Applications," in *5th International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications*. Electrochemical Society, 1999, abstract No. 1020.

[50] F. Lärmer et al., "Method of Anisotropically Etching Silicon," *United States Patent*, vol. Patent Number 5,501,893, March 1996.

[51] ——, "Bosch Deep Silicon Etching: Improving Uniformity and Etch Rate for Advanced MEMS Applications," *Proc. IEEE 12th Int. Workshop on MEMS*, pp. 211–216, 1999.

[52] J. Bhardwaj, H. Ashraf, and A. McQuarrie, "Dry silicon etching for MEMS," *Proc. Symposium on Microstructures and Microfabricated Systems*, 1997.

[53] S. A. McAuley et al., "Silicon micromachining using a high-density plasma source," *J. Phys. D: Appl. Phys.*, vol. 34, pp. 2769–2774, 2001.

[54] M. A. Vyvoda, M. Li, and D. B. Graves, "Hardmask Charging During Cl_2 Plasma Etching of Silicon," *J. Vac. Sci. Technol. A*, vol. 17, no. 6, pp. 3293–3307, Nov./Dec. 1999.

[55] W. A. Nevin et al., "Materials Defects on Stress-Induced Defect Generation in Trenched Silicon-on-Insulator Structures," *J. Electrochem. Soc.*, vol. 148, no. 11, pp. G649–G654, 2001.

[56] S. Matsuda et al., "Three–Dimensional Mechanical Stress Analysis of Trench Isolation along {111} Gliding Planes," *IEEE IEDM Tech. Dig.*, pp. 885–888, 1994.

[57] J. P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Norwell: Kluwer Academic Publishers, 1997.

[58] W. Timp et al., "Two-Dimensional Dopant Profiling of a 60nm Gate Length nMOSFET Using Scanning Capacitance Microscopy," *IEEE IEDM Tech. Dig.*, pp. 555–558, 1998.

[59] P. de Wolf et al., "Direct Measurement of L_{eff} and Channel Profile in MOSFETs Using 2-D Carrier Profiling Techniques," *IEEE IEDM Tech. Dig.*, pp. 559–562, 1998.

[60] C. H. Kreuzer, N. Krische, and P. Nance, "Physical Based Description of Quasi-Saturation Region of Vertical DMOS Power Transistors," *IEEE IEDM Tech. Dig.*, p. 18.7, 1996.

[61] L. Vestling and J. Ankarcrona, "A General Small Signal Series Impedances Extraction Technique," *IEEE Microwave and Wireless Components Lett.*, vol. 12, pp. 249–251, 2002.

[62] R. Constapel, "Unclamped inductive switching of integrated quasi-vertical DMOSFETs," *Proc. 8th ISPSD*, pp. 219–222, 1996.

[63] M. Hattori, "Needs and Applications of High Temperature LSIs for Automotive Electronic Systems," *Proc. 3rd Europ. Conf. on High Temperature Electronics*, pp. 37–43, 1999.

[64] J. Olsson, "Self-heating effects in SOI Bipolar Devices," *Microelectronics Engineering*, vol. 56, pp. 339–351, 2001.

[65] L. J. McDaid et al., "Physical Origin of Negative Differential Resistance in SOI Transistors," *Electronics Letters*, vol. 25, no. 13, pp. 827–828, June 1989.

[66] G. M. Dolny, G. E. Nostrand, and K. E. Hill, "The Effect of Temperature on Lateral DMOS Transistors in a Power IC Technology," *IEEE Trans. on Electron Devices*, vol. 39, no. 4, pp. 990–995, April 1992.

[67] Y. S. Chung and B. Baird, "Electrical-thermal coupling mechanism on operating limit of LDMOS transistor," *Tech. Dig. IEDM*, pp. 4.4.1–4.4.4, 2000.