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Band Gap Profiling and High Speed Deposition of $Cu(In,Ga)Se_2$ for Thin Film Solar Cells

BY

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Abstract

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The $Cu(In,Ga)Se_2$-based thin film solar cell is a promising candidate for becoming one of the more important solar cell technologies in the near future. In order to realize such a development a significant reduced production cost of the $Cu(In,Ga)Se_2$ (CIGS) layer is needed. This work shows a possible way towards such a reduction by increasing the deposition rate and decreasing the CIGS thickness with almost maintained device efficiency.

Obtaining an improved device performance in CIGS-based solar cells by using an in-depth variation of the band gap has earlier been investigated without any clear conclusions. In this work an extensive experimental study of the beneficial effect of band gap profiling has been performed and firmly based conclusions have been made. For standard CIGS devices the band gap profiling can result in an improved efficiency of around 0.4 % units. This gain is related to improved field-assisted carrier collection. For reduced CIGS thicknesses the importance of a band gap profiling is enhanced, and at a CIGS thickness of 0.5 μm an efficiency gain of 2.5 % units is obtained, resulting in a 13.4 % efficient device. The main reason for the gain is passivation of the back contact, which becomes increasingly detrimental for the device performance as the CIGS thickness is reduced. With an optimized band gap profile the CIGS thickness can be reduced 3-4 times, with almost solely absorption related losses.

The potential for increasing the deposition rate of co-evaporated CIGS layers is shown to be large. An increase of up to 10 times compared to commonly used deposition rates is possible with only minor losses in efficiency. By using band gap profiled thin CIGS layers deposited at high rates, the production from a single evaporation system can be increased up 30 times. Such an increase will lead to the needed reduction of the production cost of the complete solar cell module.

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Publications

This thesis is based on the following publications, which will be referred to in the text by their Roman numerals.

I J. Kessler, J. Norling, O. Lundberg, J. Wennerberg, and L. Stolt. *Optimization of RF-sputtered ZnO/ZnO:Al for Cu(In,Ga)Se_2 based devices*, in proceedings 16th European Photovoltaic Solar Energy Conference (2000) p. 775 - 778

II M. Bodegård, O. Lundberg, J. Malmström, L. Stolt, and A. Rockett. *High voltage Cu(In,Ga)Se_2 devices with Ga-profiling fabricated using co-evaporation*, in Proceedings of 28th IEEE Photovoltaic Specialists Conference (2000) p. 430-433

III T. Dullweber, O. Lundberg, J. Malmström, M. Bodegård, L. Stolt, U. Rau, H.W. Schock, and J.H. Werner, *Back surface band gap gradings in Cu(In,Ga)Se_2 solar cells*, Thin Solid Films **387** (2001) p. 11-13

IV O. Lundberg, M. Bodegård, J. Malmström, and L. Stolt, *Influence of the Cu(In.Ga)Se_2 thickness and Ga-grading on the solar cell performance*, Progress in Photovoltaics **11** (2003) p. 77-88

V O. Lundberg, M. Bodegård, and L. Stolt, *Rapid growth of thin Cu(In,Ga)Se_2 layers for solar cells*, Thin Solid Films **431-432** (2003) p. 26-30

VI M. Bodegård, O. Lundberg, J. Lu, and L. Stolt, *Re-crystallisation and interdiffusion in CGS/CIS bilayers*, Thin Solid Films **431-432** (2003) p. 46-52

VII O. Lundberg, J. Lu, A. Rockett, M. Edoff, and L. Stolt, *Diffusion of indium and gallium in Cu(In,Ga)Se_2 thin film solar cells*, Journal of physics and chemistry of solids **64** (2003) p. 1499-1504

VIII O. Lundberg, M. Edoff, and L. Stolt. *Optimized growth conditions for Cu(In,Ga)Se_2 layers grown by co-evaporation at high deposition rate*, to appear in Material research society symposium proceedings (2003)

IX J. Malmström, O. Lundberg, and L. Stolt. *Potential for light trapping in Cu(In,Ga)Se_2 solar cells*, to appear in proceedings of 3rd World Conference on Photovoltaic Solar Energy Conversion (2003)

Contents

1. Introduction

1.1 Sustainable energy

One of the major environmental concerns of today is the emission of greenhouse gases like CO_2. Climate scientists expect that the average global surface temperature could rise 0.6-2.5°C in the next fifty years, and 1.4-5.8°C in the next century, due to this emission.[1] Such an increase will have huge impact on our environment. In order to avoid an even further rise of the temperature, we have to stop exhaust greenhouse gases in the quantities we do today. The reason for the large amount of greenhouse gases emitted into the atmosphere is that nearly 80 % of the energy generation worldwide originates from fossil fuels. In the long term there are three main alternatives to reduce the CO_2 emissions, without reducing the global energy consumption:

- **Nuclear power** – today we have around 400 nuclear power plants around the world. With about 5000 the energy-demand of today could be covered.
- **Carbon sequestration**– we could continue to use our reserves of fossil fuels if we take care of the emissions and store them in existing cavities in the earth.
- **Sustainable energy** – by a massive effort in developing existing and new technologies for sustainable energy generation, we can generate all the energy needed with these technologies.

The first alternative is not very tempting from a risk point of view. It is also a time limited solution since the amount of uranium is finite. The second alternative might be possible but is no sustainable solution. The concept of carbon sequestration is also not tested in large scale and it is not for certain that it will work. If sustainable energy solutions could replace the existing non-sustainable energy generating technologies, it would in the long term be to the benefit of us all – but is it realistic? The irradiation from the sun, reaching our globe is in relation to our energy demand, very high (in the order of 10 000 times higher). With solar cells this irradiation can, with no material consumption, directly be converted into the highest form of energy – electricity!

1.2 Solar cells

The principal function of a solar cell is rather simple. When a solar cell is put under illumination, the back and front side is charged differently, and the solar cell becomes a “battery”. The origin of this effect is caused by two basic mechanisms. Electrons in the solar cell *absorb* the incoming light and are thereby elevated to a higher energy level. As the electrons are transferred to this level, they leave an oppositely charged “hole” behind. An electric field built in to the solar cell *separate* these oppositely charged “particles” by pushing them in different directions. This leads to the oppositely charged front and backside of the solar cell. By connecting a load between back and front contact an electric current will flow through the load as long as the solar cell is kept under illumination. With this

current electrons are also brought back to the solar cell, now at the lower energy level and the process can start over again. See further Chapter 2.3.

1.2.1 History

The Photovoltaic effect was first reported in 1839 by the French physicist Edmond Bequerel. By accident he exposed two metal plates in a conductive fluid to the sunlight and observed a small voltage. Still it would take another 50 years before the first solar cell was developed. In 1886 the American Charles Fritts fabricated a solar cell, based on the photosensitive material selenium. It had an efficiency of less than 1 %, but it was a solar cell converting sunlight into electricity. In the 1950s the foundation of the modern solar cell technology was developed at Bell Laboratories, USA. More or less by chance an employed scientist, Gerald Pearson, put a silicon wafer doped with impurities under a lamp and measured a relatively high current. A few months later a silicon solar cell with a conversion efficiency of 6 % was presented.[2] A rapid development followed in the coming years and by 1960 efficiencies as high as 14 % was reported. In recent years single crystalline silicon solar cells with efficiencies up to 24 % have been fabricated in research laboratories.[3] The first larger application for silicon solar cells was in the space technology but not until the oil crisis in 1973 any significant interest in using solar cells for large-scale power production was seen. Since the beginning of the 1990s the yearly growth of the solar cell market has been 20-40 %, and in 2002 the cumulative installed capacity exceeded 1 GW_p- roughly corresponding to one nuclear reactor.[4] (A nuclear power plant commonly has a few reactors, c.f. Chapter 1.1)

1.2.2 Crystalline silicon solar cells

Over 90 % of the solar cell modules sold today are based on crystalline or polycrystalline silicon (Si). A number of reasons have lead to this great success for crystalline Si solar cells. High performance and good long-term stability are maybe the most important ones. Also the huge available amounts of Si, which comprise around 20 % of the earth crust, are to the benefit of this technology. However, crystalline silicon solar cells also have disadvantages, which result in a ten times higher cost for the generated electricity as compared to conventional electricity generation technologies. This is mainly due to a very high energy demand for purifying SiO_2 to Si, which in combination with a low material yield during fabrication leads to a high production cost. In the fabrication of crystalline Si solar cells, a so called wafer technology is used, which means that individual solar cells, made from Si wafers, need to be soldered together to form a solar cell module. This adds complexity to the production process and thereby increases the production costs further.

1.2.3 Thin film solar cells

As the name hints, thin film solar cells are normally composed of several thin films, with thicknesses in the order of 10 μm or less, deposited onto a low cost substrate. One advantage with this technology is that a complete, large area, solar cell module can be fabricated in “one piece” (so called monolithic integration). In combination with the low amounts of active material needed, the production cost of thin film solar cells can potentially be significantly lower, compared to crystalline Si solar cells. The development of thin film solar cells started in the

1970s and almost since it has been said "within 5 years the thin film technology will take over the solar cell market". The fact is that in 2002, thin film solar cells still had less than 10 % of the solar cell market.[4] One major disadvantage with thin film solar cells is that the efficiencies obtained not are as high as for crystalline silicon solar cells. Three thin film technologies are to date candidates for large-scale production. These are based on amorphous silicon (a-Si), cadmium telluride (CdTe) and copper indium gallium diselenide $Cu(In,Ga)Se_2$ (CIGS). In for example pocket calculators, a-Si solar cells have been used for many years. For power generation, this type of technology has the disadvantage of having a lower efficiency compared to the other two thin film technologies. Despite this, a-Si is the clearly dominating thin film technology today. The industrial activity for CdTe-based thin film solar cells was relatively high until 2002. However, during this year many of the industrial activities were closed. Besides technical problems a major reason for this is a lack of market acceptance related to the relatively large amounts of the toxic element Cd included in these devices. Cu(In,Ga)Se2-based solar cells is the thin film technology that results in the highest conversion efficiency[5] and is still by many seen as the most promising solar cell technology for the near future.

2 Cu(In,Ga)Se_2-based thin film solar cells

First to use $CuInSe_2$ (CIS) as a photovoltaic material were Wagner and co-workers, who in 1973 fabricated a solar cell device with a single crystalline $CuInSe_2$ absorber, which had an efficiency of 12 %.[6] During the early 1980s, Boeing Corporation made large progress in the development of thin film polycrystalline Cu(In,Ga)Se_2 (CIGS) solar cells. Efficiencies above 10 % were achieved using a three-sources co-evaporation process.[7] In 1987 ARCO fabricated a CIS based solar cell with an efficiency of 14.1 %, which became a long lasting record for thin film solar cells.[8] ARCO used a different approach for absorber preparation, namely selenization of stacked metal layers by H_2Se. The highest conversion efficiency, until today obtained for CIGS based thin film solar cells, is 19.2 %, achieved by the research group at NREL.[9] In this device the CIGS layer was fabricated by co-evaporation. The currently most efficient thin film solar cell module has been fabricated at Uppsala University. The 19 cm^2 large module reached an efficiency of 16.6 %.[10] In the book chapters by Rau and Schock[11] and by Shafarman and Stolt[12] good reviews of CIGS based thin film solar cells are given. In the following a short description of the device structure, with focus on the CIGS layer, will be presented together with a brief explanation of the device operation. In the last part of this chapter our experimental procedure of fabricating and characterizing devices is described.

2.1 Device structure

In Figure 2.1 a sketch of the state-of-the-art Cu(In,Ga)Se_2-based thin film solar cell structure is shown. The structure consists of five thin layers deposited on a substrate. In the following the used materials, in this structure, will be motivated.

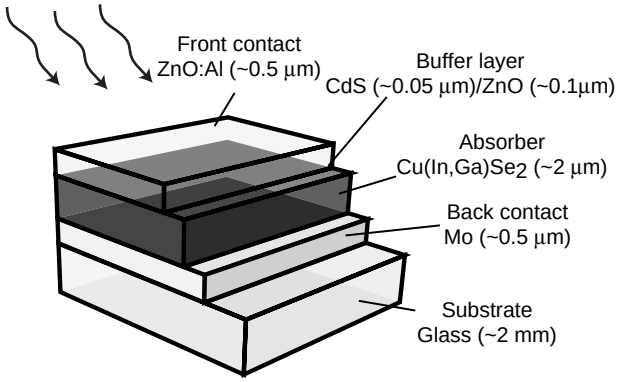


Figure 2.1. Outline of a CIGS based thin film solar cell structure.

Substrate: In the early 1990s a large improvement of the device performance was observed when the commonly used sodium-free substrates, alumina (Al_2O_3) or Corning® 7059 glass, were replaced by soda-lime glass. First the improvement was believed to originate from a better match of thermal expansion coefficients, but the beneficial effect of sodium, diffusing from the glass to the absorber, was soon recognized.[13, 14] Soda-lime glass substrates are also suitable because of its

relatively low cost as well as its good surface quality. Replacing the glass with a flexible substrate, like a plastic or metal foil, would be advantageous in many ways. However, so far no such material resulting in a comparable module performance has been found.

Back contact: The criteria for a good back contact material in CIGS based solar cells are, except for being conductive, that it should provide a good ohmic contact for holes as majority carriers and at the same time provide low recombination for the electrons as minority carriers. It should also be inert during absorber deposition and preferable have a high light reflectance. Molybdenum is so far the best alternative, which also has the special quality of allowing sodium to diffuse from the glass into the absorber layer. One possible reason for the electrical relatively well behaving interface between the absorber and the molybdenum layer is the formation of a thin $MoSe_2$ layer, which has been found at this interface[15]. But as will be discussed in chapter 4.1.2, one disadvantage with molybdenum is its relatively low light reflection.

Absorber: An absolute need for the absorber in a thin film solar cell is a high absorption coefficient. This is one of the qualities that make Cu(In,Ga)Se_2 suitable as a solar cell absorber. A further description of this compound is made Chapter 2.2.

Buffer layer: Cadmium sulfide (CdS) is the buffer layer so far yielding the highest device performance. The effect of this CdS buffer layer is manifold but not completely understood, which also is illustrated by the difficulty of replacing it with a non-toxic buffer layer. Surface passivation and junction formation are two important tasks fulfilled by this layer. The best results are obtained if the around 50 nm thick CdS layer is deposited with a solution growth process often referred to as chemical bath deposition (CBD). Devices with less toxic alternative buffer layers such as In_2S_3[16] and Zn(OH,S)[17] have recently reached similar efficiencies as devices with CdS. These layers can also be deposited by a "dry" process like atomic layer deposition (ALD), which in large-scale production might be beneficial over a "wet" process like CBD. An intrinsic zinc oxide layer (i-ZnO) is commonly used as a second buffer layer. Among other things the actual need for this layer is investigated in Paper I. It is here found that if a thick enough CdS buffer layer is used, the as deposited device performance is not affected by the presence or absence of this i-ZnO layer. However, looking at the long-term stability it seems as devices degrade faster without than with this second buffer layer.

Front contact: The front contact of a solar cell has the special requirement that it should be both conductive and transparent. A few different kinds of transparent conductive oxides (TCO) exist, of which zinc oxide doped with aluminum (ZnO:Al) is the most commonly used for CIGS-based thin film solar cells.

2.2 Cu(In,Ga)Se_2 absorber layer

Due to the many including elements in ternary and multinary compounds, like CIGS, these materials often have the disadvantage of being relatively complicated

to fabricate. However, ternary and multinary semiconductors also have advantages over elementary and binary semiconductors like Si and GaAs. One such important advantage is that ternary and multinary semiconductors can have an off-stochiometric composition and still appear intrinsic.

2.2.1 Material, electrical and optical properties

Cu(In,Ga)Se$_2$ belongs to the semiconducting I-III-VI$_2$ materials that crystallize in the tetragonal chalcopyrite (CuFeS$_2$) structure. Its complete phase diagram is relatively complicated, but it can be reduced to a simpler pseudo-binary phase diagram, which for Cu-In-Se is shown in Figure 2.2.

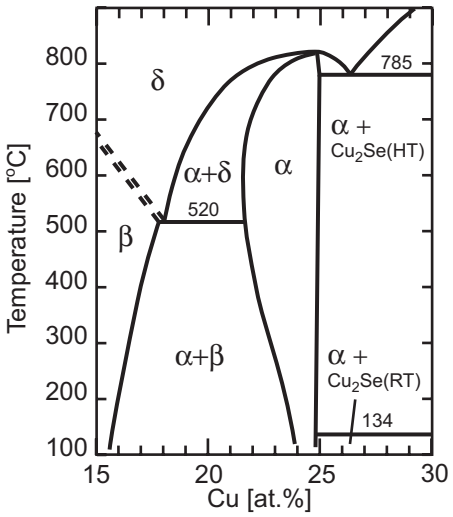


Figure 2.2. Pseudo-binary In_2Se_3 – Cu_2Se equilibrium phase diagram for compositions around the $CuInSe_2$ chalcopyrite α-phase. β represents an ordered defect phase and δ a high temperature sphalerite phase. After Gödeck et al.[18]

The phase diagram shows four different phases: the α-phase ($CuInSe_2$), the β-phase ($CuIn_3Se_5$) the δ-phase (high-temperature sphalerite phase) and the Cu_xSe phase. All the neighboring phases to the α-phase have a similar structure. For example is the β-phase a defect chalcopyrite phase, built by ordered arrays of defect pairs (V_{cu} and In_{Cu}). The existence range for the α-phase at room temperature is small and only extends over a Cu content from 24 to 24.5 %. Fortunately, it turns out that this single-phase region is widened by the introduction of sodium and partial replacement of indium with gallium.[19] Cu-rich (Cu concentration > 25 %) $CuInSe_2$ is always p-type, while Cu-poor CIS layers can be both n and p-type.[20] By heating n-type Cu-poor CIS in Se overpressure it becomes p-type and by heating a p-type CIS layer in a Se free or a Se low pressure environment it can be converted to n-type.[21] This effect is believed to originate from the selenium vacancy acting as a donor.

In CIS/CIGS based solar cells a Cu-poor p-type material with a typical carrier concentration of 10^{16} cm^{-3} is used. The minority carrier diffusion length reported for this material is typically between 0.5 and 1.5 μm[11], corresponding to electron

minority carrier life times of 1-9 ns. The main acceptor in p-type material is probably copper vacancies (V_{Cu}) and the main compensating donor selenium vacancies (V_{Se}). Many different intrinsic defects are possible in the chalcopyrite structure and these are also significantly influencing the solar cell device performance. A very important feature of the CIGS material is that the electrically neutral defect pair $2V_{Cu}+In_{Cu}$, which can compensate for off-stochiometric composition, has a low formation energy and also appears be electrically inactive.[22] This has the consequence that CIGS with a relatively large compositional variation can still result in high performance solar cell devices.

Another special quality of the CIGS material is its variable band gap. By changing the Ga/(In+Ga) ratio from 0 to 1, the band gap is increased from 1.0 to 1.7 eV[23]. CIGS has a direct band gap and for CIS the absorption coefficient is above 10^5 cm^{-1} for photon energies of 1.4 eV and higher[24].

2.2.2 CIGS deposition methods

Among the large number of possible ways of depositing polycrystalline CIGS layers there are two main approaches that have been more successful than the others, *co-evaporation* and *selenization*. The selenization process is a two-step process where the deposition and Cu(In,Ga)Se_2 formation are separated. Many variations exist of the precursor combinations and the Se reaction step. A common approach is to first deposit the metals by DC-sputtering and thereafter selenize them at an elevated temperature in an H_2Se atmosphere.[25] High efficiency devices have also been achieved by first depositing all four elements and then, for the film formation, use a rapid thermal process in a Se atmosphere.[26] Single devices, where the CIGS layer is fabricated in this type of process, have reached efficiencies of around 16 %, which is around 3 % units lower than the record device obtained with the co-evaporation method.[27] However, the effort put into the device optimization has been smaller, and for large area modules, similar efficiencies are obtained with both methods. We also note that CIGS layers grown in a selenization process spontaneously will have an increased Ga/(In+Ga) ratio towards the back contact. This occurs due to the different formation times of CIS and CGS and because the film formation starts from the top.

Co-evaporation is the second main approach for the deposition of CIGS material. Here the four elements are thermally co-evaporated in a vacuum chamber onto a heated substrate, where the Cu(In,Ga)Se_2 formation occurs. The sticking coefficients for the metals are close to one. For Se the sticking coefficient is lower and in combination with a high vapor pressure for Se, it needs to be evaporated in excess. With co-evaporation the flexibility of the process is large since the deposition rate of each element can be changed separately during deposition. The simplest stationary co-evaporation process is to keep the evaporation rates, for all elements, constant during the deposition. In the 1980:s a large improvement of the device performance was obtained at Boeing when a so called bilayer process was used.[28] In this bilayer process the deposition is started in Cu-rich conditions, and after some time the Cu/(In+Ga) ratio is reduced so that a desired final Cu-poor composition is obtained. The presence of Cu_xSe, during the Cu-rich growth phase was proposed by Klenk *et al*.[29] to explain the increased grain size observed for the CIS layers gown with this recipe. Another possible process is the so-called *inverted process*. The concept of this process was first used by Kessler *et al.*[30], starting with the deposition of In_2Se_3 at a substrate temperature below 300˚C. Then Cu and Se

were evaporated at an elevated substrate temperature until an overall composition close to stochiometry is reached. This process was later developed to the so called *three-stage process*, by depositing enough copper in the second stage so that a Cu-rich phase was reached and thereafter, in a third stage, evaporate In, Ga and Se until a Cu-poor CIGS film was obtained.[31] As mentioned above the CIGS layer in the world record device was fabricated with this method. CIGS layers grown in a three-stage process will have an increased Ga/(In+Ga) ratio both towards the back contact and the front surface with a lower ratio in between.[32]

2.3 Device operation

The general device operation for solar cells is well described in the textbooks by for example Green[33] and Fonash[34]. The solar cell performance is commonly described in the terms of four current-voltage (I-V) parameters: efficiency, η, short circuit current, I_{sc}, open circuit voltage, V_{oc}, and the fill factor, *FF*. In Figure 2.3 the ideal current-voltage characteristics of a solar cell in dark and under illumination is shown.

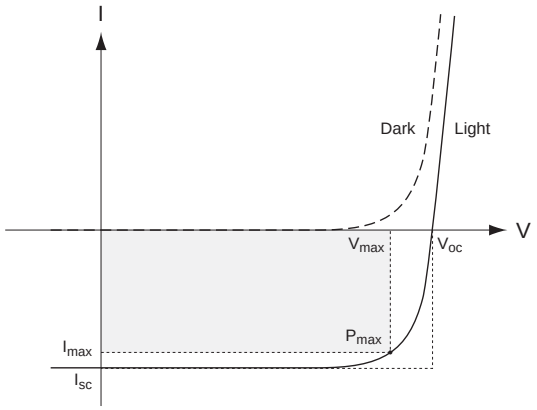


Figure 2.3. Current-voltage characteristics of a solar cell in dark (dotted line) and under illumination (solid line) Open circuit voltage (V_{oc}), short circuit current (I_{sc}) and maximum power point (P_{max}) are indicated.

The energy conversion efficiency is defined according to Equation 2.1

$$\eta = \frac{V_{\max} I_{\max}}{P_{in}} = \frac{V_{oc} I_{sc} FF}{P_{in}} \qquad (2.1)$$

where P_{in} is the total radiation incident on the solar cell. The I-V parameters are commonly measured under *Standard Test Conditions (STC)*[35]. Under these conditions the solar cell temperature is 25 ˚C and the total irradiance is 1000 W/m^2 with a spectral distribution according to a standard *Air Mass (AM)* 1.5 spectrum.[35] In the following the definitions and limitations of the three I-V parameters I_{sc}, V_{oc} and FF will be described.

2.3.1 Short circuit current

The current obtained from a solar cell in short circuit conditions is called the *short circuit current, I_{sc}*. In general terms the I_{sc} can be described by Equation 2.2

$$I_{SC} = I(V = 0V) = \int_0^d G(x) - R(x,0)dx \qquad (2.2)$$

where *G(x)* is the photogeneration of carriers as a function of the position in the CIGS film, *d* is the CIGS thickness and *R(x,V)* is the recombination at position *x* and applied voltage *V*. In short circuit conditions the applied voltage is 0 V. The photogeneration in the CIGS layer, G, is first of all limited by the light reaching this layer. The initial light intensity is reduced due to reflectance from the complete device structure and absorption in the CdS, ZnO and ZnO:Al layers. The largest loss, among these, is the reflectance from the complete device, which, however, can be reduced significantly by an anti-reflective coating like MgF_2. Another limitation of the photogeneration, G, is the absorption of light in the CIGS layer. In Paper IV a method is described from which the integrated photogeneration can be calculated as a function of wavelength, for devices with various absorber thicknesses. By comparing the integrated photogeneration (absorption) with the actual obtained quantum efficiency (QE) an estimate of the integrated recombination, R, as a function of wavelength is obtained. An astonishingly large fraction of the photogenerated carriers are contributing to the short circuit current. This implies that the recombination at short circuit conditions is rather small. I_{sc} is also commonly expressed as a current density J_{sc} [mA/cm^2]

2.3.2 Open circuit voltage

The voltage across an unloaded (open) solar cell is called the *open circuit voltage, V_{oc}*. V_{oc} is equal to the separation of the Fermi levels between the front and back contact. Theoretically this separation is, in the case of CIGS based solar cells, limited by the band gap of the CIGS layer. In practice the V_{oc} will, however, be much lower because of various recombination processes. Commonly the V_{oc} reaches a level corresponding to 50-60 % of the band gap energy. In Figure 2.4 a band edge diagram of a CIGS based solar cell under open circuit conditions and illumination is shown. The dashed lines indicate the three main recombination processes.

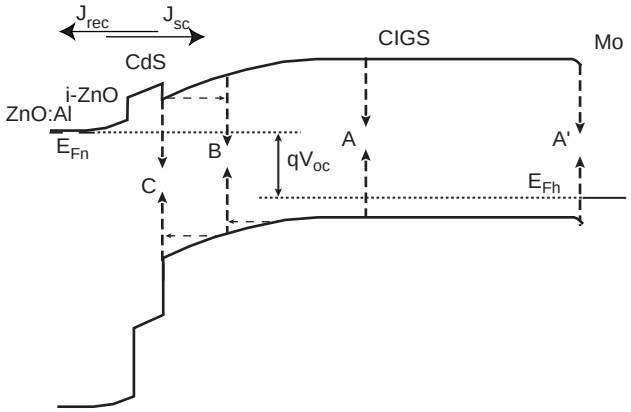


Figure 2.4. Band edge diagram for a standard CIGS solar cell under open circuit conditions and illumination. (A) Illustrates recombination in the neutral bulk and (A') recombination at the CIGS/Mo interface, (B) recombination in the space charge region (SCR) and (C) recombination at the CIGS/CdS interface. The thin dashed horizontal arrows indicate that the latter two can be enhanced by tunneling. $J_{rec}=J_{sc}$ at open circuit conditions. E_{Fn},E_{Fh} are the Fermi energies for electrons and holes respectively.

In Figure 2.4 we have considered recombination in the neutral bulk (A) and at the CIGS/Mo interface (A'), recombination in the space charge region (SCR) (B) and interface recombination (C). The horizontal dotted lines indicate that tunneling can enhance the latter two recombination mechanisms. The voltage dependence of the recombination currents A-C can be described by the general Equation 2.3[36]

$$j_{rec} = j_0(e^{\frac{qV}{AkT}} - 1) \tag{2.3}$$

where V is the applied voltage, kT/q is the thermal voltage, A the diode quality factor and the saturation current j_0 is in general thermally activated and may be expressed according to Equation 2.4[11]

$$j_0 = j_{00}e^{\frac{E_A}{AkT}} \tag{2.4}$$

where E_A is the activation energy of the recombination process and j_{00} is a prefactor. Since the recombination processes (A-C) are connected in parallel, they can all contribute to the total recombination current but commonly one dominates at $V \approx V_{oc}$. At open circuit conditions, the net current is zero and the total recombination current (J_{rec}) will exactly compensate the J_{sc}. Combining Equations 2.3 and 2.4 gives the following expression for the V_{oc}:

$$V_{oc} = \frac{E_A}{q} - \frac{AkT}{q}\ln(\frac{j_{00}}{j_{sc}}) \tag{2.5}$$

From Equation 2.5 it can be seen that the V_{oc} becomes equal to the activation energy if the temperature is reduced towards 0 K. An analytical expressions of j_{00} can be found for the different recombination processes in Figure 2.4, and thus their limitation of V_{oc}.[11] The dominating recombination process for CIGS based solar

cells is believed to be recombination process B, recombination in the SCR.[36, 37] Except for recombination losses, the V_{oc} is also affected by "parasitic losses" like series resistance, R_s, and shunt conductance, G_{sh}.

2.3.3 Fill factor

The fill factor, FF, is a measure of how "square" the output I-V characteristics are and is defined as

$$FF = \frac{V_{\max} I_{\max}}{V_{oc} I_{sc}} \tag{2.6}$$

Ideally, the FF is a function only of the V_{oc}[38]. A typical value for a CIGS solar cell is 75-78 %.

2.4 Experimental

At Ångström Solar Center a *baseline* approach is used in the fabrication and characterization of the solar cell devices.[39] This means that all steps, from substrate purchasing to device measurements, are well defined. If any alternative procedure or process is shown to be superior in any way, for example by resulting in an improved device performance or simplified process step, this process/procedure will replace the current baseline step. The baseline device gives a reference level for experimental work.

2.4.1 Device fabrication

In Figure 2.5 a cross sectional transmission electron microscope (TEM) picture of the current baseline device structure is shown.

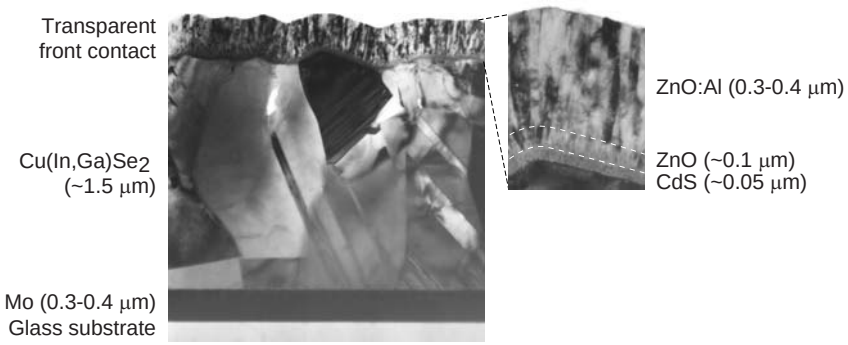


Figure 2.5. Cross sectional transmission electron microscope (TEM) picture of a baseline device structure

The molybdenum layer is fabricated by DC sputtering, yielding a 0.3-0.4 μm thick film. When choosing the deposition parameters special care needs to be taken so that the molybdenum layer allows the sodium to diffuse from the glass to the absorber. All CIGS films in this thesis are fabricated by co-evaporation from elemental sources. Figure 2.6 shows a photo of the evaporation system that has been used.

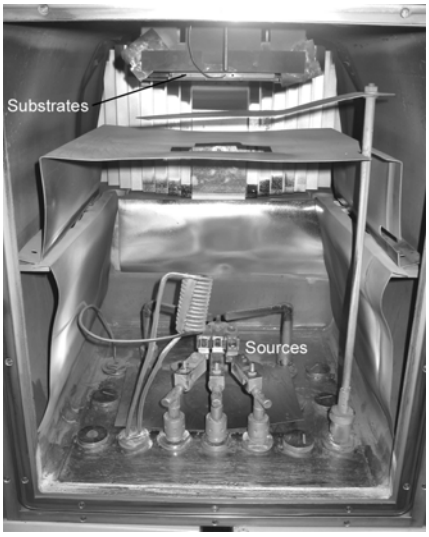


Figure 2.6. Photo of the baseline CIGS evaporation system.

In Stolt *et al.*[40] this evaporation system is described in detail. Resistively heated open boats are used as metal sources. The evaporation rate from these sources can be changed rapidly but a direct in-situ measurement of the fluxes is needed. For this purpose a quadrupole mass spectrometer with a direct view of the metal sources is used. The signal from the mass spectrometer is fed into a computer, which compares the actual rate with the desired rate, and regulates the power to the sources based on this information. Selenium is evaporated from a resistively heated quartz crucible. In a baseline deposition, the three 5x5 cm^2 Mo-coated substrates are mounted on a graphite substrate holder and placed around 40 cm above the sources. The graphite substrate holder is heated from behind with heat lamps.

In an industrial fabrication of large-scale CIGS layers with co-evaporation the substrates will travel by stationary sources. In order to realize a similar situation in our stationary system, we let the evaporation rate profile of our sources follow a similar rate which a moving substrate experience in such an industrial in-line evaporation system, see Figure 2.7.

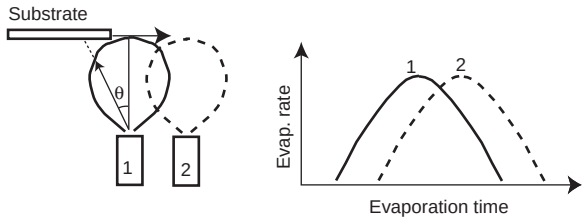


Figure 2.7. In-line evaporation system with a schematic illustration of the resulting evaporation rate profiles.

The evaporation rate profiles in an in-line evaporation system will follow a $\cos^n \theta$ relation. Here θ is defined according to Figure 2.6 and n is dependent on the design of the evaporation source and will also get an additional contribution of one, accounting for the angle of incidence. A typical value of n is 5, see for example Hanket *et al.*[41] In our stationary evaporation system we thus let the evaporation rates follow a $\cos^5 \theta$ relation. In Figure 2.8 the baseline evaporation rate profiles of the metals are shown.

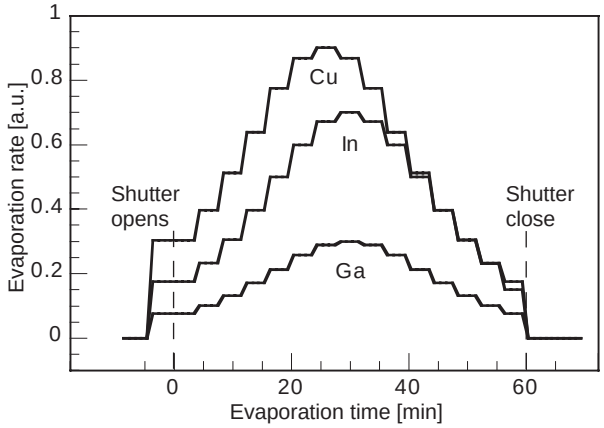


Figure 2.8. Baseline evaporation rate profiles for the metals – simulating an in-line evaporation system.

The evaporation rate profiles are divided into 17 discrete "cycles", in which the evaporation rate is constant. Each cycle is 240 seconds long. As can be seen in Figure 2.6, the peak of the Cu rate is reached one cycle before the peak rates of In and Ga. This corresponds to that the Cu-source is placed according to source 1 in Figure 2.6. The consequence of such a set up is that the CIGS film will have a Cu/(In+Ga) ratio above one during most of the deposition and first close to the end a Cu-poor composition is obtained.[42] In some cases a constantly Cu-poor baseline process is used. In this case the Cu source is simulated to be at the same position as the other metal sources so that a constant Cu/(In+Ga) ratio (<1) is obtained during growth. The Se rate is held constant during the evaporation and at the maximum metal evaporation rates it is estimated to be around 3 times higher than the rate required for stochiometric CIGS formation. The substrate temperature is kept at around 400 ˚C in the beginning of the process, and increased to approximately 500 ˚C after cycle five. The resulting baseline CIGS layer has a thickness of 1.5 μm a Cu/(In+Ga) ratio between 0.8 and 0.95 and a Ga/(In+Ga) ratio between 0.2-0.4.

The following deposition of the CdS should be done within 24 hours. The approximately 50 nm thick CdS buffer layer is fabricated in a chemical bath deposition process, by keeping the absorber in an alkaline aqueous solution containing ammonia, thiourea and cadmium acetate in around 7 minutes while the solution is heated to 60˚C. Both the i-ZnO and the ZnO:Al layers are deposited by RF-sputtering from compound targets. In order to avoid oxygen deficiency of the target and the sputtered film, the targets needs to be "re-conditioned" with oxygen. The conditioning is done by pre-sputtering in an oxygen-containing atmosphere. In

Paper I, a continuous process was investigated, where this conditioning is made during the actual deposition by adding a very small amount of oxygen (< 0.5 %). A similar film quality, in terms of conductivity versus transparency, was obtained for this process and for the few devices fabricated with this process also equal device performance was obtained. Further comparison needs to be performed before this continuous process can replace the current baseline process.

When fabricating cells and not modules, we deposit a Ni/Al/Ni grid structure on to the device, both for contacting reasons and in order to reduce resistive losses. The grids are deposited by electron gun evaporation through a shadow mask. Commonly we cut the 5x5 cm^2 substrates into three stripes, each 5x1.7 cm^2. On these stripes we define 8 cells, by scribing, with an area of 0.5 cm^2 each. In Figure 2.7 a sketch of a typical sample with 8 cells is shown.

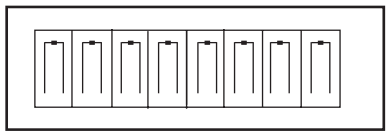


Figure 2.9. Sketch of a typical sample with 8 cells.

2.4.2 Device and material characterization

The solar cell devices are characterized with current voltage (I-V) measurements under simulated AM 1.5 G (100 mW/cm^2) illumination and in the dark. The I-V parameters presented in this thesis are average values of 8 cells from a 5x1.7 cm^2 strip, see Figure 2.9. Quantum efficiency (QE) measurements are used to calculate the short circuit current at AM 1.5 and to determine the minimum band gap. The J_{sc} calculated from the QE measurements is more accurate than the J_{sc} obtained from our I-V setup. This is because the spectrum of our I-V lamp, which is a halogen (ELH) projection lamp with a cold mirror, has a too low intensity at long wavelengths, compared to the standard air mass (AM) 1.5 spectrum[35]. In order to investigate the absorption in the CIGS layer, total reflectance and transmittance measurements were performed using a double beam spectrophotometer (Lambda 900). X-ray diffraction (XRD) measurements were performed to analyze preferred orientation of the CIGS layer and interdiffusion of gallium and indium. A Philips D5000 X-ray diffractometer, using Cu K_α radiation and a parallel beam set up (X-ray mirror on primary side and a collimator on the secondary side) was used to scan through the $\theta/2\theta$ angles. Scanning electron microscope (SEM) was used to study grain sizes and surface roughness. Transmission electron microscope (TEM) was used for a more detailed analysis of the CIGS material quality, as for example concentrations of dislocations and voids. X-ray fluorescence (XRF) was used to measure the composition of the absorber layer. For XRF system calibration a CIGS layer with a Cu/(In+Ga) ratio of 0.90 was used. For Cu/(In+Ga) ratios above this values of 0.9 the Cu/(In+Ga) ratio becomes slightly overestimated resulting in Cu/(In+Ga) values exceeding 1 for working devices, which not is expected. The absolute error of the Cu/(In+Ga) values obtained from the X-ray fluorescence measurements is estimated to be ± 0.05 but the reproducibility is better, around ± 0.02. Secondary ion mass spectrometry (SIMS) was used to determine Ga/(In+Ga) depth profiles. The CIGS thickness was measured with a profilometer.

3 The beneficial effect of Ga-grading

As mentioned in Chapter 2.2.1 a special quality of the CIGS material is its variable band gap, which can be changed by varying the Ga/(In+Ga) ratio. This quality can be used, not only to optimize the general band gap level, but also to obtain different band gaps at different depths in the CIGS film, so called band gap profiling. Already in 1957 Tauc[43] predicted that a semiconductor with such an in-depth variation of the band gap could generate an open circuit voltage under illumination. For the minority carriers a locally changed doping concentration can have similar effect as a band gap variation. The introduction of such a higher doped region close to the back contact in Si solar cells resulted in an important technological improvement in the 1970s.[44] Not only was the device performance improved, the Si thickness could also be reduced without detrimental recombination losses at the back contact. This effect is normally referred to as a *Back Surface Field (BSF)*. In CIGS thin film solar cells an in-depth band gap variation due to changes in the Ga/(In+Ga) ratio is commonly referred to as *Ga-grading*.

In the following chapter I will describe the theoretical effects of Ga-grading, make a literature review of the computer simulations performed on this topic, describe how such an in depth variation of the Ga/(In+Ga) ratio can be obtained, describe the experimental effects that we and other groups have observed and at last come to some conclusions concerning the effect of Ga-grading.

3.1 Theory

The variation of the Ga/(In+Ga) ratio, x, will affect the band gap according to

$$E_g = 1.02 + 0.67 \cdot x + b \cdot x(x-1) \qquad (3.1)$$

where values between 0.11-0.24 have been reported for the optical bowing coefficient, *b*.[23] Wei and Zunger[23] have theoretically shown that a variation of the Ga/(In+Ga) ratio will mainly affect the level of the conduction band minima. Band gap variations in the CIGS material can also be obtained by introducing other elements, like for example sulfur[45]. The results presented in this thesis are, however, limited to band gap variations obtained by different Ga/(In+Ga) ratios. In Figure 3.1, a band edge diagram for a CIGS layer with an increased Ga/(In+Ga) ratio both towards the back contact and in the SRC is illustrated.

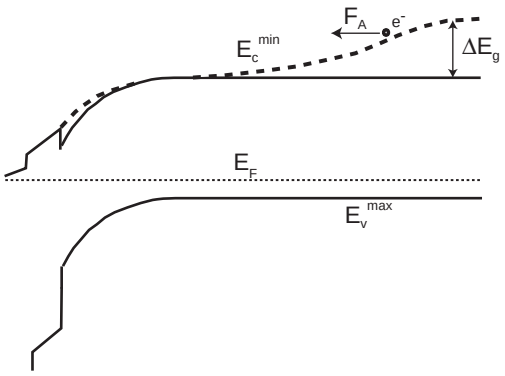


Figure 3.1. Band edge diagram of a CIGS thin film solar cell where the dotted line illustrates how the conduction band minimum (E_c^{min}) is changed for a CIGS layer with an increased Ga/(In+Ga) ratio towards the back contact and in the SCR. An additional force, F_A, acting on photogenerated electrons is obtained due to the band gap variation.

The locally increased band gap has two effects on the photgenerated electrons. First of all the recombination probability will be reduced at the position of the band gap increase.[46] Secondly an additional force, F_A, acting on the these electrons is obtained and can be described by[34]

$$F_A = q\left(\frac{d\Delta E_g}{dx} + \frac{kT}{\Delta n}\cdot\frac{d\Delta n}{dx}\right) \qquad (3.2)$$

where Δn is the change in electron concentration due to the Ga-grading. Here we have assumed that $d\Delta N_c/dx$ is zero, where ΔN_c is the change in density of states in the conduction band due to the Ga-grading. The second tern in Equation 3.2 is a diffusion term, arising from a changed gradient of the electron concentration due to the Ga/(In+Ga) variation. By assuming a linear variation of ΔE_g over a distance Δx and a linear variation of Δn over the same distance, we can see that this term becomes small compared to the first term if $\Delta E_g > kT$. In such a case the additional force from the Ga-grading becomes $q\cdot d\Delta E_g/dx$. This force corresponds to an additional effective electric field, $\xi_A = d\Delta E_g/dx$.

3.1.1 Potential effects of Ga-grading

In the following I have classified the effects an in-depth variation the Ga/(In+Ga) ratio can have on the device performance into four different categories.

1) *Improved V_{oc} by reduced impact of regions with high recombination*
   At open circuit conditions the dominating part of the recombination is expected to occur in the SCR region, c.f. Chapter 2.3.2. By increasing the Ga/(In+Ga) ratio here this recombination can be reduced, resulting in an improved V_{oc}. But as illustrated in Figure 3.1, an increased conduction band minimum in the SCR will also reduce the resulting electric field at the p-n junction with the possible consequence of a decreased carrier collection. An increased band gap in the front part will also reduce the absorption in this region. This can be compensated for by an increased absorption further into

the CIGS layer, where the band gap not is increased. Photoelectrons generated deeper into the CIGS material will on the other hand have a lower collection probability. Whether an increased Ga/(In+Ga) ratio in the SCR will have a net beneficial effect or not is difficult to predict analytically.

At the CIGS/Mo interface it would be desirable with an additional force keeping the photoelectrons away from this interface, which is expected have a relatively high recombination velocity. By an increased conduction band minimum, towards the back contact, we can keep the good conductivity for the majority holes and at the same time reject the minority electrons. An increased band gap will also here, further into the CIGS layer, lead to a reduced light absorption. But since the photogeneration of carriers is expected to be rather small here anyway, this should only have a small effect on the resulting short circuit current. Whether this passivation of the CIGS back contact will have any significant beneficial effect or not, will depend on how detrimental this CIGS/Mo interface is for the device performance. As mentioned earlier a thin layer of $MoSe_2$ has been observed between the CIGS and Mo layer, which potentially could lead to a spontaneous passivation of the backcontact[11]. If this is the case, the effect of an additional passivation by a Ga-grading would be reduced.

In order to analytically estimate the potential for a V_{oc} improvement by a back contact passivation, Equations 3.3 and 3.4 can be used. Equation 3.3 describes the limitation of the V_{oc} due to recombination in the neutral bulk, where the effective diffusion length is described by Equation 3.4.[11]

$$V_{OC} = \frac{E_g}{q} - \frac{kT}{q}\ln\left(\frac{qD_e N_C N_V}{J_{sc} N_A L_{eff}}\right) \tag{3.3}$$

$$L_{eff} = L_d \frac{\cosh(d/L_d) + S_b L_d / D_e \sinh(d/L_d)}{\sinh(d/L_d) + S_b L_d / D_e \cosh(d/L_d)} \tag{3.4}$$

Here L_d is the bulk diffusion length, D_e is the diffusion constant for minority electrons, S_b is the recombination velocity at the back contact, N_c and N_v the density of states in the conduction and valence band respectively, N_A the net acceptor concentration and d is the thickness of the neutral bulk. With values of the parameters according to Rau and Schock[11]: D_e=2.6 cm^2s^{-1}, N_C=6.7·10^{17} cm^{-3}, N_V=1.5·10^{19} cm^{-3} and N_A=10^{16} cm^{-3} and assuming a L_d=1 µm and a SCR width of 0.3 µm, the gain in V_{oc} by reducing S_b from 10^6 cm/s down to 10^4 cm/s for a device with a standard CIGS thickness of 1.5 µm, is only 6 mV. This clearly illustrates that the bulk diffusion length must be at least as long as the CIGS thickness if the back contact should have any significant influence on the device performance. For a device with a CIGS thickness of 0.5 µm, the corresponding gain is 40 mV.

2) Improved J_{sc} due to field assisted carrier collection

Carrier collection of photoelectrons generated outside the SCR in homogeneous CIGS layers rely on diffusion. The collection probability, f_c, outside the SCR is given by[38]

$$f_C = e^{\frac{-X}{L_d}} \tag{3.5}$$

where x is the distance from the SCR and L_d is the diffusion length. As illustrated in Figure 3.1 an additional force acting on the electrons can be obtained by increasing the Ga/(In+Ga) ratio towards the back contact, potentially improving the carrier collection. In order to qualitatively estimate how large influence a Ga-gradient can have on the carrier collection, we can estimate how far an electron can drift in the additional effective electric field during one minority carrier lifetime. Equation 3.6 describes the additional length, L, that an electron with mobility, μ_e can drift in the additional effective electric field ξ_A, during a lifetime, τ_e.

$$L = \mu_e \cdot \xi_A \cdot \tau_e = \frac{\xi_A}{kT/q} \cdot L_d^{\,2} \approx 1 \cdot 10^7 \cdot L_d^{\,2}\ [m] \tag{3.6}$$

By the use of $L_d = (D_e \cdot \tau_e)^{1/2}$ and $D_e = kT/q \cdot \mu_e$ we come to the second expression in Equation 3.6. Assuming a linear additional effective electric field of $3 \cdot 10^5$ V/m through the neutral bulk of the CIGS layer (corresponding to a conduction band minimum increase of 0.3 eV over 1 μm) the last expression is obtained. For a typical diffusion length of 1 μm the additional length an electron in this electric field can move is in average 10 μm. This means that the carrier collection can be significantly improved with the additional field obtained from Ga-grading. From Equation 3.6 we can also see that the length an electron can move in an electric field is proportional to L_d^2. This means that the additional length L becomes much longer in a material that has a long diffusion length already without Ga-grading. On the other hand, the carrier collection in such a material is expected to be high anyway, and the potential for improvement is smaller than in a material with shorter diffusion length. Ultimately, it will be a balance between an improved carrier collection and reduced absorption that decides whether there will be a net improvement of the short circuit current or not, c.f. Equation 2.2.

3) *Additional contribution to the Photovoltaic effect*

As mentioned above, *Tauc* already in 1957 predicted that a semiconductor with a band gap variation can generate an open circuit voltage under illumination. In the same way that an electric field, obtained at a p-n junction, can generate a V_{oc}, an effective electric field originating from a compositional variation can generate a photovoltage. In 1979 Fonash and Ashok[47] showed that these two effects can be added so that an additional photovoltaic effect is obtained from a band gap variation. However, unless the light intensity is high at the position where the band gap variation takes place, this additional effect will not have a measurable contribution to the V_{oc}.

4) *Material quality effect*

Ga-grading can also indirectly influence the device performance by affecting the material quality of the CIGS layer. The lattice constants for CGS are somewhat different from those of CIS. This means that by introducing variations of Ga/(In+Ga) ratio in the absorber, there will be stress built into the

lattice and/or dislocations will occur. Both of these might have a detrimental affect on the material quality, lowering the minority carrier lifetime. If a CIGS layer is fabricated by co-evaporation and an increased Ga/(In+Ga) ratio towards the back contact is desired, the deposition must be started with pure CGS or CIGS with a high Ga/(In+Ga) ratio. Such layers with high Ga/(In+Ga) ratio have, to our experience, both smaller grains and a different preferred crystal orientation than CIGS with a lower Ga/(In+Ga) ratio.[42] Since these layers are deposited in the beginning of the deposition they can affect the orientation and morphology of the complete CIGS layer.[48] The electric quality of CIGS layers with a Ga/(In+Ga) ratio above 0.5 is also reported to be reduced.[49]

3.1.2 Device simulations

The band gap profiling is commonly classified in two categories, *normal* and *double* grading. Normal grading is an increase of the band gap towards the back contact, while the double grading profile has a minimum band gap some distance into the CIGS layer and an increased band gap both towards the back and front contact (see Figure 3.1). The complexity of how the device performance is affected by an in-depth variation of the Ga/(In+Ga) ratio is well illustrated by the diverse results obtained by simulations on this topic.

A few device simulations have been performed using the simulation program ADEPT[50]. Gray and Lee[51] used this program and simulated a band gap structure with a minimum band gap 0.5 μm into the CIGS layer. By linearly increasing the band gap from 1.0 at this point up to 1.2 eV at the back contact a small improvement of the carrier collection resulting in an increased J_{sc} of 0.6 mA/cm^2 was obtained. A larger improvement of the device performance was obtained by increasing the band gap towards the surface, which resulted in an increased V_{oc}. Similar results were obtained by Gabor *et al.*[32], using the same simulation tool.

Dhingra *et al.*[52] used a p-i-n model for the CIS device structure and varied the grading in the intrinsic region. With this structure improved efficiencies were obtained using a normal, a double and a reverse (linearly increased band gap from the back to the front contact) grading structure. Topic *et al.*[53] used a simulation tool developed at the University of Ljubljana. In their optimum band gap profile the conduction band minimum increased linearly from just outside the SCR towards the back contact with 0.3 eV. Due to an increased J_{sc} this band gap structure improved device performance by 5 %. By simulating a double grading profile, a slight increase in V_{oc} was obtained, but due to a reduced FF and J_{sc} no gain in efficiency was observed. Menner *et al.*[54] simulated a perfect electron mirror at the back contact and pointed out that the combination of a high absorption coefficient and short diffusion length (~ 0.7 μm) makes the gain by such a mirror insignificant.

In Paper III simulations were performed on how a normal Ga-grading profile could influence the device performance by reducing back contact recombination in devices with 2 μm thick CIS layers. In line with what was said under point 2 in Chapter 3.1.1, a bulk diffusion length as long as 4 μm had to be assumed in order to explain the observed increase in V_{oc} for the devices with Ga-grading.

All the simulations mentioned above predict a small increase of J_{sc} for a normal grading profile, due to an improved carrier collection. A majority also predicts a larger gain in efficiency by the use of a double grading profile. In some cases

different results are obtained, but since all the details of the simulations often not are presented, it is difficult to point out originating reasons for these differences.

3.2 Obtaining a Ga-gradient

In the previous section we discussed a few effects of an in-depth variation of the Ga/(In+Ga) ratio. The next question to be answered is - how can such an in-depth variation of the Ga/(In+Ga) ratio be obtained and what are the limitations of the obtainable Ga/(In+Ga) profiles?

As described in Chapter 2.2.2, the selenization process results in a spontaneous *normal* Ga-grading and in the three-stage process in a *double* Ga-grading profile. Some variation of these Ga-grading profiles is possible but the flexibility is strongly limited.[31, 45] By using a single or bilayer co-evaporation process, in principal any in-depth variation of the Ga/(In+Ga) ratio can be obtained by varying the gallium and indium deposition rates during the evaporation. The "as-deposited" Ga-grading profile is only limited by how fast the sources can change their deposition rate. However, as gallium and indium gradients are introduced into the material, diffusion will tend to reduce this Ga/(In+Ga) variation. Depending on how fast this diffusion process is, it will limit the obtainable Ga-gradient profiles. In Paper VI and VII the indium and gallium diffusion and intermixing have been investigated and a summary of the results and conclusions is presented in the following.

3.2.1 Diffusion of In and Ga

A common belief in the CIGS community has been that the diffusion of gallium and indium is very rapid in Cu-rich CIGS films (Cu/(In+Ga) > 1). Because of this, a Cu-rich phase during deposition, has in some cases, been avoided under the assumption that no Ga-gradient would sustain such conditions. In our Ga-grading experiments, where we had a Cu-rich growth stage we did, however, still observe a Ga-gradient. The Paper mostly referred to concerning the high diffusion in Cu-rich grown CIGS is by Walter and Schock[48]. In this Paper, multilayer structures of CIS and CGS layers were evaporated on borosilicate glass (Corning®7059) substrates, resulting in essentially sodium-free CIS/CGS films. This motivated us to investigate how the presence of sodium influences the diffusion of indium and gallium. In order to do so, we fabricated two bilayer structures, CIS on CGS and CGS on CIS. The structures were both fabricated in a Cu-rich and in a Cu-poor process. In each CIS/CGS and CGS/CIS run, molybdenum coated soda lime glass substrates, with and without a sodium barrier of Al_2O_3 were used. This meant that we could study how the diffusion was influenced by sodium. The bilayers were deposited in 30 minutes at a substrate temperature of 500 ˚C, resulting in a total thickness of 1 μm.. The bilayers were subsequently analyzed with secondary ion mass spectrometry, X-ray diffraction, scanning electron microscope and transmission electron microscope equipped with energy dispersive x-ray spectroscopy (TEM-EDS). We made the following observations concerning the diffusion of indium and gallium:

- The main diffusion takes places inside the grains, possibly by vacancy diffusion, i.e. the diffusing atoms are moving via vacant lattice sites in the crystal. Diffusion in the grain boundaries is not significantly higher than

inside the grains, not even if the layers are Cu-rich. Indium has a similar diffusivity in CGS as gallium in CIS.

- The diffusion is higher in sodium-free films than in films containing sodium, possibly due to increased concentration of metal vacancies, which could promote diffusion. Sodium free Cu-rich layers show higher diffusion of In and Ga as compared to sodium-free Cu-poor layers. This can be explained by higher concentrations of the for indium and gallium diffusion more favorable V_{Ga} and V_{In} in the Cu-rich films compared to V_{cu} in the Cu-poor films.[55]
- In the presence of sodium, there is no increase of the diffusion in Cu-rich layers as compared to Cu-poor layers.

From these bilayers structures we also got an estimation of how steep Ga-gradients that can be obtained in our CIGS layers. In Figure 3.2, SEM pictures, SIMS depth profiles and XRD plots are shown for two sodium containing bilayer structures with CGS in the bottom and CIS at the top, one grown under Cu-rich conditions (Cu/(In+Ga)=1.1) and one under Cu-poor conditions (Cu/(In+Ga)=0.95).

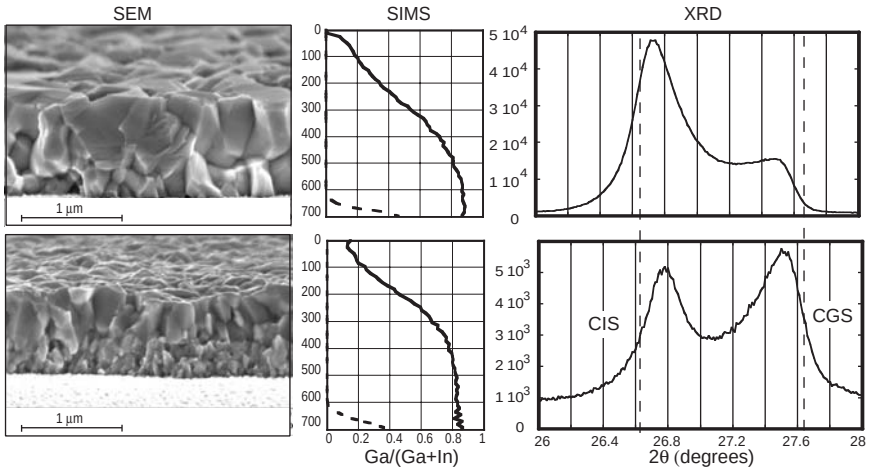


Figure 3.2. Two bilayers*, CIS on top of CGS, grown with sodium under Cu-rich conditions (top) and Cu-poor conditions (bottom) are illustrated with a SEM picture (left), SIMS depth profile (middle) and XRD graph showing the (112) peak (right). The y-axis on the SIMS profile is the sputter time, the dotted line in the SIMS profile represents the measurement signal from the molybdenum back contact and the dotted lines in the XRD plot indicate the peak position of the single CGS and CIS layers.*

In the SEM pictures a two-layer structure can be seen, with smaller grains in the bottom part, where the CGS layer was deposited. The SIMS depth profiles and XRD plots show a relatively strong interdiffusion in both samples. The fastest variation of the Ga/(In+Ga) ratio is seen in the Cu-poor layer, for which the Ga/(In+Ga) ratio is ranging from around 0.8 to around 0.1 over a distance of 0.5 µm. That results in an effective electric field about 10^6 V/m.

In the XRD spectra, two separate peaks can be observed for both bilayer structures. From both SIMS and XRD it seems as if the intermixing has been slightly higher close to the original interface between the CIS and CGS layer in the Cu-rich bilayer. In the SEM picture for this bilayer it can also be seen that the top part of the deposited CGS layer, closest to the original interface with the CIS layer, also has a larger grain size compared to the bottom part. We interpretate this as that a re-crystallization has occurred, see Paper VI. The re-crystallization could be a sign that some kind of re-organization has occurred, which could also possibly explain the enhanced intermixing of indium and gallium in this region. This re-crystallization effect is only observed in Cu-rich layers and is even stronger in the sodium free bilayers. The observation by Walter and Schock[48] of a large difference in intermixing of In and Ga in Cu-rich and Cu-poor layers could be explained by this effect, rather than an increased diffusion.

Concerning our initial question of how a Ga-gradient can be obtained and what the limitations are, we have learnt that:

- The interdiffusion is in general so high that depositing pure CGS in the beginning of the process can be used to obtain a smooth Ga-gradient in the CIGS film.
- Ga-gradients can be nearly as steep in CIGS layers grown under Cu-rich conditions as CIGS layers grown under Cu-poor conditions.
- From Ga-grading an additional effective electric field of 10^6 V/m can be obtained. However, the stronger field, the larger change of the Ga/(In+Ga) ratio, which also means a stronger material related effect as discussed in Chapter 3.1.1- point 4.

3.3 Experimentally observed effects of Ga-grading

The CIGS layer in the world record device was fabricated with the *three-stage* process[9]. As mentioned in the previous chapter, CIGS layers grown with this process will have a double grading profile. But, since homogenous CIGS layers can not easily be fabricated with this process, it is difficult to make comparative studies, showing that the high efficiencies obtained really are due to the double Ga-profile and not the process itself. In this perspective a single or bilayer co-evaporation process is a more suitable deposition method, since both homogenous and Ga-graded CIGS layers can be fabricated under similar conditions. In the following a review of experimentally observed effects of Ga-grading found in the literature will be presented, thereafter our results on the effect of Ga-grading, at different conditions, will be described.

3.3.1 Literature review

The first paper describing an in-depth variation of the Ga/(In+Ga) ratio, in CIS based thin film solar cells, is a paper by Tuttle *et al.*[56] (1989). In this paper $CuGaSe_2$ layers of various thickness were deposited, both at the back and in the front of CIS layers. With the CGS layer at the back the authors observed improved QE values at long wavelengths but at the same time reduced values at short wavelengths, with no resulting net gain in the J_{sc}. For the devices with CGS deposited at the front a higher V_{oc} was obtained, but an even stronger reduction of J_{sc}. Birkmire *et al.* 1990 increased the band gap towards the surface in CIS based solar cells by adding Ga. A slightly improved V_{oc} was obtained but the overall

efficiency was significantly reduced. Menner *et al.*[54] in 1991 added differently thick CIGS layers in the front part of CIS layers. The best device was obtained for a 20 nm thick Ga containing layer at the surface, which, however, was not significantly better than the pure CIS devices. In 1993 Jensen *et al.*[57] fabricated CIS layers in a selenization process on substrates with and without a thin layer of a Ga containing precursor and observed an efficiency increase from 10.5 to 11.7 % for the device with a Ga-precursor. The increased performance was mainly due to a gain in V_{oc} (around 50 mV).

Contreras *et al.* [58] obtained in 1993 the so far highest open circuit voltage in a CIGS based solar cell, 687 mV, by the use of a Ga-graded co-evaporated CIGS layer. Since no comparative study between samples with and without Ga-grading was performed, no conclusion can be made that the high V_{oc} obtained was due to the effect of the Ga-grading. In 1996 Contreras *et al.*[59] compared results from devices with both normal and double grading profiles fabricated by both a bilayer and a three-stage co-evaporation process. For a similar Ga-profile the CIGS layers fabricated with the three-stage process yielded around 1 % unit higher efficiencies than CIGS layers fabricated in the bilayer process. For the CIGS layers fabricated in the bilayer process, the ones with a double grading profile had slightly higher efficiencies than the CIGS layers with a normal grading profile. However, no conclusions concerning the beneficial effect of Ga-grading were made.

Gabor *et al.*[31] investigated Ga-grading effects in devices where the CIGS layer is grown with the three-stage process. Different Ga/(In+Ga) ratios of the material deposited in the third stage were used and an increased efficiency was observed for increased Ga/(In+Ga) ratios. However, the gain was not due to an improved V_{oc} as the simulations in the same paper predicted, but due to a higher FF and $J_{sc.}$ Shafarman *et al.*[49] coevaporated CIGS layers with different bulk Ga/(In+Ga) ratios on substrates with and without an elemental Ga layer deposited prior to the CIGS deposition. An increased FF was observed at all Ga/(In+Ga) ratios but a net reduction of the efficiency was obtained due to a reduced J_{sc}.

Dullweber *et al.*[60] investigated samples with both normal and reverse Ga-gradings and concluded that the carrier collection can be influenced by graded band gaps. Since the efficiencies were rather low (10-12 %), the Cu content varied largely (between 17 and 22 atomic %) and an improved carrier collection was obtained also for a device with a reverse Ga-grading, no conclusion concerning the beneficial effect of Ga-grading can be made. In the same paper, samples with a "multi grading" profile were analyzed. These and some additional samples were also further investigated and discussed in Dullweber *et al.*[60, 61, 62]. The multigrading CIGS layers have an increased band gap towards the back contact, a minimum band gap 0.5-1 μm from the surface, an increased band gap in the SCR and a slightly reduced band gap at the very surface. For these devices the authors claim that the V_{oc} is correlated to the band gap in the SCR, whereas the J_{sc} is more correlated with the minimum band gap. The conclusions are not convincing and from the presented data it is not clear how the FF is influenced by the increased Ga/(In+Ga) ratio in the SCR.

In 2002 Orgassa *et al.*[63] investigated alternative back contact metals in comparison to the normally used molybdenum. On to these different back contact metals, both homogeneous and a Ga-graded CIGS layers were deposited. For devices with a homogeneous CIGS layer that experienced a significantly reduced

device performance due to the back contact material, the authors observed a large improvement by the use of Ga-graded CIGS layers. However, the Ga-graded CIGS layers were 1.4 μm thick, while the homogeneous CIGS layer was only 0.9 μm thick. This makes the results less conclusive.

From the experimental results available in the literature no clear conclusions concerning the beneficial effect of the Ga-grading can be made, often because good reference devices with a homogenous CIGS layer are missing. It is, however, clear that high efficiency devices can be made using Ga-graded CIGS layers, both with normal and double grading profiles. The only cases for which a significant gain in efficiency is obtained by the incorporation of Ga, is for pure CIS [57].

3.3.2 Optimization of the Ga-profile

The aim of this study was to investigate if we could observe any beneficial effect of Ga-grading in our baseline devices, and if so, what the optimal Ga-profile should look like. Most of the results are presented in Paper II, but our setup for measuring QE has been improved since Paper II was written and in this chapter the re-measured data will be used. We limited our investigation to normal Ga-grading profiles, with an increased Ga concentration towards the back contact. The motivation for this limitation is the result from an earlier study in our group, mentioned in Paper II, where the Ga/(In+Ga) ratio was increased in the front part of the CIGS layer without any beneficial effect.

In Chapter 3.2 I concluded that a smooth Ga-gradient can be obtained by depositing pure $CuGaSe_2$ in the beginning of the process. By varying the thickness of this initial CGS layer and also by varying the bulk Ga/(In+Ga) ratio, CIGS layers with different Ga-grading profiles were obtained. In Figure 3.3 the evaporation rate profiles for a CIGS layer with a CGS layer deposited in the beginning of the process is shown. Indium is replaced by gallium, here in the four first cycles of the deposition, otherwise the same evaporation rate profiles are used as for our baseline process. From now on this process will be referred to as a Ga-graded baseline process.

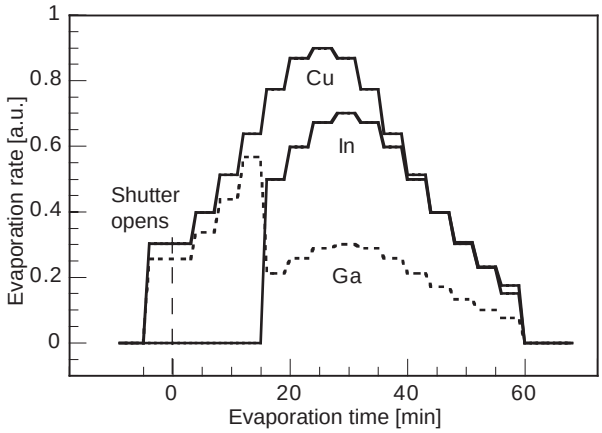


Figure 3.3. Metal evaporation profiles for a Ga-graded baseline evaporation. Ga replaces In in the first four cycles.

In order to investigate the Ga-grading profiles, obtained by the different CGS thicknesses and the different Ga/(In+Ga) bulk ratios, the CIGS layers were analyzed with SIMS and XRD. In Figure 3.4 (a) SIMS depth profiles of the Ga intensity (normalized to the intensities of the other elements) for five CIGS layers are shown and in Figure 3.4 (b) XRD plots of the (112) peak for the same CIGS layers are shown. Two of the CIGS layers have a homogenous Ga/(In+Ga) concentration of 0.25 and 0.5 respectively. Two have the same bulk Ga/(In+Ga) concentrations but with a CGS layer deposited at the bottom, corresponding to 30 % of the final thickness. The fifth CIGS layer has a bulk Ga/(In+Ga) concentration of around 35 % with a deposited CGS layer corresponding to around 15 % of the total CIGS thickness, i.e. with a bulk Ga/(In+Ga) ratio in between the two others and with half of the CGS thickness.

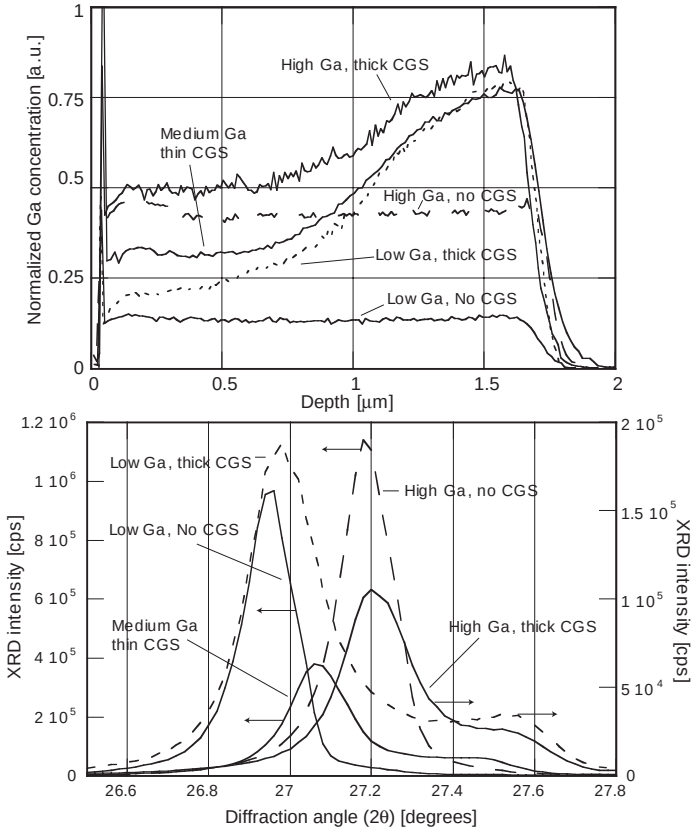


Figure 3.4. a) SIMS depth profiles of the normalized Ga intensity and b) XRD plot of the (112) peak for five CIGS layers with different Ga/(In+Ga) ratios and CGS back contacts.

The SIMS depth profiles and the XRD data together give a coherent picture of the different Ga-grading profiles. From the SIMS profile we get the depth profile and from the XRD spectra we can estimate the maximum and minimum Ga/(In+Ga) ratios. As expected the strongest Ga-gradient is obtained for the Ga-graded CIGS layer with the lowest Ga/(In+Ga) bulk ratio (0.25) and the thicker

CGS layer, corresponding to 30 % of the total thickness. In this film the Ga concentration changes throughout the entire CIGS layer with a Ga/(In+Ga) ratio of around 0.8 at the back and slightly above 0.25 at the front, according to the XRD peak positions. The Ga-gradient in the layer with the highest Ga concentration, as well as the CIGS layer with the medium high Ga concentration, does not reach all the way to the front surface. The upper third part of these CIGS layers has a constant Ga concentration.

The CGS bottom layer also has an impact on the film texture. By comparing CIGS films with and without a CGS bottom layer, we observe a much lower preferred (112) orientation in the films with a CGS layer. Thicker CGS bottom layers lead to a further reduction of the (112) orientation.

In Figure 3.5 the I-V data for these five samples is shown as a function of the thickness of the initial CGS layers and their bulk Ga/(In+Ga) ratio.

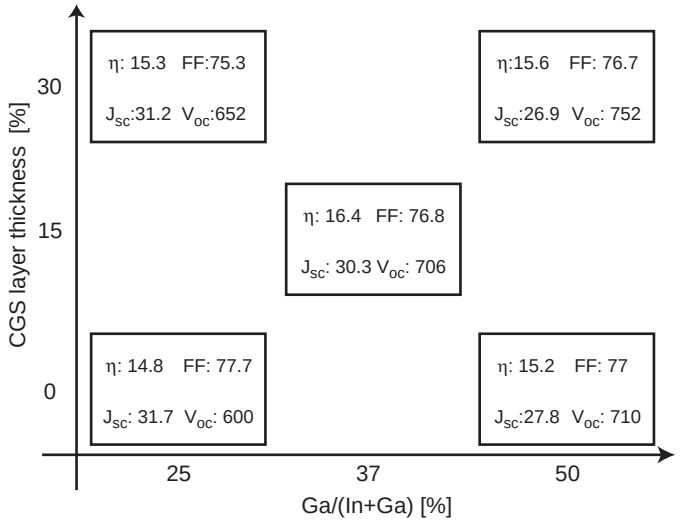


Figure 3.5. η, FF, J_{sc}, and V_{oc} for five devices with different bulk Ga/(In+Ga) ratios and/or different thickness of the bottom CGS layer(given in % of the total thickness).

The trend for these devices is an increased performance as Ga-graded CIGS layers are used. The best efficiency is obtained for the sample with a bulk Ga/(In+Ga) ratio of around 35 % combined with a CGS layer corresponding to around 15 % of the total CIGS thickness. This recipe was also used in the fabrication of the current world record thin film solar module, with an efficiency of 16.6 %[10]. From the I-V parameters in Figure 3.5 it appears like the V_{oc} is improved for the devices with a Ga-graded CIGS layer. However, as can be seen in Figure 3.4, the Ga-graded CIGS layers have slightly increased Ga concentrations also in the front part, which means that the minimum band gap is increased. From this data alone we cannot say whether the increase in V_{oc} is due to this increased band gap or due to the Ga-grading. Since the Cu/(In+Ga) ratio varies somewhat for these CIGS layers (between 0.8 and 0.95), and this variation can have some effect on the device performance we save the detailed analysis of the beneficial effect of Ga-grading for the next chapter. Concerning the Ga-grading optimization it seems

as if a CGS layer corresponding to around 15 % of the total thickness results in a superior Ga-grading profile compared to a CGS layer that corresponds to 30 % of the total thickness.

3.3.3 The effect of Ga-grading at baseline conditions

Since the effect of Ga-grading seems to be relatively small we have compared a large set of devices with and without a Ga-grading in this study, so that a statistically significant result can be obtained. The results are from Paper VIII, with some new unpublished data added.

Both the baseline process and the Ga-graded baseline process are regularly used to fabricate CIGS layers in our laboratory. In the Ga-graded baseline process a CGS layer with a thickness corresponding to 10-15 % of the total thickness is used. Since the device performance is significantly affected by the Cu/(In+Ga) ratio, see for example Paper VIII, and the effect of Ga-grading is relatively small, it only makes sense to compare devices with a similar Cu/(In+Ga) ratio. In order to compare open circuit voltages (V_{oc}) and short circuit currents (J_{sc}) of devices with slightly different Ga/(In+Ga) ratios, we introduce the following "band gap normalized" I-V parameters: $\Delta V_{oc} = V_{oc}-(E_g/q-0.6V)$ and $J_{sc}^{rel} = J_{sc}^{measured}/J_{sc}^{max}$. Here E_g is the band gap of the CIGS layer, q the elementary charge, $J_{sc}^{measured}$ is the J_{sc} obtained from the QE measurement and J_{sc}^{max} is the J_{sc} that would be obtained in a device with the QE equal to 1 between 360 nm and the wavelength corresponding to the band gap, E_g. For example is J_{sc}^{max} 40 mA/cm^2 for a band gap of around 1.2 eV, which means that 1 % unit of J_{sc}^{rel} corresponds to 0.4 mA/cm^2. The expression for ΔV_{oc} is defined as above since the V_{oc} is roughly proportional to E_g for band gaps between 1.1 and 1.25 eV[37] and by subtracting 0.6 V, ΔV_{oc} values greater than zero are generally obtained.

In Figure 3.6 the η, ΔV_{oc}, J_{sc}^{rel} and the FF is shown as a function of the Cu/(In+Ga) ratio for a large number of samples, grown at baseline conditions both with and without a Ga-grading. I remind that each point in Figure 3.6 is an average over 8 individual cells.

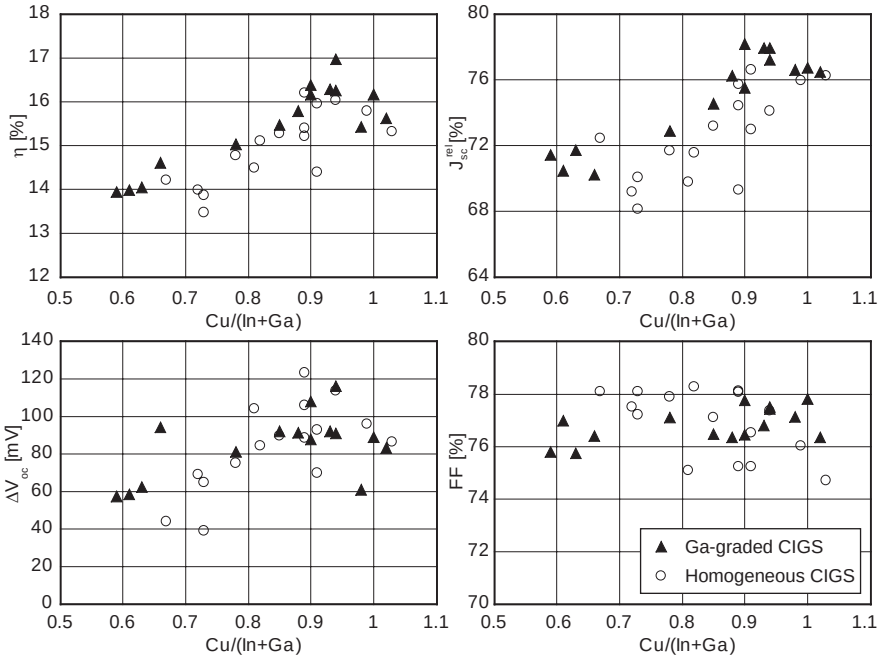


Figure 3.6. The band gap normalized I-V parameters η, FF, ΔV_{oc} and J_{sc}^{rel} versus the Cu/(In+Ga) ratio for devices with and without a Ga-graded CIGS layer.(For Cu/(In+Ga) ratios above 1 see 2.4.2)

In Paper VIII some of these I-V data are presented with the focus on how device performance is affected by the Cu/(In+Ga) ratio. Here we focus on the beneficial effect of the Ga-grading and we can first of all state that the effect of the Ga-grading is small, but there is a statistically significant beneficial effect. In order to obtain numbers that make sense to compare for these devices with such a large variation in the Cu/(In+Ga) ratio, we divided the CIGS layers after their Cu/(In+Ga) ratio into four different groups. Within each group the performance variation is relatively small. In table 3.1 the difference in the band-gap normalized I-V parameters between devices with Ga-graded and homogenous CIGS layers is shown for the four different Cu/(In+Ga) regions, where the last column shows the average over these four regions.

Table 3.1.The difference in the band gap normalized I-V parameters between Ga-graded and homogeneous CIGS layers in different Cu/(In+Ga) regions. The average is taken over the four intervals in the table.

Cu/(In+Ga) ratio	-0.75	0.76-0.85	0.86-0.95	0.96-	Average
$\eta_{Graded} - \eta_{Homo}$	0.27	0.34	0.77	0.16	0.4 [% units]
$FF_{Graded} - FF_{Homo}$	-1.5	-0.3	0.3	0.17	0.0 [% units]
$J_{sc}^{rel}{}_{Graded} - J_{sc}^{rel}{}_{Homo}$	0.74	2.18	3.3	1.3	1.6 [% units]
$\Delta V_{oc\ Graded} - \Delta V_{oc\ Homo}$	15	-2	-1	-7	1.5 [mV]

In average the devices with a Ga-graded CIGS layer have 0.4 % units higher efficiency than devices with a homogeneous CIGS layer with a similar Cu/(In+Ga) ratio. The gain is largest for Cu/(In+Ga) ratios between 0.86-0.95, where also the overall best device performance is obtained. All the gain in efficiency can be attributed to an improved J_{sc}. Concerning the FF, there is no gain for devices with a Ga-grading and at Cu/(In+Ga) ratios below 0.9 the FF is even slightly larger for the devices with homogenous CIGS layers. The difference in V_{oc} (same as the difference in ΔV_{oc}) is very small. In Figure 3.7, the QE as a function of wavelength is shown for two typical devices, with and without Ga-grading.

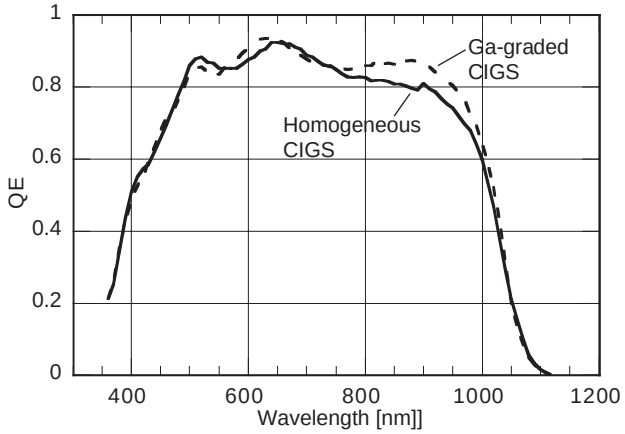


Figure 3.7. QE for devices with and without Ga-grading but similar Cu/(In+Ga) ratio.

The carrier collection for the device with the Ga-graded CIGS layer is improved for photoelectrons generated by light with a wavelength longer than 800 nm. The improved carrier collection in Figure 3.6 corresponds to a gain in J_{sc} of 0.7 mA/cm^2. In Paper VIII we argue that the longest diffusion length is obtained for the material with a Cu/(In+Ga) ratio between 0.85 and 0.95 and it is also for these devices that we see the largest gain in J_{sc} due to the Ga-grading.

3.3.4 The effect of Ga-grading at high deposition rates

In this chapter the effect of Ga-grading is investigated for devices where the CIGS layer is deposited at a higher deposition rate than under baseline conditions, is investigated. Both in Paper VI and Paper VIII CIGS layers at high depositions rates, with and without Ga-grading, are presented. However, the Ga-graded CIGS layers presented in Paper VI, have a more optimized Cu/(In+Ga) ratio, compared to the homogenous CIGS layers. This means that they are less suitable for a detailed analysis of the beneficial effect of Ga-grading. Most of the results presented here are from Paper VIII.

In order to reduce the deposition times, we simulated an increased travel speed of the substrates and increased the evaporation rates correspondingly so that the same CIGS thicknesses were obtained. No effect of the Ga-grading profile due to the increased deposition rates was observed. In Figure 3.8 we compare the band gap normalized I-V parameters as a function of the Cu/(In+Ga) ratio for devices with and without Ga-grading, where the CIGS layers is grown at 15 minutes.

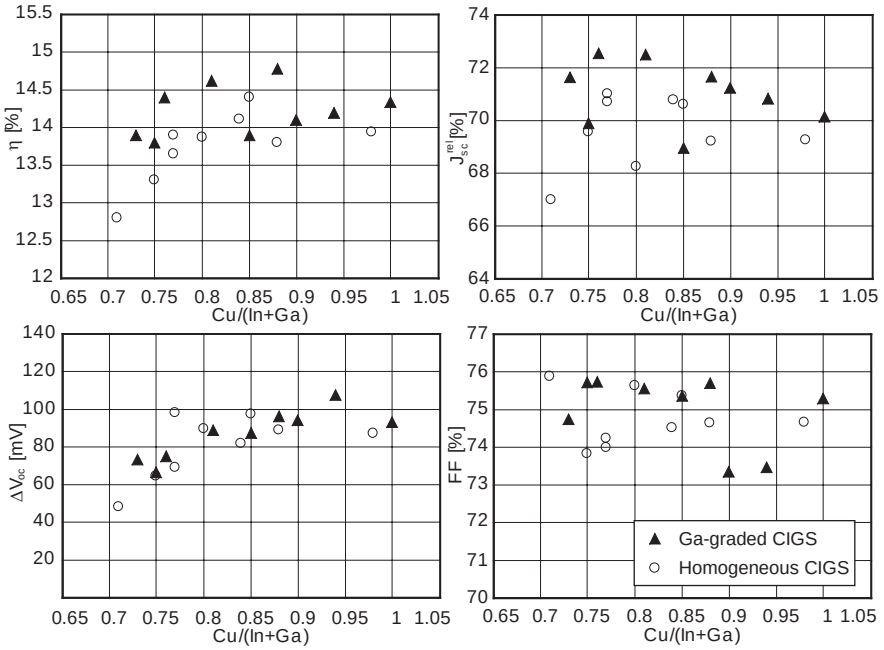


Figure 3.8. The η, FF, ΔV_{oc} and J_{sc}^{rel} as a function of the Cu/(In+Ga) ratio for devices with and without a Ga-graded CIGS layer fabricated at 15 minutes.

Also for these devices, where the CIGS layers are grown at four times higher evaporation rate than used in the baseline process, a beneficial effect of the Ga-grading is observed. In order to obtain numbers for comparison for these devices it is enough to divide them into two different categories since they are less influenced by the Cu/(In+Ga) ratio. In Table 3.2 the differences in the band gap normalized I-V parameters between devices with and without a Ga-graded CIGS layer are shown.

Table 3.2. The differences in band gap normalized I-V parameters between Ga-graded and homogeneous CIGS layers in different Cu/(In+Ga) regions. The average is the mean value of the two intervals in the table.

Cu/(In+Ga) ratio	-0.80	0.81-	Average
$\eta_{Graded} - \eta_{Homo}$	0.5	0.3	0.4 [% units]
$FF_{graded} - FF_{homo}$	1.4	0	0.7 [% units]
$J_{sc}^{rel}{}_{graded} - J_{sc}^{rel}{}_{homo}$	2.0	0.5	1.3 [% units]
$\Delta V_{oc\ (graded)} - \Delta V_{oc\ (homo)}$	-2	11	4 [mV]

As can be seen from Table 3.2 the average gain in efficiency is 0.4 % units, which is the same as for the devices with the CIGS layers grown at 60 minutes. Also at this shorter deposition time the dominant gain is seen in the J_{sc}, although some gain also is obtained in the FF. The largest gain in J_{sc} is seen for Cu/(In+Ga) ratios below 0.80, in contradiction to the previous section, where the larger gain

was obtained for higher Cu/(In+Ga) ratios. As discussed in Paper VIII, there is some additional loss mechanisms introduced at higher Cu/(In+Ga) ratios for these devices, which for example results in a wavelength independent reduction of the QE. These additional losses might overshadow some of the effects of Ga-grading.

3.3.5 The effect of Ga-grading for CIS

In Paper III the influence of Ga-grading in pure $CuInSe_2$ was investigated. CIS layers with a 0 to 1.25 μm thick CGS layer at the back were fabricated with constant evaporation rates under Cu-poor conditions. The total thickness was around 2 μm for all the layers. In the upper 250 nm a small amount of Ga was added, so that a Ga/(In+Ga) ratio of around 0.2 was obtained. No beneficial effect of this top layer could, however, be proven. In Figure 3.9a depth profiles of the Ga/(In+Ga) ratio obtained from SIMS measurements are shown and in Figure 3.9b absorbtance data as a function of wavelength are shown for some of the CIS/CGS samples.

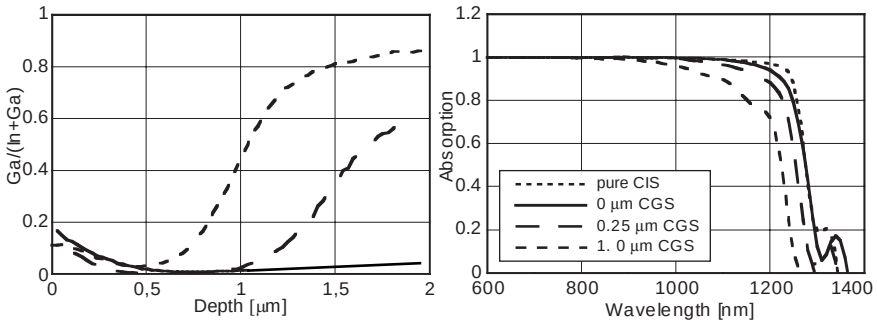


Figure 3.9.(a) SIMS depth profiles and (b) absorbtance data (compensated for reflection losses) as a function of wavelength for CIS layers with different thick CGS layers at the back. "Pure CIS" means that this layer, in contrast to the others, does not have any Ga in the front region.

In Figure 3.11a we can see that the CIS layer with a 1 μm thick CGS layer deposited at the back, has a very steep gradient of the Ga/(In+Ga) ratio. In Figure 3.11b it can also be seen that the absorbtance at long wavelengths is reduced for this CIGS layer, which corresponds to a J_{sc} reduction of around 2 mA/cm^2. The corresponding loss for the CIGS film with a 0.25 μm thick CGS layer at the back is around 0.5 mA/cm^2. A small reduction in absorption, compared to the pure CIS layer, is also seen for the film with no CGS at the back, but only a 250 nm thick layer of $Cu(In_{0.8}Ga_{0.2})Se_2$ at the front. The absorbtance data are obtained from reflectance and transmittance measurements performed on the CIS/CGS layers deposited on glass.

In Figure 3.10 the I-V parameters as a function of the CGS layer thickness are shown. These J_{sc} data are obtained from the I-V measurement and not from QE measurements, because QE measurements were not available for all the samples.

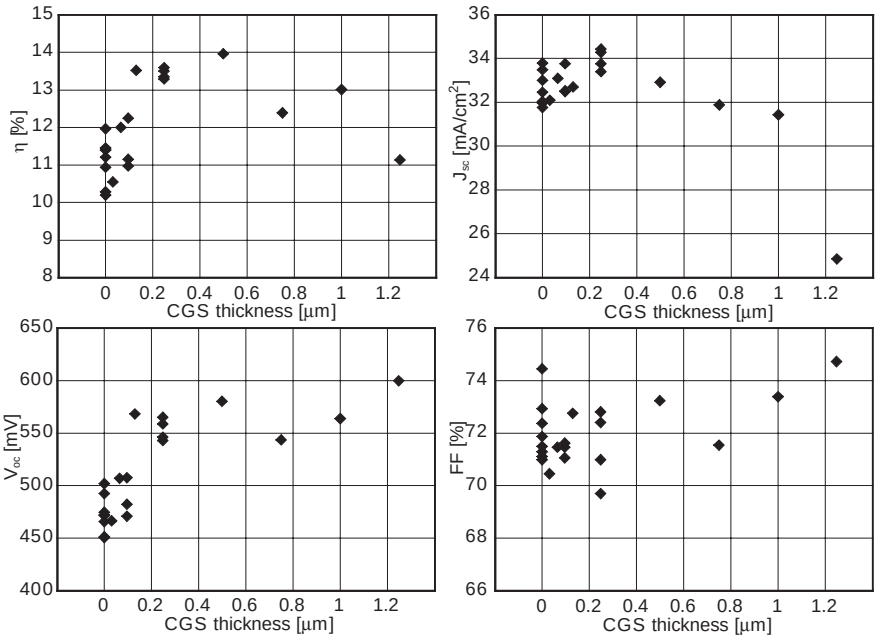


Figure 3.10. I-V parameters as a function of the CGS layer thickness at the back in devices with CIS/CGS absorber layers.

By adding an only 0.13 µm thick CGS layer at the back an improved efficiency of around 2 % units is obtained. The gain in efficiency is mainly due to an increased V_{oc}, which is around 60 mV higher for the device with a 0.25 µm thick CGS layer compared to the CIS layers without any CGS bottom layer. A small gain of the short circuit current is also obtained for CGS layers up to 0.25 µm, despite the fact that the absorbtance is reduced. When the CGS thickness is increased above 0.5 µm the performance is reduced compared to the optimal value. This is mainly because the J_{sc} starts to decrease, in accordance with the absorbtance measurements. The FF shows no correlation with the added CGS layer.

3.3.6 The effect of Ga-grading at different CIGS thicknesses

In chapter 3.1.1, we predicted that the back contact passivation would have an increased importance as the CIGS thickness was reduced. Possibly such a passivation can be obtainable by an increased Ga/(In+Ga) ratio towards the absorber backside, By comparing devices with different CIGS thicknesses, with and without Ga-grading, we should find out whether the back contact is detrimental for the device performance and if it is, whether a Ga-grading can help or not. Most of the results in this chapter are presented in Paper IV.

CIGS layers were fabricated with a thickness ranging from 1.8 down to 0.15 µm, both with and without Ga-grading. At the CIGS thickness of 0.5 µm we also performed an optimization of the Ga-gradient by trying CGS layers with different thickness. Cu-poor baseline and Cu-poor Ga-graded baseline evaporation rate profiles were used (see Chapter 2), where only the deposition time was shortened in order to obtain the thinner CIGS layers. The CGS thickness, in the Ga-graded CIGS layers, was in this study corresponding to around 5-10 % of total

thickness. In Figure 3.11 the band gap normalized I-V parameters η, ΔV_{oc}, J_{sc}^{rel} and FF are shown as a function of the CIGS thickness for devices with and without Ga-grading.

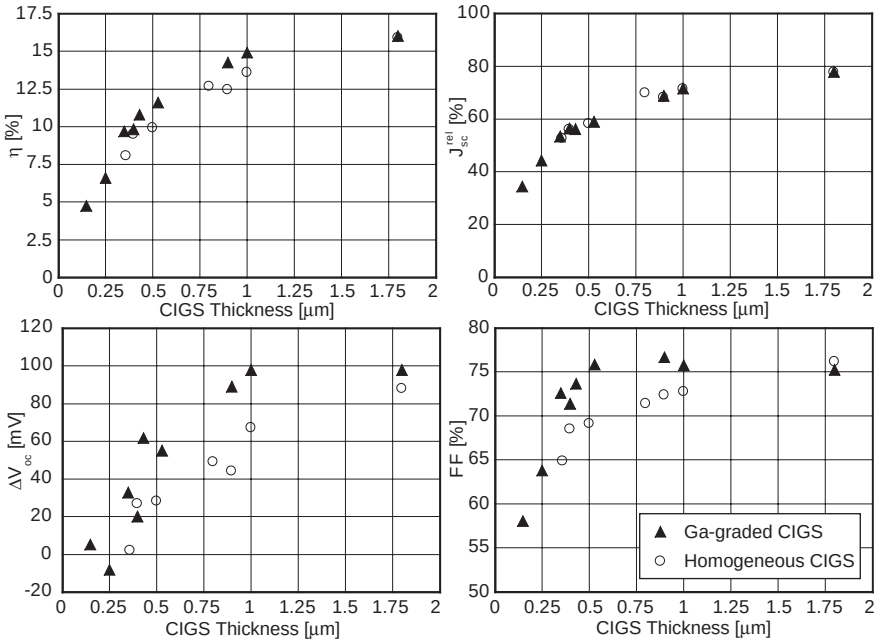


Figure 3.11. The η, FF, ΔV_{oc} and J_{sc}^{rel} versus absorber thickness for samples with (filled triangles) and without (open circles) a Ga-graded CIGS layer

The general device performance as a function of the CIGS thickness will be discussed in Chapter 4, while we focus here on the effect of Ga-grading. In Paper IV, we did not make any correction for the fact that the devices with thinner CIGS layers in general had slightly higher band gaps. Here, this is done and the conclusions are slightly different. For devices with homogeneous CIGS layers the V_{oc} is reduced by roughly 70 mV as the CIGS thickness is reduced from 1.8 µm down to 0.5 µm. Around 20 mV of this loss can be attributed to the reduction in J_{sc}, which means that the loss due to an increased recombination is about 50 mV. The corresponding loss in V_{oc} for devices with Ga-graded CIGS layers is only 20 mV. The gain in V_{oc} by using a Ga-graded CIGS layer increases as the CIGS thickness is reduced, from 10 mV at 1.8 µm to around 30 mV at 0.5 µm. A similar behavior is seen for the FF, which for devices without Ga-grading is reduced almost linearly from 76 % down to below 70 %, as the CIGS thickness is reduced from 1.8 to 0.5 µm. For the devices with a Ga-graded CIGS layer, however, the FF stays unaffected, around 75 %, as the CIGS thickness is decreased down to 0.5 µm. Concerning the J_{sc} no significant difference between devices with and with out Ga-grading was observed for these devices. The resulting gain in efficiency, due to the Ga-grading, is thus increasing with a decreased CIGS thickness.

In Figure 3.12 the ΔV_{oc} and FF for devices with a 0.5 µm thick CIGS layer and an additional CGS layer at the back are shown as a function of the CGS layer thickness.

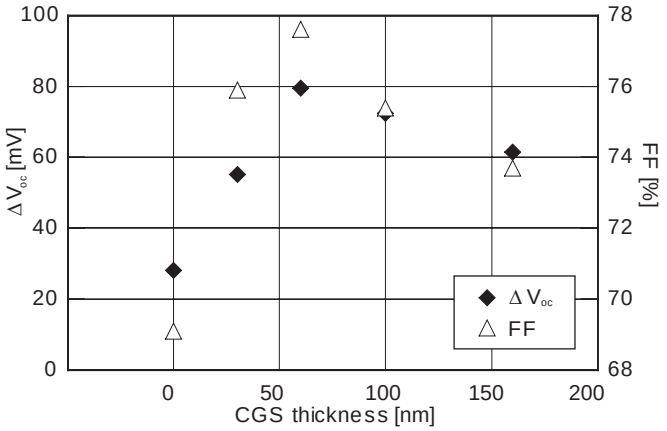


Figure 3.12. Voc and FF versus CGS bottom layer thickness for devices with a CIGS thickness of 0.5 µm.

The 30 nm additional CGS layer corresponds to around 6 % of the total absorber thickness, which was the CGS thickness used for the devices in Figure 3.11. By increasing the CGS thickness to 60 nm an additional gain in V_{oc} of around 20 mV and in FF of close to 2 % units is obtained. From figure 3.13 we stated that the loss in V_{oc} for the device with the 0,5 µm thick Ga-graded CIGS layer was around 20 mV compared to devices with standard thickness of the CIGS layers. This means that, after an optimization of the Ga-grading, devices with a 0.5 µm thick absorber layer can obtain V_{oc} and FF as high as for standard devices. The gain compared to homogenous CIGS layers for this device is around 50 mV in V_{oc} and 8 % units in FF. Increasing the CGS thickness further, up to 160 nm, the device performance is slightly reduced again. This means that the Ga-grading profile used for the devices in Figure 3.11 was close to optimum but a slight further improvement is obtained by increasing the CGS thickness to around 10-15 % of the CIGS thickness. No gain in J_{sc} correlated to the Ga-grading was observed for these devices.

3.5 Discussion and Conclusions

For devices with 1.5-2 µm thick CIGS layers grown in a Ga-graded baseline process, the average gain in efficiency, compared to CIGS layers grown in a normal baseline process, is about 0.4 % units. The gain is due to an improved short circuit current (J_{sc}) which is increased due to an enhanced QE response at wavelengths above 800 nm. In average the improvement in J_{sc} is around 0.5 mA/cm^2, which is in good agreement with the gain obtained in a number of simulations[31, 50, 53]. All these results indicate that the improved carrier collection is due to the additional electric field obtained by the Ga-grading, as discussed in point 2 - Chapter 3.1.1. The fact that V_{oc} and FF are not significantly influenced by the Ga-gradient could be explained by that the recombination current, limiting

these parameters, is strongly dominated by recombination in the SCR (c.f. Chapter 2.3).

A significantly larger beneficial effect of the Ga-grading is obtained for thin CIGS layers. The gain in efficiency due to the Ga-grading is increased as the absorber thickness is reduced (at least for CIGS thickness down to 0.5 μm). An increase in both FF and V_{oc}, which can be correlated to a reduced saturation current, is the reason for the gain in efficiency. At a CIGS thickness of 0.5 μm the improvement in efficiency, by using a Ga-graded CIGS layer, is around 2.5 % units and the obtained values of V_{oc} and FF reach the same level as for devices with standard thick CIGS layers. These observations are all in agreement with that the Ga-grading passivates the back contact, which becomes increasingly detrimental for the device performance as the CIGS thickness is reduced. The theoretically predicted gain in V_{oc}, from a reduced back contact recombination in point 1-Chapter 3.1.1 is also in agreement with the obtained results. Since we did not observe any increased FF or V_{oc} for devices with 1.5-2 μm thick Ga-graded CIGS layers it indicates that the CIGS/Mo interface does not play a significant role in these devices. For devices with thinner CIGS layers no improvement in J_{sc}, related to the Ga-grading was observed. This could be understood by that in thin CIGS layers the relative absorption loss due to the Ga-grading is larger, and the need for field assisted carrier collection is smaller than in absorber layers with standard thicknesses.

Devices with CIGS layers grown at an elevated deposition rate, exhibit a similar gain in efficiency due to the Ga-grading as devices with CIGS layers grown at 60 minutes. Also here the main part of the gain is due to an improved J_{sc}, but a small gain in FF is also obtained.

We, as well as others, have observed a large beneficial effect of adding Ga in pure CIS layers. By adding only 0.13 μm CGS at the back of a 2 μm thick CIS layer, we obtained an around 2 % units gain in efficiency. The suggested explanation for this observation was in Paper III a reduced back contact recombination. Due to a number of reasons, we do not longer find this explanation very probable. First of all this interpretation does not fit to the other observations and conclusions made above. It also requires a bulk diffusion length of around 4 μm, which is longer than normally observed. We instead suggest that the introduction of gallium itself is the main reason for the observed improvement in performance. In Wei *et al.*[64] a number of beneficial effects obtained by introducing gallium in CIS are summarized. For example the introduction of gallium leads to a larger domain for stoichiometric CIGS (α-phase) in the phase diagram, potentially leading to a generally improved material quality. At our lab we have also observed an improved device performance for CIS layers by adding very small homogeneous amounts of Ga.

Concerning the optimal Ga-grading profile our results suggest that, independent of the CIGS thickness, deposition rate and composition, the optimal normal Ga-profile is obtained by starting the deposition with a CGS layer corresponding to 10-15 % of the total absorber thickness. Such a layer results in a Ga-gradient starting approximately 1/3 into the CIGS layer and reaches a Ga/(In+Ga) ratio of around 0.7 at the back contact. By increasing the initial CGS thickness further a reduced device performance was obtained. This could be correlated both larger absorption

related losses and to an increase in the potentially detrimental material related effects mentioned in chapter 3.1.1- point 4.

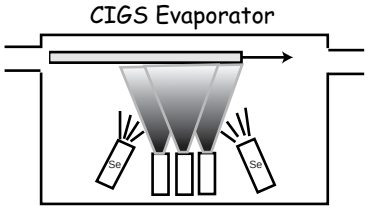
In this work we have focused on the normal Ga-grading profile, and in the experiments where we have used a double grading profile, no additional beneficial effect was observed. Despite the results from many simulations showing a superior device performance for a double grading profile compared to a normal grading, there are no clear experimental results showing this in the literature. As mentioned above, the CIGS layer in the world record device has a double grading profile, which proves that high performance devices can be obtained with such a profile. But as shown by Contreras *et al.*[59] the three-stage process results in around 1 % unit higher efficiency devices compared to devices where CIGS layers have a similar double graded profile, but grown in a single stage process. This indicates that it is the three-stage process in it self that is the origin of the high performance and not necessarily the double Ga-grading profile.

Concerning the beneficial effect of Ga-grading we conclude:

- For devices with a standard thick CIGS layer (1.5-2 μm) with a Ga/(In+Ga) ratio between 0.25-0.5, a Cu/(In+Ga) ratio between 0.7 and 1 and a deposition time from 60 down to 15 minutes the efficiency gain with a normal Ga-grading profile is in the order of 0.5 % units. The main part of the gain is due to an improved carrier collection at long wavelengths due to the additional effective electric field obtained from the increased Ga/(In+Ga) ratio towards the back contact. No significant gain in V_{oc} or FF related to the Ga-grading is obtained under these conditions.
- By reducing the CIGS thickness, the beneficial effect of Ga-grading is increased. At an absorber thickness of 0.5 μm the gain in efficiency is around 2.5 % units due to an increased FF and $V_{oc,}$ which becomes comparable to those obtained for standard devices. The increased gain at thinner CIGS layers is due to a passivation of the CIGS back contact, which becomes increasingly detrimental for the device performance as the CIGS thickness is reduced.
- No additional gain in performance due to an increased Ga/(In+Ga) ratio in the front part of the CIGS layer can be concluded.

4 Next generation CIGS layers

From an application point of view, the two most important numbers for a solar cell module are the module efficiency and the module production cost. Among the five different layers within the device structure, the CIGS film is the layer associated with the highest production cost. A large capital cost for the deposition equipment, in combination with a relatively long deposition time leads to the high production cost for the CIGS layer. The need for lowering the production cost for the next generation CIGS layers can be illustrated by the following example:
In Figure 4.1 a sketch of a CIGS in-line deposition system is shown together with an equation for estimating the yearly production from this CIGS evaporator.



$$\text{Yearly production} = \text{Efficiency} \cdot \text{Yield} \cdot \text{"Up-time"} \cdot \frac{\text{Deposition area}}{\text{Deposition time}}$$

Figure 4.1. Sketch of a CIGS in-line deposition system and an equation for estimating the yearly production (in W_p) from such a system.

Standard values of these parameters today are: module efficiency= ~10 %, deposition area= ~1 m^2, deposition time=30 min, up time=5700 h (three shift operation) and by assuming a yield of 100 % we end up with a yearly production of about 1 MW_p. Assume that we would like to produce the complete modules for 1 $/W and that the production of the CIGS layer not may exceed 10 % of the total production cost. The yearly available money, for both capital and operational costs of the CIGS production then becomes around $ 100 000. Only the salaries for two full time workers will cover this amount of money, clearly pointing out the need to either develop a low-cost deposition equipment and/or increase the production from an "expensive" deposition system.

Beside the deposition methods, described in Chapter 2 (co-evaporation and selenization), there are a number of alternative ways of depositing the CIGS layer. Electro-deposition is one example of a potentially cheaper method. CIGS films resulting in 10 % efficiency small area devices have been fabricated with this method[65], but many things remains to be improved before this process can be scaled up and produce large, high efficiency modules at a lower cost. We will here instead focus on how we can increase the production from a co-evaporation system.

Among the parameters given in Figure 4.1, our estimate is that the deposition-time hosts the largest potential for improvement. Increasing the efficiency would be even more valuable, but the effort put into this is already very high and the possibility for a substantial improvement is limited. Enlarging the deposition area should be possible, but this will also make the deposition system more expensive.

This motivated us to investigate the potential for reducing the deposition time of the CIGS layer as a fundamental parameter for lowering the cost. The deposition time is determined by the final thickness of the CIGS layer and the deposition rate used during deposition, according to Equation 4.2:

$$Deposition\ time = \frac{CIGS\ thickness}{Deposition\ rate} \tag{4.2}$$

In the following we will show that by decreasing the CIGS thickness and raising the deposition rate it is possible to increase the yearly production, from the CIGS deposition system in Figure 4.1 by up to 30 times, with only a marginally reduced module efficiency.

4.1 Reduced CIGS thickness

Decreasing the thickness of the CIGS layer leads, in addition to a reduced deposition time, to a lower material consumption. A reduction of material usage is particularly important for indium and gallium since the supply of these metals might become an issue if CIGS thin film solar cells will be produced in very large volumes (~70 GW_p/year).[66] In the following we discuss the effects on the device performance when the CIGS thickness is reduced, and the possibilities to improve the performance for devices with thin CIGS layers. Most of the results are presented in Papers IV and IX.

4.1.1 Performance as a function of CIGS thickness

The standard thickness of the $Cu(In,Ga)Se_2$ layer used in the industry is around 2 µm[67, 68]. A reduction of this absorber thickness has advantages as mentioned above, however, it is also associated with a number of problems:

- *Reduced absorption*: Although the absorption coefficient is high for the CIGS material, a decreased thickness will reduce the absorption and thereby also the J_{sc}.
- *Increased risk for shunting*: In a previous study by T. Negami *et al.*[69] an increased shunting was observed as the CIGS thickness was reduced down to around 0.5 µm, which resulted in strongly decreased performance.
- *Increased influence of the back contact*: As the CIGS thickness is reduced, the risk for back contact recombination increases.
- *Reduced long-term durability:* Possibly a thinner CIGS layer will reduce the lifetime of the solar cell. This could for example happen if the corrosion of the CIGS layer itself is critical for the solar cell lifetime.
- *Reduced material quality*: Thinner CIGS layers have smaller grains, which for example could decrease the minority carrier lifetime.

Concerning the first point, it is clear that the J_{sc} will decrease with a reduced absorber thickness, but the question is how much for a specific CIGS thickness? Regarding the second point, our baseline devices are relatively smooth (rms ~ 100 nm), so the risk for roughness related shunting should be small. In order to investigate these issues, solar cells with a CIGS thickness of 1.8 µm down to 0.15 µm were fabricated. The different thicknesses were obtained only by

shortening the deposition time, from 60 minutes (1.8 μm) down to 8 minutes (0.15 μm), keeping the deposition rate unchanged. At the different thicknesses, CIGS layers were fabricated with Cu-poor baseline evaporation rates (see Chapter 2.2.3) with and without Ga-grading.

In Figure 3.11 (Chapter 3), the η, ΔV_{oc}, J_{sc}^{rel} and FF were shown as a function of the CIGS thickness. When the CIGS thickness is reduced to around 1 μm the loss in performance is around 1 % unit. By reducing the CIGS thickness further the performance reduction is more pronounced, and at a CIGS thickness of 0.5 μm the efficiency loss is around 4 % units. As pointed out in chapter 3, for CIGS thicknesses above 0.5 μm the loss in FF and V_{oc} could almost completely be avoided by the use a Ga-graded CIGS layer, making the reduction in J_{sc} alone responsible for the obtained performance loss. In order to find whether the loss in the short circuit current only is related to the expected reduction in absorption, we need to determine the amount of light absorbed in CIGS layers of different thickness. As the optical constants *n* and *k* were not well known for all the layers in the device structure at this time, we based our calculations on reflectance and transmittance measurements performed on CIGS deposited directly on glass (see Paper IV). A control measurement was performed showing that the optical constants of CIGS deposited on glass are the same as for CIGS deposited on Mo. In Figure 4.2a the calculated amount of light absorbed in the CIGS layer and the QE measurements are shown for devices with 1.8, 0.8 and 0.4 μm thick CIGS layers. In Figure 4.2b the J_{sc}^{rel} as a function of the CIGS thickness is shown, where the dotted line corresponds to the maximal J_{sc}^{rel}, obtained if all photogenerated carriers in the CIGS layer, would contribute to the short circuit current, i.e. the recombination losses are zero.

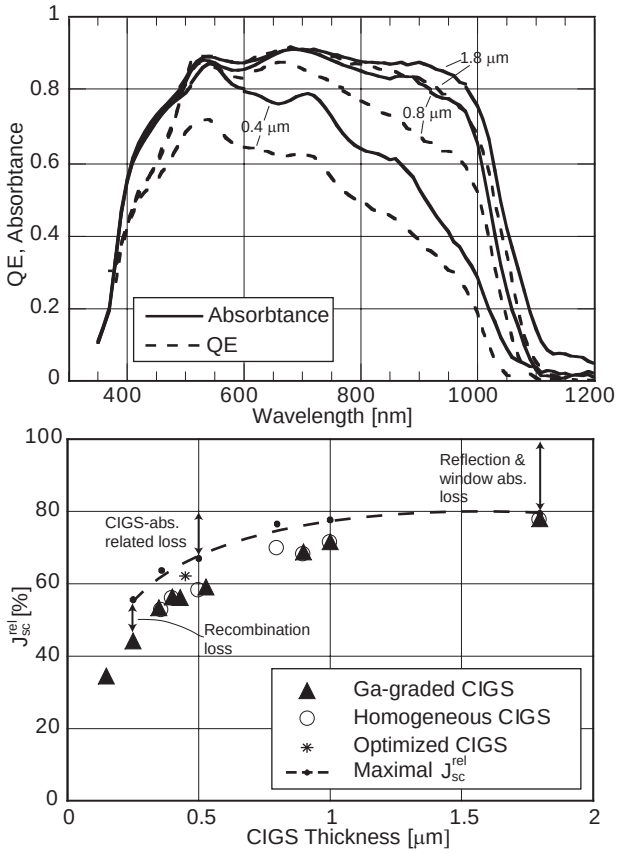


Figure 4.2. (a) Calculated absorbtance spectra and the corresponding QE measurements for three CIGS thicknesses: 1.8, 0.8 and 0.4 μm. (b) J_{sc}^{rel} as a function of the CIGS thickness. The dotted line corresponds to a J_{sc}^{rel} where all photoelectrons generated in the CIGS layer contribute to the short circuit current (Rec.=0).

At a CIGS thickness of 1.8 μm we can see, in both Figure 4.1a and b that close to all photogenerated electrons are contributing to the short circuit current. It can also be seen that the optical losses, reflection from the complete device and absorption in the window and buffer layers, at a CIGS thickness of 1.8 μm are around 20 %. By reducing the CIGS thickness to 0.8 μm, the absorption related loss in the CIGS layer only corresponds to a reduced J_{sc} of around 1 mA/cm^2, but the actually obtained decrease is around 4 mA/cm^2. In Figure 4.1a, we can see the explanation for this additional loss, the gap between the QE and the absorbtance curve is significantly increased for wavelengths above 700 nm. This means that fewer of the electrons absorbing this long wavelength light, i.e. further into the CIGS layer, are collected. As the CIGS thickness is reduced down to around 0.4 μm, the absorption related loss is significantly increased and corresponds to a loss in J_{sc} around 6 mA/cm^2. The actual loss at this thickness is around 10 mA/cm^2, and we can see that the deviation between the QE and absorbtance curve, in this case, not only is limited to longer wavelengths. Already at 500 nm the QE is

significantly lower than the absorbtance curve. This means that at a CIGS thickness of around 0.5 μm the losses in current due to incomplete carrier collection are responsible for almost half of the obtained loss in performance and at a CIGS thickness around 1 μm, this loss is clearly dominating. If these, non-absorption related losses could be reduced, a significantly improved device performance for devices with thin absorber layers would be obtained.

Concerning the losses in QE at long wavelengths, we know from Paper VIII that the carrier collection in this region is dependent on the Cu/(In+Ga) ratio. The CIGS layers in Figure 4.1b have a Cu/(In+Ga) ratio of around 0.8. In Figure 4.3 the QE for the device with a 0.5 μm thick CIGS layer in Figure 4.2 is compared with the QE for a device with a similar thickness but a more optimized Cu/(In+Ga) ratio of 0.9. As comparison the calculated absorbtance in a 0.5 μm thick CIGS layer is also shown.

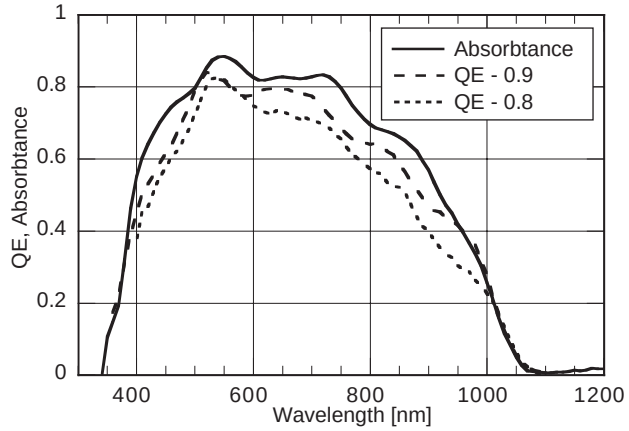


Figure 4.3. QE for devices with a Cu/(In+Ga) ratio of 0.8 and 0.9 respectively, and the calculated absorbtance in a 0.5 μm thick CIGS layer.

Here it is evident that the response in the QE is improved significantly by an increased Cu/(In+Ga) ratio. The J_{sc}^{rel} for this device is also illustrated in Figure 4.1b, with a star, and we can see that the gap between the maximum current and the measured current for this device is significantly decreased. The efficiency of this device with a CIGS thickness of 0.45 μm is 13.4 %, where the absorption related loss in J_{sc} corresponds to around 5 mA/cm^2, and the additional recombination loss only around 1.5 mA/cm^2. In Figure 4.3, we can also see that the remaining loss in J_{sc} is due to a lower value of the QE over the whole wavelength regime. This loss, which also appears at short wavelengths, indicates that photoelectrons generated within the SCR experience a non-negligible recombination.

In a more recent study, performed by Malm *et al.* (not yet published), I-V(T) measurements were performed on devices with different CIGS thickness. Here indications were found that the wavelength independent reduction of the QE, for devices with thin CIGS layers, is related to recombination at the CIGS/CdS interface. In the same study, accelerated lifetime tests were performed by putting devices with homogeneous CIGS layers with different thicknesses into a damp-heat chamber. During several hours under damp-heat conditions, a slightly increased QE level, for the devices with thin CIGS layers, was observed. It was

also found that he devices with thin CIGS layers, actually were less degraded after 1000 h under damp-heat conditions compared to devices with standard thick CIGS layers. This is an important result indicating that no reduced lifetime is expected due to a reduced CIGS thickness.

In summary, we have shown that devices with CIGS layers, down to 0.5 μm thickness, can be fabricated with almost exclusively absorption related losses in J_{sc}. At a CIGS thickness of 1 μm this loss is around 1 mA/cm^2 and at a CIGS thickness of 0.5 μm it is around 5 mA/cm^2 for a CIGS layer with a band gap of 1.16 eV.

4.1.2 Light trapping

The results from the previous chapter motivate the investigation if the absorption can be enhanced by some kind of light trapping scheme in devices with thin CIGS layers. The basic concept of light trapping is to increase the length of the path by which the light travels through the absorbing material. This can be obtained by three main methods: increased back contact reflection, diffusive back contact reflection and diffusive transmission at the entrance to the absorber layer. In both crystalline and amorphous Si solar cells light trapping schemes are regularly used to enhance the light absorption, see for example Cotter *et al.*[70] and Rech *et al.*[71]. For weakly absorbed light in silicon the path length can be enhanced up to 50 times.[46] Due to the high absorption coefficient of the CIGS material, little work has been made on investigating light trapping schemes in this kind of solar cells. But as pointed out in the previous section, when the CIGS layer thickness is reduced down to around 0.5 μm, there are significant losses in performance, which mainly are identified as incomplete absorption. This motivates the investigation of the light-trapping potential also for CIGS thin film solar cells.

In Paper IX the potential of light trapping in CIGS thin film solar cells has been investigated theoretically. An experimental attempt was also performed, in . Two cases are simulated, perfectly specular interfaces and Lambertian scattering at both front and backside of the absorber. As the CIGS/Mo interface has a relatively low reflectance, 20-40 %, in the wavelength regime of 800-1000 nm there is room for improvement just by improving this back contact reflectance. The limitation of such an approach is that the path length at the best case can be increased by a factor of two. From an optical point of view, metals like Ag and Al are the best choices for a back contact. By replacing the optical constants of Mo by those of Ag, in the optical simulations, the gain in current is around 2 mA/cm^2 for a 0.5 μm CIGS layer (Ga/(In+Ga)=0.42). The corresponding gain for the scattering case is around 3.5 mA/ cm^2, which would bring up the current level close to that of a standard thick CIGS layer. However, as pointed out in Chapter 2, the back contact layer must also be inert during absorber growth, have low recombination for minority electrons and provide good ohmic contact for majority holes. The metals like Ag and Al do unfortunately not fulfill these criteria. Orgassa *et al.*[63] investigated a number of alternative back contacts (Cr, Ta, Nb, V, Ti, Mn, W), of which most are expected to be optically superior to Mo. However, the optical effect in measured reflectance from CIGS/back contact structures was to a large extent shadowed by differences in surface scattering, and due to electrical losses no significant improvement in J_{sc} could be observed. Another approach for a-Si cells[72], is to add an intermediate transparent conductive oxide (TCO) layer between the CIGS layer and, for example, a Ag back contact. In this way the desired optical effects of the Ag film is kept, and the other needed criteria are fulfilled by the

TCO. Nakada *et al.*[73] recently published a Paper showing that ITO could potentially have the right properties for such an intermediate layer in CIGS based thin film solar cells. This needs further investigation.

In order to experimentally verify the light-trapping concept of an increased back contact reflectance we chose TiN, a stable compound with free-electron behavior and optically superior to Mo. In figure 4.4a a SEM picture shows the cross sectional view of a device with an around 100 nm thick TiN layer between the Mo and the 0.45 μm thick CIGS layer. In figure 4.3b the QE is shown for the devices with and without this TiN layer.

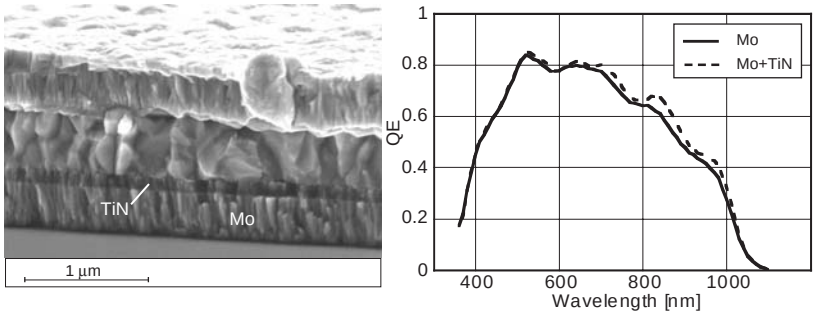


Figure 4.4. (a) SEM micrograph of a device with a around 100 nm thick TiN layer between the Mo layer and the 0.45 μm thick CIGS layer. (b) QEs for devices with and without a TiN layer.

For the device with the TiN layer an enhanced QE response and an increase in optical interference are obtained for wavelengths above 700 nm. The improvement in QE corresponds to a gain in J_{sc} of 0.6 mA/cm^2, which is in good agreement with the theoretical expectations according to the calculations in Paper IX. However, the efficiency of the device with the TiN layer is still slightly lower than without the TiN layer, 13.1 % instead of 13.4 %, due to slightly lower V_{oc} and FF.

A larger potential improvement was predicted for the scattering case. We made a first experimental attempt by etching the ZnO:Al layer in diluted HCl, resulting in a rougher front contact. This method is used for a-Si solar cells[74]. Figure 4.5a shows a cross sectional view of a device with an etched ZnO:Al layer and in Figure 4.5b the QE measurement before and after the etch is shown.

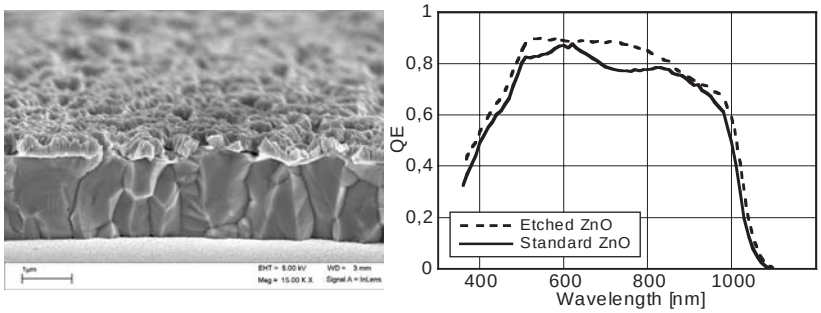


Figure 4.5. SEM image of a CIGS solar cell etched in diluted HCl resulting in a rough ZnO surface and QE spectra before and after etching.

A significant gain in QE is obtained due to the etching step, however the dominated part of the gain is obtained for wavelengths shorter than 900 nm As observed also for silicon thin film solar cells, the effect of an etched ZnO structure like this is mainly due to a reduced light reflectance, similar to that obtained by an antireflective coating.[75] A small additional gain at longer wavelengths was occasionally observed (see Figure 4.5). Such a result could, however, not be obtained reproducibly. From reflectance and transmittance measurements performed on etched ZnO:Al layers deposited on glass, it was found that the scattering of light with a wavelength above 800 nm was rather low. Apparently the roughness obtained from the HCl etch is not large enough to scatter light with such a wavelength. Other possibilities for obtaining scattered light in the CIGS film would be to use a CIGS process, which by itself results in a rougher surface. Depositing a highly reflective back contact onto a rough substrate/film could be another alternative.

4.2 Increased deposition rate

A basic limitation of the deposition rate for high quality CIGS films is the formation time of the CIGS material. Based on earlier investigations where the reaction analysis and growth kinetics for CIS grown by selenization were investigated, Shafarman *et al.*[76] *e*stimated the formation time of CIS, at a substrate temperature of 500°C, to be in the order of 10 minutes. In contrast to the selenization process, the atoms in the co-evaporation process are put close to their final positions. This could potentially lead to a shorter formation time. Kessler *et al.*[77] in 1996 showed this potential by depositing a CIGS layer in 10 minutes that resulted in a 13.7 % efficient device. In order to further investigate how the device performance is affected by the CIGS deposition rate, we fabricated and analyzed CIGS layers grown at various deposition rates (see Paper V). Since also the compositional tolerance is an important characteristic for the CIGS process, the performance dependency of the Cu/(In+Ga) ratio was investigated for devices with CIGS layers deposited at both a normal and a high deposition rate (see Paper VIII). From the results presented in these papers, I will, in the following discuss how and why the device performance and the process window are affected by an increased deposition rate of the CIGS layer.

CIGS layers were fabricated with a deposition time from 60 down to 3.75 minutes. The deposition rate was increased correspondingly so that a final thickness of 1.8-2 μm was obtained. Baseline evaporation rate profiles, with and without Ga-grading, were used. This means that the average deposition rate is obtained by dividing the CIGS thickness by deposition time, but the actual rate will change during the deposition from lower in the beginning and the end and higher in the middle (according to Figure 2.6). In figure 4.6, SEM pictures of CIGS layers deposited at 30, 15, 7.5 and 3.75 minutes are shown.

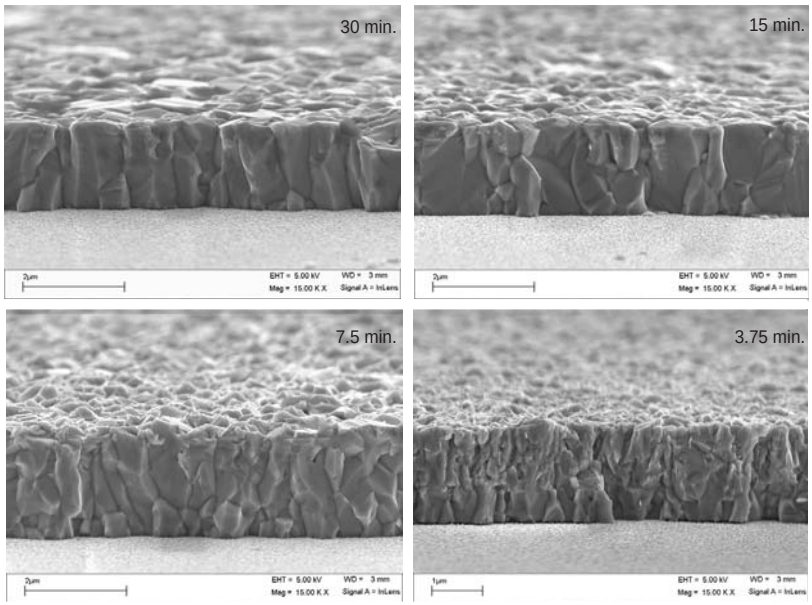


Figure 4.6. SEM pictures of homogeneous CIGS layers grown at 30, 15, 7.5 and 3.75 minutes.

No significant change of the morphology is observed when decreasing the deposition time from 30 down to 15 minutes. At a deposition time of 7.5 minutes the grain size is reduced to around 0.5 μm in width and the grains are also not extending all the way from bottom to top as they were for the CIGS layers deposited at 30 minutes. Apparently the increased deposition rate is not affecting the morphology of the CIGS material significantly until it is increased 8 times, compared to the rate used in a standard baseline deposition. By doubling the deposition rate again, resulting in a deposition time of 3.75 minutes, the grain size is further reduced to approximately 100 nm. In order to analyze the material quality of these layers further, we studied the cross section in a TEM. In Figure 4.7 TEM pictures of CIGS layers deposited at 30 and 3.75 minutes are shown.

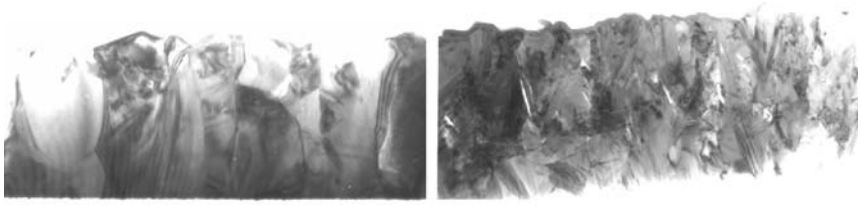


Figure 4.7. TEM pictures of homogenous CIGS layers fabricated at 30 minutes (left) and 3.75 minutes (right) respectively.

From the TEM images it is obvious that the layer deposited at 3.75 minutes contains significantly more defects and even voids. From XRD measurements it was found that the ratio of the intensity between the (112) and the (220, 204) peaks is decreasing as the deposition rate is increased. The ratio decreases from 40,

indicating a strong (112) preferred orientation at 30 minutes deposition time, down to around 4 which roughly corresponds to random orientation at 7.5 and 3.75 minutes deposition time. Even if the grains are small, defect rich and randomly oriented for the CIGS layer grown at 3.75 minutes, a relatively compact chalcopyrite structured $Cu(In,Ga)Se_2$ layer is formed during this very short time.

The next question is how the increased deposition rate affects the device performance. In Figure 4.8, the band gap normalized I-V parameters for the samples, with highest performance at each deposition time, are shown. All the CIGS layers, except the film deposited at 3.75 minutes, have an increased Ga/(In+Ga) ratio towards the back contact.

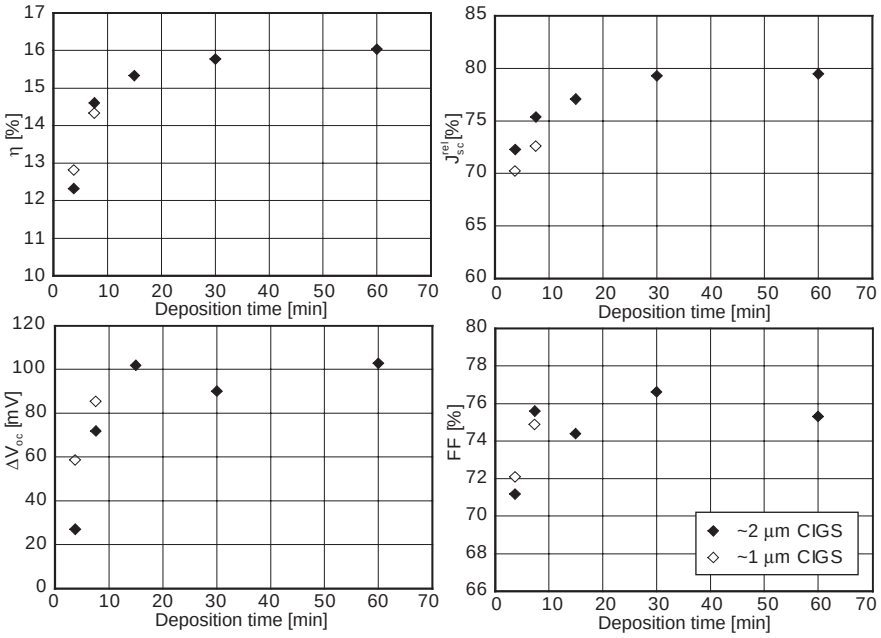


Figure 4.8. Band gap normalized I-V parameters η, FF, ΔV_{oc} and J_{sc}^{rel} versus deposition time.

No significant difference in performance between the devices with the CIGS layers deposited at 60 and 30 minutes is observed. By decreasing the deposition time from 30 down to 15 minutes, a small reduction in efficiency is obtained mainly due to a reduced J_{sc}^{rel}. At 7.5 minutes a further reduction of J_{sc}^{rel} is obtained, and also a small reduction in V_{oc}, but despite that the deposition time is reduced 8 times the efficiency is as high as 14.7 %. This is a very promising result showing that the deposition time of the CIGS layer can be reduced significantly, while maintaining a high device performance. For the CIGS layer fabricated at the extremely short time of 3.75 minutes the device still has an efficiency of 12.3 %, which is quite remarkable considering the appearance in the film in the TEM picture. The losses are here seen in all I-V parameters, where the decrease in V_{oc} is around 70 mV, in FF around 4 % units and in J_{sc}^{rel} around 7 % units (corresponds to 3 mA/cm^2) compared to a device with a CIGS layer grown at 60 minutes.

In the previous chapter we observed that the performance reduction by decreasing the CIGS thickness from 1.8 down to around 1 μm is about 1 % unit. This means that for a given deposition time, it may be advantageous to reduce the thickness and thereby lower the deposition rate, rather than to use a high deposition rate at maintained thickness. This motivated us to fabricate a 1 μm CIGS layer at 3.75 and 7.5 minutes, which thereby will be deposited with the same deposition rate as the 2 μm CIGS layer fabricated at 7.5 and 15 minutes respectively. In Figure 4.8, the open dimond illustrates the performance of these devices. For the device where the CIGS layer is deposited at 7.5 minutes the efficiency is slightly lower for the 1 μm sample. For the device where the CIGS layer is deposited at 3.75 minutes the efficiency is, however, improved for the device with the thinner CIGS layer, from 12.3 to 12.8 %. As expected the V_{oc} has increased and the J_{sc}^{rel} is reduced for both samples with a 1 μm CIGS layer. The efficiency of the device with the CIGS layer deposited at 3.75 minutes can most probably be further improved by the use of a Ga-graded CIGS layer, but this remains to be shown.

Above we have seen that the dominating reason for the efficiency loss, as the deposition times is reduced down to 7.5 minutes, is a decreased short circuit current. This was not the conclusion in Paper V, since no correction was made related to that the CIGS layers had slightly different Ga/(In+Ga) ratios. Now, why is the short circuit current lower for devices where the CIGS layer is deposited at a higher rate?

Either the optical losses or the electrical losses are higher for the devices where the CIGS layer is grown at a higher deposition rate. From reflectance and transmittance measurements on CIGS grown at 15 and 60 minutes no difference in absorbtance was found, which means that the amount of photogenerated carriers are the same. As stated earlier, the carrier collection is sensitive to the Cu/(In+Ga) ratio. In Paper VIII the performance as a function of the Cu/(In+Ga) ratio was compared for CIGS layers deposited at 60 and 15 minutes and also here the main difference was seen in the J_{sc}. At Cu/(In+Ga) ratios below 0.8 similar J_{sc}'s are obtained for devices with CIGS layers grown at 15 and 60 minutes. But as the Cu/(In+Ga) ratio is increased, the J_{sc} is much more improved for 60 minutes CIGS devices than for the 15 minutes CIGS devices. In Figure 4.9, the QE for devices with CIGS layers grown at 15 minutes with different Cu/(In+Ga) ratios are shown together with the QE for a device with a CIGS layer grown at 60 minutes and a Cu/(In+Ga) ratio of 0.95 (without Ga-grading).

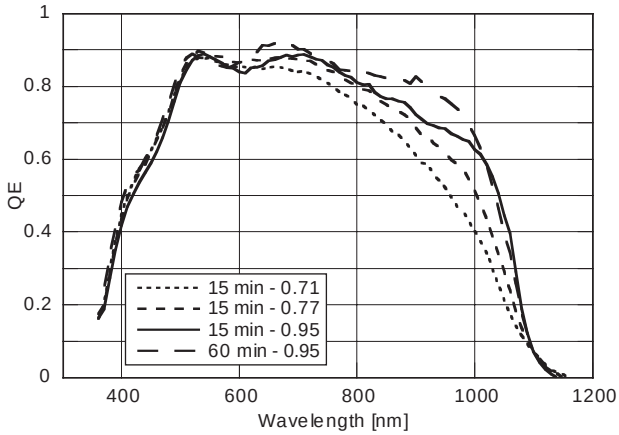


Figure 4.9. QE for different devices. CIGS growth time and Cu/(In+Ga) ratio according to the insert.

As can be seen, the carrier collection at long wavelengths is improved with an increased Cu/(In+Ga) ratio for the 15 minutes CIGS layers. However, by comparison with the QE for a 60 minutes device with an optimized Cu/(In+Ga) ratio, we see that the carrier collection, even for the best 15 minutes device, is significantly lower between 800 and 1000 nm. We have already excluded the absorption as the reason for this observation. Other parameters that are influencing the level of the QE in this region are the diffusion length, back contact recombination and the width of the SCR. In Chapter 3 we argued that the back contact recombination has little influence on the device performance as long as the diffusion length is shorter than the CIGS thickness, which is reasonable to assume in this case. Concerning the width of the SCR, we observe an increased conductivity of the CIGS film with increased Cu/(In+Ga) ratio, which indicates increased doping and thereby a decreased SCR width, rather the than opposite. Further investigations and simulations are needed in order to investigate whether a changed diffusion length can explain the variations of the QEs in Figure 4.9.

4.3 Discussion and Conclusions

We have above shown that the potential for reducing the deposition time, by a reduced CIGS thickness and an increased evaporation rate is very large. In Table 4.1 an estimation of the potential increase in production from one CIGS evaporator summarizes these results.

Table 4.1. Estimation of potential increase in production from one CIGS evaporator.

	Deposition time	CIGS thickness	Efficiency	Production Capacity
Today	30 min	2 µm	12 %	1 MW
Tomorrow	5 min	1 µm	11 %	6 MW
Future	1 min	0.5 µm	11 %	30 MW

As discussed earlier, with state of the art parameters, the total production could become around 1 MW for a given size of a CIGS deposition system. In the

previous two chapters we have seen that by increasing the deposition rate so that a 2 μm thick CIGS film is deposited in 10 minutes, the resulting loss in device performance is around 1 % units. The pure absorption related losses by reducing the CIGS thickness to 1 μm are very small, so with some additional optimization it should be possible to fabricate a 1 μm thick CIGS layer in 5 minutes, resulting in an efficiency which is only 1 % unit lower than the efficiencies obtained for the standard devices of today. That would lead to a 5-6 times increased production! In a longer perspective, it should be possible to fabricate a device with a 0.5 μm CIGS layer deposited at 1 minute yielding a similar performance. The deposition rate of such a CIGS layer is similar to that used for depositing the 2 μm thick CIGS layer at 3.75 minutes. In order to obtain such a high performance device at this deposition time, we need to reduce the non-absorption related losses in the QE further, find a beneficial light trapping scheme and also marginally improve the device performance at high deposition rates.

There are still many things to investigate which potentially could improve the performance of devices with thin CIGS layers fast grown. For example a post heat treatment of the CIGS layer, in order to provide more energy to the formation of the CIGS film, could be beneficial. We have also seen some indications that the importance of growing the CIGS layers in Cu-rich conditions becomes more important with increasing deposition rate.

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First of all would like to acknowledge YOU – for showing such a great interest in my work that you have read my thesis to the very last page!

Already in the beginning of my under-graduate studies I felt that an attraction solar cells. A few years later at sat in a bar in Wien and listened to a man talking about sputtering and ZnO – I didn't understand much but after half an hour of talking he was willing to let me do my diploma work at Ångström Solar Center. A couple of month later I arrived in Uppsala and started my diploma work, with the same guy – John Kessler – as my supervisor. With time unlimited discussions he brought me into the world of science and solar cells. Also during my following time as a PhD student, he continued always taking the time to explaining the results he got when he had made the same investigation as I was *planning* to do, but ten years earlier! (He also taught me some of the worst jokes I've ever heard like: Do you smoke? – Only when I'm on fire!)

When starting my PhD Marika Edoff took over as my supervisor. Among the many things she taught me in the lab I think the most important was the partial transfer of her "magic" feeling of growing good CIGS! During the years she has also "torn her hair" over my not "over-natural" talent in the English language, but always with great patient she has made it läseable. Lars Stolt has been my "head" supervisor during these years, which doesn't mean that he hasn't reviewed my work with the strongest magnifying glass. Not always in good time, but always – and always by bringing in a couple of new perspectives!

The cliché that says, "a fruit full discussion is never further away than my closest colleague" has been exceptionally true for my case. During the last two years I have chaired my room with Jonas "Boy" Malmen Malmström. With truly no limited enthusiasm he has always been in for discussions of any kind, and especially about solar cells! With the addition of being a good friend he has really contributed a lot to this work and my understanding of many physical phenomena (which doest not mean that this is something he is proud of!). My former roommate, Johan "thorper" Wennerberg, also contributed a lot to my well being behind the walls of Ångström. With a lot of fun we found solutions to most things in life! Also all the other "astonishingly" good people in solar cell group have embellished my time during these years!

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Important, especially during busy days of thesis writing, is the possibility to relax and think of other things. Such an oasis has been Hofors, where activities like "family championship in mushroom picking" have helped me to forget everything about solar cells!

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