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Advanced TCAD Simulations and Characterization of Semiconductor Devices

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Abstract
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Today, micro- and nano-electronic devices are becoming more complex and advanced as the dimensions are shrinking. It is therefore a very challenging task to develop new device technologies with performance that can be predicted. This thesis focuses on advanced measurement techniques and TCAD simulations in order to characterize and understand the device physics of advanced semiconductor devices.

TCAD simulations were made on a novel MOSFET device with asymmetric source and drain structures. The results showed that there exists an optimum range of implantation doses where the device has a significantly higher figure-of-merit regarding speed and voltage capability, compared to a symmetric MOSFET. Furthermore, both 2D and 3D simulations were used to develop a resistive model of the substrate noise coupling.

Of particular interest to this thesis is the random dopant fluctuation (RDF). The result of RDF can be characterized using very advance and reliable measurement techniques. In the thesis an ultra-high precision parametric mismatch measurement system was designed and implemented. The best ever reported performance on short-term repeatability of the measurements was demonstrated. A new bipolar parametric mismatch phenomenon was also revealed using the measurement system.

A complete simulation platform, called SiSPET (Simulated Statistical Parameter Extraction Tool), was developed and integrated into the framework of a commercial TCAD environment. A special program for randomization of the doping was developed and proven to provide RDF effects in agreement measurement. The SiSPET system was used to investigate how different device models were able to take RDF effects into account. The RDF effects were translated in to parameter fluctuations using the developed extraction routines. It was shown that the basic MOSFET fluctuation model could be improved by including the field dependenent mobility. However, if a precise description of the fluctuations is required an advanced compact-model, such as MOS Model 11 should be used.

Keywords: MOSFET, RDF, random dopant fluctuation, asymmetric, parametric mismatch, TCAD, compact modeling, fluctuation model

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Till Filippa, Fabian och Magdalena

List of Papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I T. Ewert, L. Vestling, and J. Olsson (2003) Investigation of the electrical behavior of an asymmetric MOSFET. *Microelectronic Engineering*, 65:428-438

II S. Kristiansson, S.P. Kagganti, T. Ewert, F. Ingvarsson, J. Olsson, and K.O. Jeppson (2003) Substrate Resistance Modeling for Noise Coupling Analysis. *In Proceedings of the IEEE International Conference on Microelectronic Teststructures, ICMTS*, 124-129

III T. Ewert, H.P. Tuinhout, N. Wils, and J. Olsson (2005) Design and implementation of an ultra high precision parametric mismatch measurement system. *In Proceedings of the IEEE International Conference on Microelectronic Teststructures, ICMTS*, 149-154

IV N. Wils, H.P. Tuinhout, T. Ewert, J. Berkum, M. Kaiser, and R. Weemaes (2005) Identification and analysis of a new BJT parametric mismatch phenomenon. *In Proceedings of the 2005 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, BCTM* 224-227

V T. Ewert (2006) Design and implementation of a random dopant fluctuation simulation system 'dr'. *Tecnical Report available from www.diva-portal.org ISBN 91-506-1868-7*

VI T. Ewert, H.P. Tuinhout, N. Wils, and J. Olsson (2006) TCAD assisted evaluation of MOSFET fluctuation models. *Manuscript*

Comments on my contribution to the appended papers

I All simulation work, the data analysis, and all of the writing with input from the co-authors.

II All device simulation work and analysis of these simulations.

III All programming and design of the measurement system and statistical evaluation tools. The new STR algorithm was also the au-

	thors invention. All writing with input from the co-authors.
IV	Contribution to part of the measurements and initial analysis.
V	All work was done by the author.
VI	All simulation work, parameter extractions, model implementations, programming, data analysis, and major part of the writing with input from the co-authors.

Contents

1. Preface

This thesis summarizes my work of the last five years at the Ångström laboratory and at the Philips Research Laboratory, PRL, Eindhoven, Netherlands. I joined a project called "High Frequency Silicon, HFS" funded by the Swedish Foundation for Strategic Research, SSF in 2000. This project was a joint project between KTH, Chalmers and Uppsala University. One of the project's objectives was to "Mastering state-of-the-art TCAD and characterization techniques for evaluation of MOS structures"; this thesis is an effort in the spirit of this objective. My starting project was "Investigation of the electrical behavior of an asymmetric MOSFET", Paper I, which introduced me to the world of TCAD simulations and MOSFET devices. This excursion into TCAD continued in the substrate-modeling project that showed the possibilities and limitations of 3D TCAD. This substrate-modeling project brought me to the ICMTS conference, where I met Hans Tuinhout who gave me the opportunity to have an internship at PRL in his project "Limits of matching"; the purpose of this internship was to build and implement a "Parametric Mismatch Characterization System" with unprecedented repeatability, the results from which internship is presented in the Paper III. This system was then used to characterize new mismatch phenomena for BJT's in Paper IV. This collaboration evolved and we finally decided to build a "Random Doping Fluctuation Simulation system", Paper V, to study intrinsic device fluctuations due to the random positions of doping atoms in semiconductor devices, by the use of TCAD tools. This system was essential for my last paper where we investigate modeling of fluctuations using compact models i.e. MOS MODEL 11.

The intention of this thesis is, from the author's point of view, to introduce TCAD and to provide a useful MOSFET TCAD primer that could be of substantial significance to anyone dealing with MOSFET simulation of modern deep submicron devices. The thesis also includes work on a number of measurement techniques as well as some useful advices.

2. Introduction

This thesis is about advanced studies of semiconductor devices using both computer simulations and measurements. This discipline of science originates from the pioneering research by Bardeen, Brattain and Shockley in 1947 when they invented the bipolar transistor. This invention was followed by an intense period of research and finally Jack Kilby at Texas Instrument made the first integrated circuit, IC, in 1959 [31]. This first IC was fabricated on a single chip of germanium with gold wires for inter connections; the implemented circuit was a flip-flop. Today IC's are found in all kinds of equipments from space shuttles to toasters. The IC is built up by integrating many small functional elements on a single silicon crystal. These functional elements are hierarchical structures that start with single transistors and end in functional blocks like a comparator or a flip-flop circuit. The desire to integrate more and more functionality into the IC's, increase their functionality as well as decrease their cost results in a never-ending race of shrinking device dimensions. The benefits of miniaturization are: higher packaging density, higher circuit speed and lower power dissipation. There exists a great variety of different transistor types but the two most important types are the bipolar transistor, BJT, and field effect transistors, FET. The most widely used transistor type today is the 'metal oxide semiconductor field effect transistor', MOSFET, however for some high performance analog applications the bipolar transistor is still commonly used together with MOSFET's in a special process called BiCMOS. There exist a number of approaches to describing and understanding device operation. The first and natural way is to use basic physics and measurements to derive closed form expressions for the desired observable; however this is only possible in the simplest of cases. Real world devices show much more complex behavior, and their description necessitates the development of comprehensive numerical and computer models. The first researcher to use this approach was Shockley in the late forties [56] on a pn-junction. These early attempts have since then evolved into a separate area of research. Using state of the art simulation tools one can today achieve very reliable results on devices where closed form expressions simply do not exist i.e. LDMOS devices [72, 6]. Another opportunity that simulation tools provide is to simulate a device that does not exist in the real world, for example one can simulate a device that only exists as a novel design idea. This whole framework of sim-

ulation tools is generally referred to as technology computer assisted design, TCAD. Another very important set of simulation tools is the circuit simulator and corresponding models, for example the SPICE simulator using models for MOSFET (BSIM4). The purpose of the circuit simulation tools is quite different compared to TCAD tools; here the goal is to simulate the electrical terminal behavior of a functional block as fast and as reliably as possible, the devices inside the block are defined by a set of equations and parameters. The parameters used in the compact model are usually determined using real measurements on real devices and a set of scaling relations together with heavy use of numerical optimization routines. This parameter extraction is a hard and tedious work but still essential if the compact model is to produce good and reliable simulation results for a given circuit. In this thesis we will analyze some advanced semiconductor devices using both commercial and in-house developed TCAD tools as well as measurements. By using simulation tools and measurements we have gained knowledge about:

- Electrical behavior of an asymmetric MOSFET.
- Resistive coupling between devices through the substrate.
- Building a state-of-the-art parametric mismatch fluctuation characterization system.
- A new BJT mismatch mechanism
- Statistical device fluctuations of MOSFET's due to random doping fluctuations.

3. TCAD - Technology Computer Assisted Design

TCAD simulations are today an extremely important activity for the IC industry, since it makes it possible to explore technologies and concepts that do not yet exist in reality. TCAD simulations also provide information about the inner workings of devices, thus simplifying improvements on existing technologies. A complete TCAD simulation involves the following steps:

- Virtual fabrication of the device using a process simulator or a device editor.
- Creation of a mesh suitable for device simulation.
- Device simulation that solves the equations describing the device behavior.
- Post processing i.e., generation of figures and plots.

In this chapter the most common TCAD simulation tools as well as some limitations of these tools are described. We follow the path of a complete TCAD simulation project in the presentation, starting with device generation, device simulation and finally an analysis of the results obtained by using TCAD tools.

3.1 Device generation

This first step of the TCAD tool-flow is intended to generate a structure that is suitable for device simulation. This means that the device structure should be described by its boundaries and materials. This step can be performed in two different ways; the first and easiest one is to use a device editor like Mdraw [63]. This program is very much like a drawing program; the structure is created and edited using the mouse or a script. The other approach involves actual computer simulations of each process step; this procedure is called process simulation. We present both approaches separately.

3.1.1 Device editor

The generation of a device using a device editor is similar to making a drawing of the device; several basic geometrical elements are available like rectangles

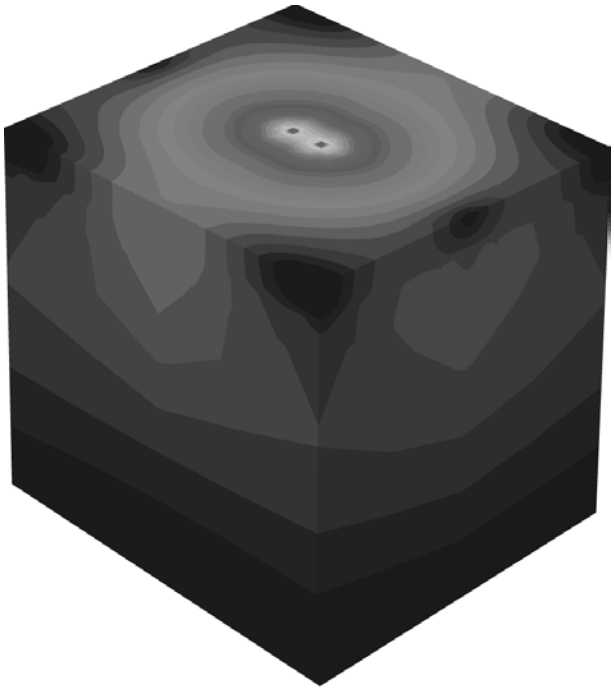

Figure 3.1: A 3D structure generated with Mdraw. Used for simulation of the resistance between contacts on silicon, Paper II.

and lines. Each of these geometrical elements is also defined in terms of materials (aluminum, silicon, oxide, poly-silicon etc). Doping distributions are defined using analytical functions [63] . Usually a device can be created using some kind of a script language together with an editor. In Mdraw an embedded TCL [44] interpreter and a script can control the program. This embedded interpreter makes it very easy to generate parameterized structures with for example varying gate lengths.

In Paper II a device editor was used to create a structure suitable for substrate coupling analysis, see figure 3.1. For this specific case a 3D model was needed in order to model the resistance between the contacts. The advantage with this approach is that the fabrication process is not needed, thus new device ideas/concepts can be tested. It is also possible to include SIMS concentration depth profiles in this approach and further improve the fit between the model and measured data. The obvious disadvantage is that one may generate a structure that may not be possible to fabricate.

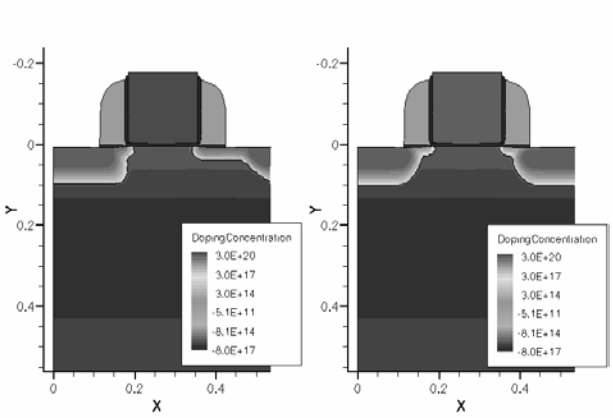

Figure 3.2: Process simulated devices from Paper I. In a) is an asymmetric device created by tilting the source and drain implantation. In b) is the normal device illustrated.

3.1.2 Process simulation

The idea behind process simulations is to mimic the manufacturing processes that are used to fabricate real devices. Such processes usually involve deposition, etching, planarization and implantation of different species. The development of models for each of these processes is a separate field of research [28]. The TCAD software developer takes the appropriate models and adopts them to fit the constraints of the process simulator. The actual process simulation follows the exact process flow of the real device. After the simulation the final device is defined in terms of a grid, and also information associated with the grid, i.e., the impurity concentration etc. In Paper I a 0.25 μm nMOSFET was process simulated, and the effect of tilting the S/D implantation resulting in an asymmetric device was studied, see figure 3.2.

3.2 Generation of a mesh suitable for device simulation

The output from the device generation is a boundary definition and a material specification. However in order to perform a device simulation a specific mesh suitable for the device simulation is needed since it is a finite element method, FEM, simulation. Extra refinements of the grid are needed particularly near interfaces between different materials, at doping gradients, in regions where interesting effects are known a-priori etc. The generation of a device grid can almost automatically be obtained using the software tools. However, it is often required hands-on manipulation in order to obtain an optimized simulation

grid, especially for complex device geometries.

3.3 Device simulation

A device simulation provides information about the inner conditions and the terminal characteristics of the device and thereby be able to predict the device behavior. There exist two fundamentally different methods in this area, first an analytical approach that uses simplified equations and geometries and solves these equations for different regions such as quasi- neutral, space-charge etc. The solutions are then linked using the boundary conditions for the different regions, this is the traditional schoolbook approach, see [64, 66]. In the first approach, only limited information about the inner conditions of the device is available. The other approach that will be discussed in more detail is the numerical approach that solves the fundamental semiconductor equations numerically [57]; this approach will be the focus of the next section.

3.3.1 Numerical Approach

This approach solves the fundamental semiconductor equations for each mesh point in the grid for the device. The fundamental semiconductor equations are Poisson equation, continuity equations for electrons and holes as well as for some special cases the hydrodynamic equations. The numerical approach can be applied both in 2D and 3D. However, the memory consumption for a 3D simulation is much larger compared to a 2D simulation. This is illustrated by the following estimates - the memory consumption for the device simulation in Paper I was approximately 100 MB compared to 1 GB for the simulations in Paper II. Both simulations used the device simulator DESSIS [1]. This is a limiting factor for most modern devices since they need quite a dense grid, so for most modern simulations one has to resort to 2D simulations or very crude 3D simulations. The selection of physical models is very important in order to get realistic results from the device simulator. This includes mobility models, carrier transport mechanism, velocity saturation, carrier generation and recombination, as well as QM correction. Some of the models need extra refinements of the grid at critical positions [1]. These issues will be discussed in detail for modern MOSFET simulations in the next chapter.

3.4 Special simulations

The simulations discussed so far are standard DC simulations but during the research culminating in this thesis several special simulations had to be per-

formed. In this section I will shortly describe the technology that underpins those special simulations.

3.4.1 Simulation of AC behavior

Traditionally, a device simulation is a DC simulation in a steady-state condition. But if a small sinusoidal signal is superimposed on a DC solution the complex (small-signal) admittance matrix can be calculated [35]. The admittance matrix describes the current response at a given node to a small voltage change on another node. By decomposing this matrix into a conductance matrix and a capacitance matrix one can calculate the other AC parameters like H, Z or S [52]. This technique was used in Paper I where simulations of high frequency behavior were performed. This was needed in order to calculate the important figures- of-merit that were used to evaluate the asymmetric MOSFET devices.

3.4.2 Transient simulations

Another powerful way to simulate and investigate a device is by doing simulations in the time domain. Based on a steady-state solution a voltage or current transient can be applied to any of the device terminals. The simulator then calculates the transient response on the other terminals. This approach is obviously relevant for simulation of switching devices, such as the MOSFET, among others. It is especially useful when studying non- quasi static phenomena within the actual device.

3.4.3 Mixed-mode simulations

In mixed mode simulations several device-simulated devices can be connected in a circuit together with elements that have a compact model description. This approach is very suitable for example in breakdown simulations of MOSFET devices, where it is important to include a series resistance in order to reduce the current that otherwise would impose numerical instabilities. In Paper I we used mixed mode simulations for the simulation of the breakdown voltage and in that paper we used a series resistance of 1 MOhm, see figure 3.3.

3.4.4 Statistical simulations

Variability of supposedly identical devices (mismatch) is today a hot topic for all disciplines of circuit design. These problems become more pronounced when going to smaller device geometries i.e., less atoms per device. The variability can be due to a lot of different factors; line edge roughness, process

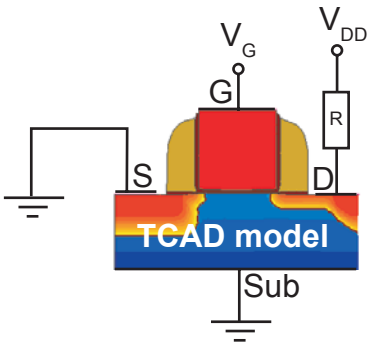

Figure 3.3: A circuit for mixed-mode simulations, the TCAD structure is connected to an external resistor for breakdown simulations.

gradients and dopant fluctuations etc [14, 43, 67]. In this thesis we focus particularly on random dopant fluctuations, RDF. This phenomenon was already identified in the early 60's by Shockley [58] as a limiting factor for the breakdown voltage of p-n junctions. In the mid 70's Robert W. Keyes from IBM wrote a paper about the impact of RDF on MOSFET [30] devices. During the 80's and early 90's several authors [23, 43, 74, 17, 62] started to use device simulations to understand the effects of RDF on MOSFET's. In our attempt to study the impact of RDF on MOSFET's we implemented a randomizer 'dr', Paper V, which applied Poisson statistics to the boron impurities in Paper VI, which gave us the opportunity to do statistical MOSFET simulations.

4. A MOSFET TCAD primer

In this chapter MOSFET device operation is introduced quantitatively. This section is followed by a description of the generation and simulation of a modern MOSFET device. The actual device simulation is introduced by a discussion about the appropriate physical models for a modern MOSFET.

4.1 Quantitative description of MOSFET operation

Here we introduce the basic operation of a conventional MOSFET, for simplicity we limit our discussion to n-type MOSFET throughout the chapter.

The top and cross-section view of an MOSFET is shown in figure 4.1. The conventional MOSFET is manufactured in bulk silicon and has a source, drain, gate and substrate terminals. The length of the poly-silicon gate length, Lf, is defined through the manufacturing process i.e. lithography steps. This gate length is longer than the metallurgical gate length, Lm, that is defined by the source and drain junctions which extend under the poly silicon gate. A third gate length that governs the electrical characteristics of a MOSFET is the effective gate length, Leff. This is the most important gate length for modeling MOSFET's.

The drain current that flows in the device is controlled by the gate and drain voltage. The vertical electrical field due to the gate voltage controls the number of free-carriers in the channel by creating an inversion layer of electrons and thus the number of carriers available for conduction. A positive voltage on the drain terminal will drain electrons out of the device and in order to maintain charge neutrality the source will supply electrons to the device. If the drain voltage is small enough the inversion layer charge extends through the channel region, this makes the MOSFET behave like a resistor. However if the drain voltage is large enough this region will be depleted near the drain side due to the high field, this will saturate the current and the MOSFET is said to be operating in the saturation region. If the gate voltage is below the required voltage for strong inversion; then the MOSFET device is in the subthreshold region and there is a small current floating in the device. Subthreshold behavior is of particular importance in low-voltage, low-power applications [20] .

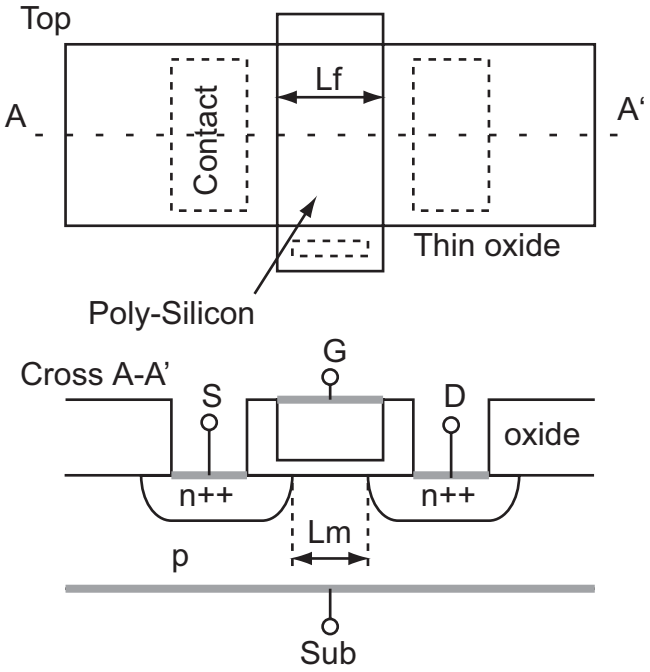

Figure 4.1: Top and cross-sectional view of a simplified MOSFET structure. The bottom view is the cross-section indicated by A-A’ in the top view. The source, drain, gate and substrate contacts are denoted S, D, G and Sub.

The subthreshold behavior is very important for digital applications since it describes how the device switches off. One important physical effect in subthreshold is that the current is dominated by the diffusion part in contrast to the other regions of operation.

4.2 A modern MOSFET device structure

A modern MOSFET is somewhat different from the device in figure 4.1. The MOSFET’s that are used for modern IC’s have additional device engineering techniques applied to it in order to enhance its performance like: HALO doping to suppress short-channel-effects [66] , threshold implants to adjust the threshold voltage, Anti-punch through implantations that locally increase doping concentration under the channel, source and drain extensions, silicided source and drain etc. A device with these features is illustrated in figure 4.2; this structure was generated with a device editor (MDraw) and all channel engineering implantations are defined by analytical functions. This device has a gate length, Lf, of 180 nm, but the used technology (oxide thickness, doping levels etc.) is for a 65 nm process.

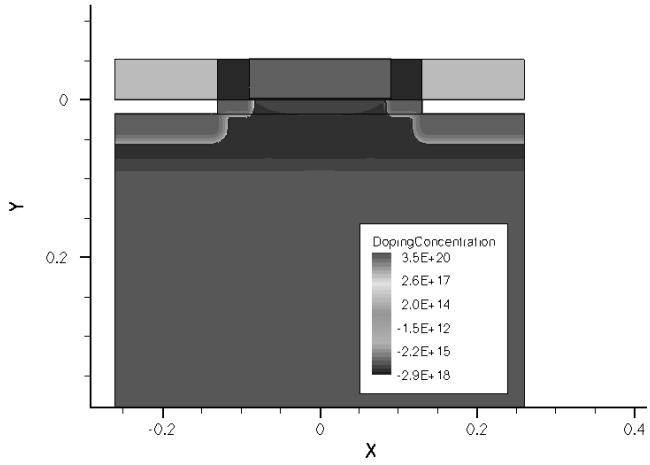

Figure 4.2: A modern MOSFET with Lf equals 180 nm, oxide thickness 1.8 nm. This device was created using a device editor (MDraw).

To get realistic device simulation results several different physical models are needed and some of them have special needs concerning grid density. The first thing to decide is which transport mechanism to choose. Thus, for this relatively long channel device it is sufficient with the basic drift-diffusion equations but if the gate length is below 60 nm then it is often suggested to use hydrodynamic (energy-balance) simulations. The standard drift-diffusion approach cannot reproduce velocity overshoot and often overestimates the impact ionization generation rates. The hydrodynamic model is a very good compromise to the full Monte-Carlo, M-C, simulation of the Boltzmann kinetic equation; the M- C approach is computationally very intensive and cannot be used for industrial TCAD simulations. The full hydrodynamic formulation is comprised of 8 partial differential equations [11, 10, 9]. However, in here we have used drift-diffusion equations as suggested by an authority on TCAD simulations. Since the conduction current is mainly confined to a region close to the gate oxide - silicon interface the bulk mobility model must be modified by taking into account surface effects [37], velocity saturation [12] . These effects reduce the effective surface mobility to be a fraction of the bulk mobility. The channel region (top 10nm) is the most critical region to have a dense grid in, since many of the mobility models have special requirements. We also found that it was crucial to have a dense lateral grid near the drain if a good description of the output characteristic is desired. Finally, due to the heavy scaling of MOSFET devices i.e. thinner gate oxide, higher level of channel doping and shorter gate lengths, the wave nature of electrons and holes cannot be neglected. The most basic quantum mechanical (QM) effect is the shift of threshold voltage and reduction of gate capacitance. This means that the quan-

tization effects will electrically appear like an effectively thicker gate oxide. In our approach we used the simple Van-Dort model [70] which was accurate and fast enough for our purposes; however this model does not give the correct density distribution in the channel, thus it is only used for MOSFET devices. On the other hand, it describes accurately enough important terminal characteristics. The last effect to model is the poly-depletion which is the depletion of the poly due to the gate voltage. This is done by assigning the right material to the gate and define a number of layers of dense grid (< 1nm) near the oxide interface. A simple but very important thing to remember is to assign the correct resistivity to the terminal contacts; otherwise the terminal currents will not be correct. Our modern MOSFET simulation recipe is summarized in the following list:

- The band gap and density of states are crucial parameters of a semiconductor material. For the band gap narrowing we use the Slotboom model [59, 60, 32]. The density of states is calculated as a function of carrier effective mass. For silicon the most appropriate model for carrier effective mass is the temperature independent model [34].
- For most practical MOSFET TCAD projects it is enough to use the basic drift-diffusion equations even for gate lengths below 100 nm. This is contrary to the results in the literature but a common practice within the industry.
- Use a doping dependent mobility model, Masetti [38] , with the following extensions; Mobility degradation at interfaces (Lombardi model [37]), High field saturation (velocity saturation) i.e., carrier drift velocity is no longer proportional to the electric field (Canali model [12]). The mobility degradation models need a grid with a vertical spacing of < 0.1 nm for the top 2 nm.
- Use the Van-Dort model for quantization (Q-M) effects. This is also a common practice within the industry. For a more realistic description of the density distribution use a Density-Gradient model [5, 4] , however, this model requires much longer simulation times and convergence problems are common.
- Use Shockley-Read-Hall (SRH) model for recombination through deep levels in the band. Add Hurkx [26] model for trap-assisted tunneling. This model reduces SRH lifetimes in regions with high electric field.
- Use a model for Avalanche generation (impact ionization). In our simulations we used the model of van Overstraaten - de Man [45].
- To simulate the effects of poly-silicon depletion due to the gate voltage add some layers of fine (<0.1nm) vertical grid.
- Assign the correct resistivity to the source and drain contacts, usually for a TCAD simulation this means to assign a reasonable value to the distributed resistance.

5. Circuit simulation and compact models

Traditionally electronic circuits have been designed by using prototypes and simple back-of-envelope calculations. A very important step in this approach was to build a prototype circuit on a breadboard. This prototype circuit could easily be evaluated and fine-tuned. But when the circuits grew larger and more complex it became desirable to simulate their behavior on computers. This was particularly true for integrated circuits with hundreds and later thousands of components. The task of setting up such a circuit on a breadboard was becoming impossible. At the same time the computing power was increasing and it finally was possible to write a simulation program that could provide accurate results. This was at the time somewhat revolutionary; a circuit could be designed, evaluated and redesigned using only computer simulations. The first attempt to make a computer-aided circuit simulator was CANCER (Computer Analysis of Nonlinear Circuits, Excluding Radiation) [42]. CANCER was the predecessor of the SPICE (Simulation Program with Integrated Circuit Emphasis) program [41]. SPICE and CANCER were developed at the University of California/Berkeley. Today SPICE is the standard simulation tool for the IC industry mainly due to two reasons - it was available from the University of California/Berkeley for a small fee including the source code, thus giving the user the possibility to extend the program with his/her own code. Secondly, SPICE became available at the right time! Today there exist numerous offsprings of the original SPICE; PSpice, HSpice, hpeesofsim, PStar etc.

A SPICE type simulator treats a circuit in a node/element fashion; see figure 5.1 where the circuit is described as a collection of various electronic components (resistors, capacitors, diodes etc.) and these components are connected at numbered nodes. This means that a circuit is completely defined in terms of the nodes and by the components connected to the nodes. A circuit with n-nodes will be described by an nxn matrix. By defining state variables at each node (voltages) and fixing the external nodes (such as ground, supply voltage etc) the matrix can be solved to determine the values of the state variables. In order to reach a solution, models for each component are needed. These models that are used within a circuit simulator are denoted as compact models. Since there are many different types of components that need to be modeled inside a circuit simulator many different compact models have been developed

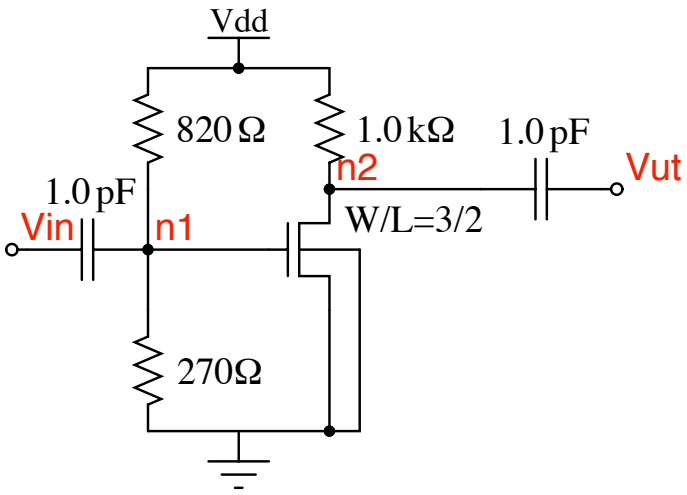

Figure 5.1: A schematic for a circuit to be simulated using SPICE, the nodes are labeled Vin, n1, n2, Vdd, GND and Vut.

and used over the years. SPICE has built-in models for resistors, capacitors, inductances and simple models for semiconductor devices. But in order to simulate more complex semiconductor devices special models are needed, for instance MEXTRAM [46].

5.1 A survey of compact models for MOSFET

The models that are commonly employed can be divided into three historical generations. The first generation of MOSFET models treats the device as almost ideal describing the MOSFET from very simple physically based parameters. This generation of models consists of the Level 1[55], Level 2 [73]and Level 3 [36] models. The second generation of models is markedly different; here the focus of the model is circuit simulation usage. In this generation the parameters in the model are empirical in their character. This generation of models encompasses BSIM1[54], BSIM2 [27] and HSPICE Level 28 [8]. The third generation of models basic intent is to return to a simpler model structure with a reduced number of parameters. The parameters should also be physically based. This generation also includes more advanced smoothing functions; with these functions the device equations are smooth and continuous, and a single equation is used for all regions of operation (sub- threshold, linear and saturation). Typical models from this generation are BSIM3 [25],

BSIM3v3 [13] and MOS Model 9 [71] and MOS Model 11 [49] from Philips. MOS Model 11 is a compact MOSFET model intended for digital, analogue and RF circuit simulation in modern CMOS technologies. MM11 is a successor to MOS Model 9. This model was developed to give accurate descriptions of the currents and charges, especially the first-order derivatives (transconductance, conductance, capacitances etc.) The main feature of the model is that it is surface-potential based, thus resulting in equations that are valid in all regions (accumulation, depletion and weak- moderate- and strong inversion). This model is extensively used in Paper VI for all compact model simulations. The most recent addition to the MOSFET compact model family is the PSP model [22], which is intended for the same applications as MM11. The PSP model has its origin in the MOS Model 11 and SP [21] from Pennsylvania State University and is jointly developed by Philips and Pennsylvania State University. The PSP model is also a surface-potential based MOSFET model that contains all important physical effects (mobility reduction, velocity saturation, Drain Induced Barrier Lowering (DIBL), gate current etc.). The PSP model was recently selected to be the industry-wide standard for future nanometer chip design by the Compact Model Council, CMC. The CMC is the world's foremost authority on standardization, implementation and use of transistor models and is comprised of 31 leading semiconductor companies and circuit simulator suppliers.

5.2 Statistical simulations with circuit simulators

The purpose of circuit simulation and compact models is to describe the behavior of a circuit. The circuit simulator can also be used to estimate the importance of variations in devices for the overall behavior of the circuit. This discipline of circuit simulations is called statistical circuit simulations [48]. This type of simulations is of great importance in the design for manufacturability. A statistical circuit simulation is a Monte-Carlo simulation that could be performed in two different ways; the first way is to use a dedicated mismatch model, the other way is to manipulate the model parameters in a way that describes the fluctuations. Both of these approaches involve several hundreds of re-simulations of the circuit in order to assess the performance of the circuit.

6. Measurements

The purpose of a measurement can be quite different, but usually it is an attempt in one of these directions:

- To understand and/or improve a device/technology.
- To obtain parameters for a compact-model.
- To verify the performance of a device.

In this section we discuss some measurements that are important in order to understand MOSFET device operation. We also shortly describe parametric mismatch measurements and the special requirements of such esoteric high precision activities.

6.1 DC measurements

DC measurements are the most important type of measurement for characterizing semiconductor devices. A DC measurement is a measurement of the device response to a fixed bias condition. The DC measurement on a semiconductor device is usually performed using a special type of measurement equipment, the source-measure unit, SMU. This unit can simultaneously both measure an observable (voltage or current) and provide bias (voltage or current) to the device. A very useful feature of the SMU is that it is possible to sweep a bias i.e., increase/decrease a bias in small steps and simultaneously measure the device response to the stimuli. It is of utmost importance for the accuracy and precision of the measurement to use an integration time of 1 PLC (Power Line Cycle, in Sweden 20ms). If extra precision is needed extra measures are available e.g., use the MxSy concept; Measure x times and use the median value y [68]. Usually several SMU's are integrated within one instrument in a modular way. The classical instrument of this type is the Agilent HP4156A precision semiconductor parameter analyzer. A recent addition to this family of instruments is the Keithley 4200- SCS Semiconductor Characterization System. Both instruments have several SMU's available and are controlled by the means of an integrated computer. However the HP4156A is equipped with an old and slow CPU (M68k, 6MHz) whereas the 4200-SCS basically is a modern PC (2 GHz Pentium P4). In the 4200-SCS the SMU's are controlled by the means of a special PCI card that controls the SMU's via a fast instrumental bus, this makes it possible to measure in parallel on differ-

Figure 6.1: The author of this thesis is working with the Keithley 4200-SCS parameter analyzer at Philips Research/Eindhoven. In the background the Cascade 12k Summit semi-automatic probe-station is visible, and on the monitor in the background is a wafer map shown. This system was used in Paper III and Paper IV.

ent SMU's. Both instruments are easily controlled remotely via the GPIB bus (General Purpose Instrument Bus).

For on-wafer characterization, the measurement equipment and the device are connected via triaxial cables to a wafer probe station , see figure 6.1. The wafer probe station can be of three different types: fully automatic, semi automatic and manual. The fully automatic probe station handles the wafer in an automatic way; several wafers are loaded in a plastic cassette. The probe station then loads and aligns the wafers. In the semi-automatic probe station the user loads and aligns the wafer manually, the probe-station and a wafer map control the actual stepping between devices and chips. Finally the manual probe station is fully manual. In the work culminating in Paper III and Paper IV we used a semi-automatic wafer probe station Cascade Summit 12k and a Keithley 4200-SCS [29], see figure 6.1. This system should in theory be able to measure in 1 fA range.

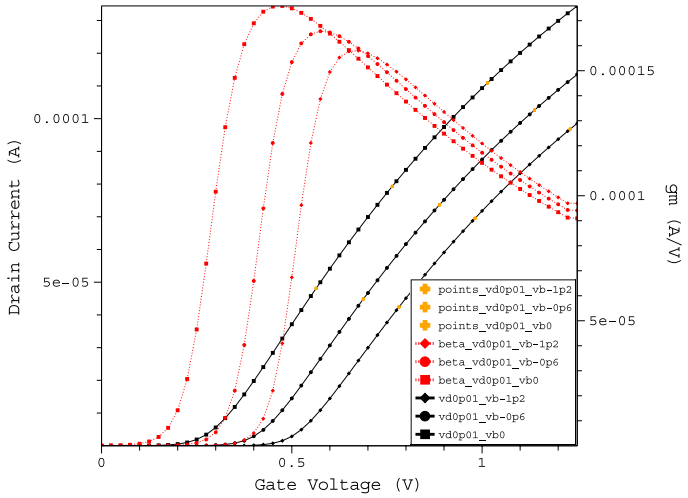

Figure 6.2: Linear region transfer characteristics for the 180 nm MOSFET device in figure 4.2. V_{DS}=10mV, V_{GS}=0..1.25@25mV steps and V_{BS}=0,-0.6,-1.2 V.

6.2 The most important DC measurements for MOSFET characterization

The most important measurements for the characterization of MOSFET devices are: linear region transfer characteristics, subthreshold characteristics and finally the well-known output characteristics. These measurements give an almost complete picture of the static behavior of the MOSFET device. Each of these characteristics are discussed separately as follows.

6.2.1 Linear region transfer characteristics

The first characteristic to study in more detail is the linear region transfer characteristics, see figure 6.2. This graph is typically obtained by using the following bias condition:

- V_{DS} is small (V_{DS} < 10 - 100 mV)
- V_{GS} =0..V_{DD}@25 mV steps
- V_{BS}=0..-V_{DD}@3 steps

This graph tells us most about the physical structure of the device. This graph is used to extract the threshold voltage, gain factor and mobility reduction parameters. By using different V_{BS} biases a calculation of the body factor is possible. The body effect is visible in figure 6.2; this effect increases the threshold voltage with increasing substrate bias.

The important thing to note is that due to the low V_{DS} almost the whole curve is in the linear region. The low V_{DS} also reduce the impact of velocity

saturation and short-channel-effects. The peak transconductance roll-off for higher V_{BS} is due to mobility reduction and source/drain series resistance. This characteristic is also used for threshold voltage extraction and assessment of V_T roll-off for shorter devices.

Threshold voltage extraction

In this thesis nearly all extractions of the threshold parameters were done in the linear region. The method employed was published by M.F Hamer [24] and is referred to as the 3-point method. This method is essentially a direct extraction of the parameters in the following expression for the drain current in the linear region.

$$I_D = \frac{\beta(V_G - V_T - \frac{1}{2}V_{DS})V_{DS}}{1 + \theta(V_G - V_T)} \tag{6.1}$$

In the original approach a fixed gate bias, FGB, was used for the extraction. This FGB is comprised of three voltages and the corresponding drain currents. The first voltage is the voltage when the maximum transconductance occurs. The third voltage is at V_{DD}. Finally the second voltage is the sum of the first voltage and one third of the difference between the first and the third. A variant of this approach is the fixed gate overdrive, FGO. In this method a first estimate of the threshold voltage is used and to this estimate the overdrive voltages are added. A combination of FGB and FGO has successfully been used in high precision studies [15] . In here we use a FGB extraction for the initial threshold voltage followed by ten iterations of FGO, usually it is more than enough with five iterations. The selection of the overdrive voltages needs special attention. In our particular experiments we used 0.25, 0.45 and 0.7 V.

6.2.2 Subthreshold characteristic

This curve is very interesting from the device limitations perspective. This curve shows how the device turns off, see figure 6.3. Since the diffusion current dominates the current transport in this regime, the drain current has a logarithmic dependence on the gate voltage. Therefore, the current is plotted using a logarithmic scale. This graph is obtained by using the following biases:

- V_{DS}=0.1 ... V_{DD} 3 values
- V_{GS}=0 ... V_{DD}@25 mV steps
- V_{BS}=0, -V_{DD}

The parameters that can be extracted from a subthreshold characteristic are: Subthreshold swing in mV/decade current, Drain-Induced-Barrier-Lowering;

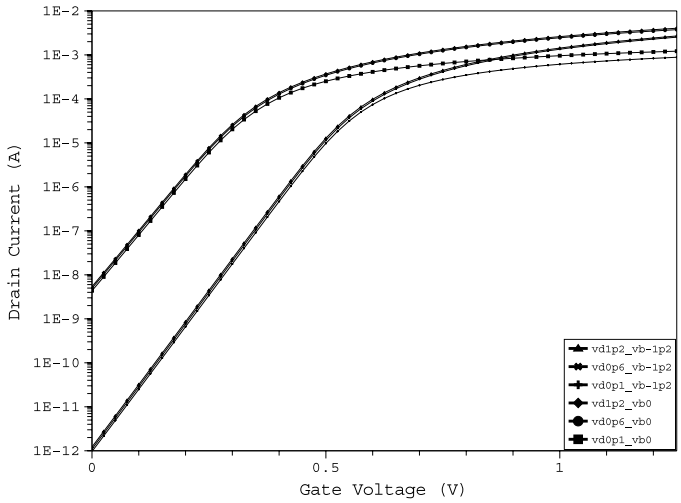

Figure 6.3: Subthreshold characteristics for the 180 nm device,in figure 4.2 V_{DS}=0.1, 0.6 and 1.2 V, V_{BS}=0,-1,2 V and V_{GS}=0..1.25 V@25mV steps.

threshold voltage reduction due to the depleted source and drain regions. Off-current and On-current and Low-current behavior, punch through etc.

6.2.3 Output characteristic

This output characteristic, figure 6.4 provides the common transistor curves, but from a device physics standpoint this graph adds little in comparison to the other two. However this characteristic is often used for back-of- envelope calculations for circuit design. The output characteristic is obtained by using the following biases:

- V_{DS}=0 ... V_{DD}@50mV step
- V_{GS}=0 ... V_{DD}@7 steps
- V_{BS}=0V

This curve provides information about the maximum available current (saturation current) that the device can deliver (V_{DS}=V_{GS}=V_{DD}=1.2 V).

Important things to observe in the output characteristics are the slope in saturation caused by channel length modulation and static drain feedback.

6.3 Extraction of parameters for MOS Model 11

Extraction of parameters for compact-models is also a common and important type of DC measurement activity; usually this involves measuring many

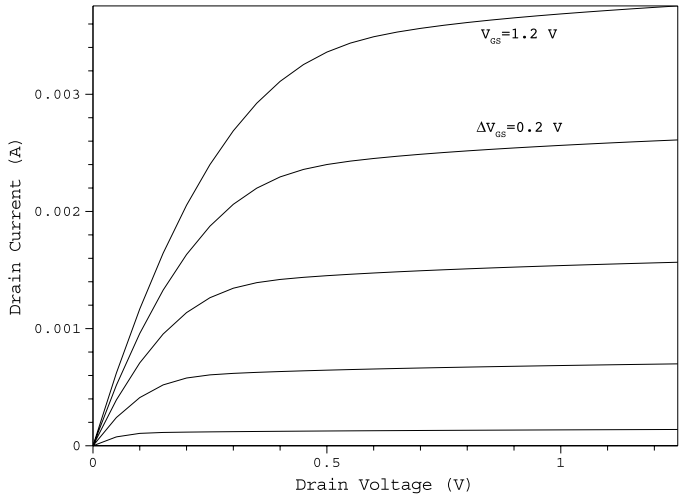

Figure 6.4: Output characteristics for the 180 nm device in figure 4.2.V_{DS}=0 ... 1.2@50mV, V_{BS}=0,-1,2 V and V_{GS}=0..1.2 V@200mV steps.

different geometries and IV-curves. The measurement hardware used in the industry is of the same type as described in the previous section. However, the compact-models of today usually involve numerical optimization to extract the parameters. Therefore, it is very convenient to use an integrated program like IC-CAP that handles everything from instrument control via GPIB to optimization and extraction of the parameters. In this section I will shortly outline the procedure for extracting a miniset of parameters for MM11. The miniset describes the electrical behavior of a single geometry [51] . All of these extractions were performed with IC-CAP on TCAD simulated data.

6.3.1 Outline of the extraction procedure

The strategy used for parameter extraction for MOS Model 11 minisets on TCAD simulated devices is based on three main steps:

1. TCAD simulation of the necessary DC-measurements, export the data to MDM file format [2].
2. Extraction of a miniset for long channel device.
3. Extraction of a miniset for short channel device, using the long channel device data.

The needed TCAD simulations for n-type MOSFET are listed in table 6.1.

By using the procedure described in [51] a set of parameters for the long device is obtained. These long channel parameters are then used as starting values for the extraction of the short channel parameters for the different devices with short gate lengths.

Table 6.1: *Measurments needed for extraction of MOS Model 11 parameters*

Measurement	V_{GS}	V_{DS}	V_{BS}
Linear I_D/g_m–V_{GS}	0–V_{DD}@25mV	10 mV	-V_{DD}–0@ 3 steps
Subthreshold I_D–V_{GS}	0–V_{DD}@25mV	0.1–V_{DD}@3 steps	-V_{DD},0
Output I_D/g_{ds}–V_{DS}	0–V_{DD}@7 step	0–V_{DD}@50mV	0

Extracting parameters for compact-models is a hard and complicated work. Since the extraction routines rely heavily on numerical optimization it is easy to end up with unphysical parameters for a physical model. The first extraction of the threshold parameters for example is best done manually for the first iteration. The problem of doing the parameter extraction is partly due to the complexity of the model itself, one has to get the gut feeling for the parameters that comes from experience. It is also necessary to have the guidance of the gurus behind the model. To illustrate the above arguments we would like to discuss a specific aspect of the extraction. Thus, during the extraction of the threshold parameters (PHIB, KO, BET, THESR, THER) the parameters describing the mobility reduction (THESR, THER) compete with the gain factor (BET). This often results in a situation where either the gain factor or the mobility reduction parameters have unphysical values. This situation is resolved by assigning reasonable values to the different parameters at the beginning of the extraction. Eventually the extraction procedure is working and the extraction is smooth and easy, resulting in physical parameters and fits that are attainable only with a modern surface potential based model see figure 6.5. These experiences come from the extended work of doing parameter extraction for high precision purposes in Paper VI.

6.4 Measurement of Parametric Mismatch Fluctuations

In this section we describe a special characterization technique that is used to characterize Parametric Mismatch Fluctuations, PMF, on supposedly identical devices. Many analogue circuit blocks need identical devices for their function (current mirrors etc.). By placing the devices close to each other and with equal surroundings this equality should be assured, see figure 6.6 where a matched MOSFET pair is displayed.

However, even for closely spaced devices there are small electrical differences due to the microscopic differences: line-edge roughness, electrical charges and random doping fluctuations. These effects are denoted as mismatch or parametric mismatch fluctuations, PMF. Mismatch is defined either

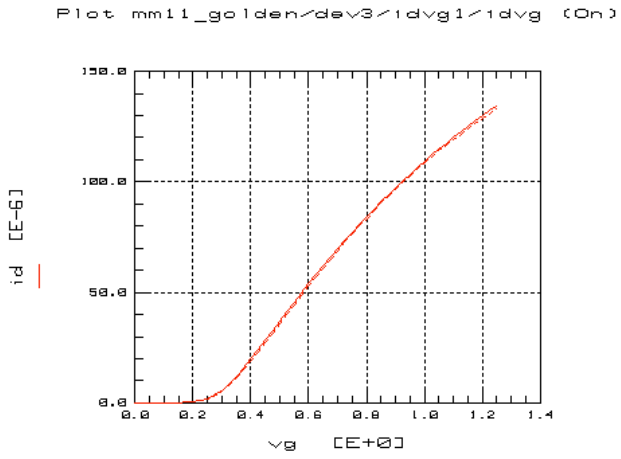

Figure 6.5: Linear transfer characteristic (V_{DS}=10mV, V_{BS}=0 V) for a 180 nm device with HALO, Paper VI. Solid line is from TCAD simulation. Dotted line is modeled using MOS Model 11. These curves are on top of each other!

for a measurable quantity like the current or for a device parameter like the threshold voltage.

By measuring a number of matched pairs on different chips on a wafer one can assess parametric mismatch fluctuations by the means of statistics, see figure 6.7. The observables to use are either the absolute difference ($\Delta P = P_1 - P_2$) or the relative difference ($\Delta P/P$) between the observable P for device one (P_1) and two (P_2) in the pair. Often the relative difference is used for currents and the absolute difference for voltages. This population of ΔP or $\Delta P/P$ is normally distributed; hence it is fully described by the median and the standard deviation of the population. Usually the population studied is relatively small (<100). This results in large uncertainties. It is also quite common that the populations contain outliers that ruin the statistics; these outliers should be filtered out [68]. A very useful tool to detect outliers is to plot the population using normal scaled cumulative probability plots [68]. In this plot the deviations from a normal distribution is plotted as a deviation from a straight line. The requirements on the measurement equipment are very high. Often the differences between the measured observables are much below the instruments accuracy specification. This means that special algorithm, Paper III, and shielding for EMC [69] are very important to assure the quality of the measurement. Since the measurements in a PMF study can be much below the specification of the accuracy for the instrument, special precautions are needed. These precautions include a continuous monitoring of the short-term repeatability, STR. The STR is essentially based on a re-measure of the measurement. If the time between these measurements is below 1 minute then the

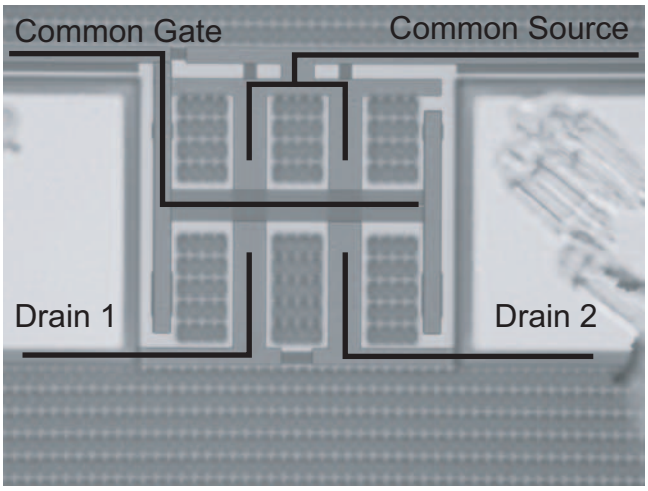

Figure 6.6: A matched MOSFET pair, where each transistor in the pair has equal surroundings to assure that the observed differences are due to the microscopic fluctuations. Pictures are the courtesy of Philips Research.

difference can be attributed to system and device noise and EMC disturbances. In Paper III we implemented a PMF characterization system with extremely good STR (<10 ppm). This system was used extensively during PMF study that resulted in Paper IV. During these measurements on very sensitive bipolar devices strange anomalies were encountered. After a thorough investigation [69] it was concluded that the major part of these anomalies was due to RF disturbances. The Cascade 12k Summit probe station provides a shielded micro chamber for the wafer, figure 6.8 however it proved not to be sufficient in terms of RF shielding without extra measures (new top-hat).

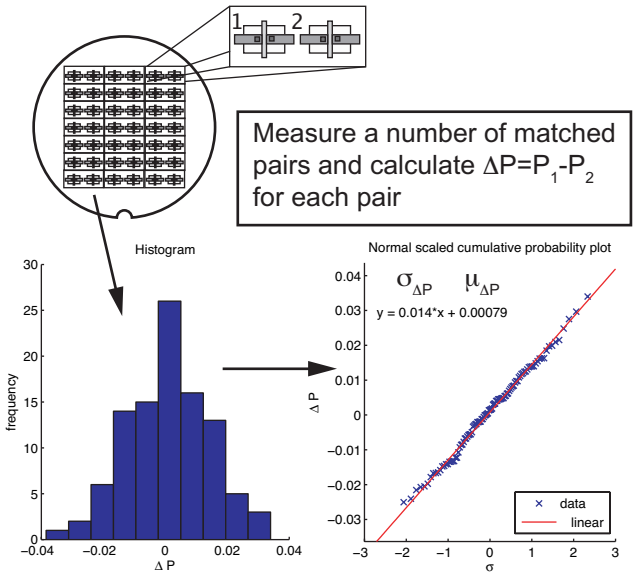

Figure 6.7: Principle of a parametric mismatch fluctuation measurement of the threshold voltage variations on a population (101 device pairs) of MOSFET matched pairs. The normality of the population is verified in the normal scaled cumulative probability plot to the right. There are no outliers in the population.

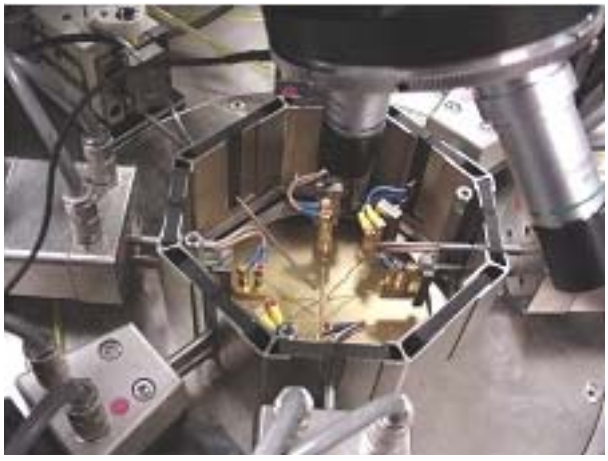

Figure 6.8: The shielded micro-chamber on a Cascade Summit 12k used to protect the DUT (device under test) from EMC disturbances.

7. SiSPET: a tool for studying the gaps between microscopic device architecture fluctuations and compact model parameters

This chapter is based on a joint project between the author and Hans Tuinhout, Philips Research/Eindhoven. This project is the work that resulted in the last papers, Paper V and Paper VI. In this work we used results from all chapters in this thesis; hence the author thinks that presenting this project is a nice way to wrap up the thesis. We start to briefly introduce the purpose of this project; this is followed by a discussion on the implementation of the system. Finally we present our findings and discuss the future of this project.

7.1 Introduction

PMF (matching) of MOS transistors forms a traditional performance limiter for high precision analogue electronic circuit blocks such as A/D & D/A converters, differential amplifiers, comparators, bandgap references, PLL's, etc. [33, 47]. Due to device scaling into the deep-sub micron region, large digital systems and memories in ULSI CMOS technologies now also suffer from yield- and/or performance degradations associated with random parameter fluctuations [40, 61] . These statistical device fluctuations are generally attributed to microscopic device architecture fluctuations (Poisson statistics) associated with physical elements such as dopants, charges, interface states, grain boundaries, edge roughnesses, etc. Considerable effort has been put into understanding and modeling the relations between microscopic device architecture fluctuations and resulting parametric fluctuations [67, 19, 62, 18, 14]. Nevertheless, many inconsistencies and gaps can still be identified in terms of interpretations of the exact impact of fluctuation mechanisms.

One of the problems of parametric mismatch interpretations is that statistical parametric measurements (by definition) form an indirect approach with respect to interpretation of the underlying physical microscopic device architecture fluctuations. One cannot look inside a real transistor to determine what actually causes the observed parametric fluctuations. By using a known source

of the fluctuations this problem could be resolved. However, in reality this is not possible. But by inserting a known fluctuation source in a TCAD environment it is possible to study the effects isolated from other fluctuation sources. Statistical device simulations have proven to be an excellent approach to obtain quantitative insights with respect to the relative importance of physical fluctuation mechanisms [62, 7, 65].

Statistical circuit simulations assess the impact of fluctuations on a circuit level. To accomplish this task these fluctuations must be incorporated into the circuit-simulation. This can be done in two different ways; add a dedicated mismatch model to the circuit simulation [53, 16], or manipulate the model parameters to reflect the fluctuations[19] . The latter approach uses only a standard industry grade MOSFET compact-model (MM11, BSIM4). The circuit-simulator used must provide means to transfer the fluctuations into the model-decks.

By using a TCAD environment with a known source of fluctuations and a modern compact-model with extraction procedure it should be possible to evaluate and compare different modeling approaches in a completely new way, These ideas were implemented as a in-house developed system SiSPET (Simulated Statistical Parameter Extraction Tool)

7.2 The SiSPET system

First we introduce the SiSPET system in a top-down approach. The system comprises of the following subsystems: TCAD environment from Synopsis [63] and a developed random doping fluctuation randomizer 'dr', Paper V. For the compact-modeling part we use the ICCAP system from Agilent [2] both for modeling of IV-curves and extraction of MOS Model 11 parameters. The last subsystem is a collection of Matlab [39] scripts used for direct extraction and statistical analysis. For an illustration of the SiSPET system see figure 7.1. In the coming sections we describe each subsystem separatel

7.2.1 TCAD subsystem

For the TCAD part of this system we use a commercial TCAD solution from Synopsis (ISE TCAD). This system has the usual TCAD tools mentioned in the TCAD chapter of this thesis. This whole TCAD system is controlled by a shell, GENESISe, which provides a graphical interface as well as scripting capabilities. In SiSPET we use the following tools - the device generator MdrawTCL [63] and Mdraw [63] used for the meshing of the structure. The device simulator is dessis [1]. The final processing of the IV-curves is performed by INSPECT [63], this tool also takes care of translating the IV-

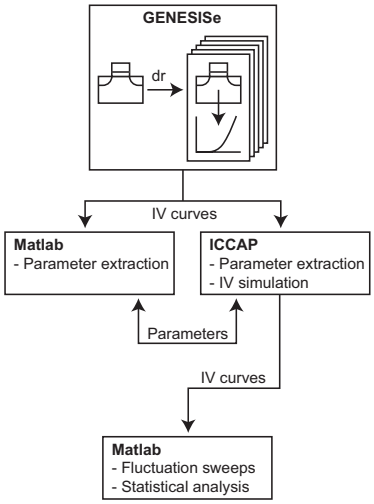

Figure 7.1: Overview of the SiSPET system.

curves to the IC-CAP data format mdm [2] .

7.2.2 Random doping randomizer

The TCAD system employed does not provide a tool to introduce random doping fluctuations into a device structure. Therefore, the author of the thesis developed his own random doping fluctuation randomizer, dr. This tool calculates the random doping fluctuations based on the grid and doping information, and new doping concentrations are generated from Poisson distributions [62] . For the complete source code and documentation for this program see the technical report Paper V. A randomized version of the 90 nm device with HALO is shown in figure 7.2.

7.2.3 ICCAP subsystem

This part of the system handles all issues regarding compact-modeling and parameter extraction. Principally, this subsystem has two purposes in SiSPET; the first purpose is extraction of MOS Model 11 parameters from the TCAD generated IV-data. The second purpose is generation of IV-curves from model parameters, hence different strategies. ICCAP does not have the MOS Model 11 built-in but by using the Philips SIMKIT 2.1 [50] and the Agilent hpeesofsim [3] simulator it is possible to use MOS Model 11[49].

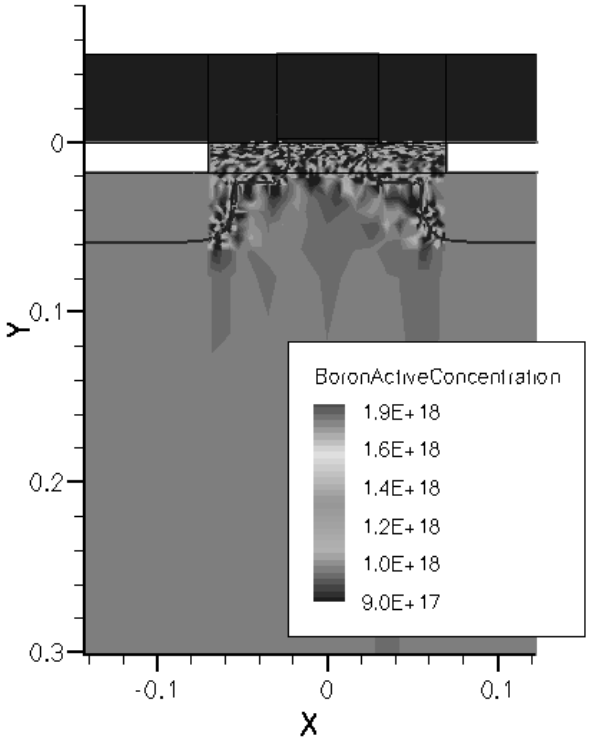

Figure 7.2: A 90 nm MOSFET device with randomized substrate doping. This randomized device is generated with 'dr'

7.2.4 Matlab

The last part of the system is a collection of various matlab scripts that are used for direct extraction of parameters i.e., 3-point extraction of threshold voltage parameters. Simple back-of-envelope type modeling approaches and finally statistical analysis of the results are presented in Paper VI.

7.2.5 The first experiment

The first real study performed with the SiSPET system was the evaluation of different MOSFET fluctuation models that are described in Paper VI. In this study we used all features of the simulation system and it proved it to be very successful.

8. Summary and Future

The work described in this thesis is based on TCAD simulations and high precision parametric mismatch fluctuation measurements and methodology. During this very exciting journey the author have gained experience with all aspects of TCAD simulation. This experience and the collaboration with one of the worlds leading mismatch experts at Philips Research led to the realization of the SiSPET system. This system made it possible for the first time to compare all major metods to model drain current fluctuations of MOSFETs. The SiSPET system will be used for some more fluctuation studies on SOI-MOSFETs. We will also start using the PSP compact model instead of MOS Model 11. We would also like to investigate measured data from a modern 65 nm MOSFET process and verify the results from Paper VI. The complete SiSPET system will also be transferred to Philips Research for further use and development.

Finally the author would like to end this thesis with the words from a leading Linux company:

Have a lot of fun...

9. Summary of Papers

9.1 Paper I

"Investigation of the electrical behavior of an asymmetric MOSFET" In Paper I, the use of a tilted source/drain implantation was suggested and evaluated. The idea behind this paper is that a tilted source/drain implantation would create an asymmetric MOSFET device. This asymmetry would result in an extended LDD region near the drain, thus enabling a higher breakdown voltage. This idea was evaluated by the means of TCAD simulations. The investigation shows that there exists an optimum range of LDD doses where the asymmetric device has a higher figure-of-merit, with regard to breakdown voltage and cut-off frequency, compared to the symmetric MOSFET structure.

9.2 Paper II

"Substrate Resistance Modeling for Noise Coupling Analysis" In Paper II, we presented a physically based Z-parameter model of a representative two-port with all contacts on the surface of a lightly doped substrate. This Z-parameter model is expressed using a one-port resistance model. Interestingly simulations indicate that the coupling does not go to zero as the distance between the circuit blocks increase. It is also shown in this paper that a simple Pi network cannot quantitatively model the coupling between two devices.

9.3 Paper III

"Design and implementation of an ultra high precision parametric mismatch measurement system" This paper discusses the design and implementation of an ultra-high precision parametric mismatch measurement system with integrated statistical data evaluation and mismatch measurement precision monitoring. By adjusting the number of observations used for each mismatch determination, the precision of the mismatch measurement can be increased up to levels that have not been reported so far. Even for extremely sensitive devices such as common-emitter / common-collector BJT pairs we report sub-10 ppm precision performances of the measurement system. To reach such lev-

els, a new so-called intertwined measurement algorithm proved essential to mitigate the impact of (typical 200-ppm) equipment and device (temperature) drifts. This new system opens up new possibilities in terms of being able to characterize the mismatch of much larger devices. For more common devices, the enhanced precision and built-in analysis procedures greatly increase the confidence in the derived statistical results.

9.4 Paper IV

"Identification of a new BJT parametric mismatch phenomenon" During the work that resulted in Paper III we encountered devices from a 0.25 μm BiCMOS technology that showed an unexpected discrepancy in the npn BJT base current mismatch area scaling for one specific geometry only. The following analysis of this phenomenon resulted in Paper IV. Based on TEM and electrical analysis it was concluded that the observed increase of the base current fluctuations is attributable to microscopic fluctuations of the (too small) distance between the emitter's $TiSi_2$ layer and its poly- mono interface. Due to an unfortunate combination of a number of process steps, a marginally thin non-silicided emitter poly silicon layer remains between silicide and mono silicon for a specific emitter geometry range, in which one of our matched pair test structures (1.1x1.1 μm^2) was (fortunately) designed. This study for the first time revealed this new microscopic device architecture fluctuation mechanism that can severely affect the base current mismatch and the yield of high performance bipolar transistors.

9.5 Paper V

"Development of a random dopant fluctuation simulation system-'dr"' This technical report describes my implementation of a random dopant fluctuation (RDF) simulation program. Such a program is used to study the effects of the random positions of doping atoms on the electrical characteristics. The randomizations are based on calculations using the grid and doping files from a TCAD generated device structure. The RDF program was integrated into the framework of the commercial TCAD environment from ISE/Synopsis.

9.6 Paper VI

"TCAD assisted evaluation of MOSFET fluctuation models" In Paper VI we evaluated different MOSFET fluctuation models using the in- house developed system SiSPET (Simulated Statistical Parameter Extraction Tool). The

basic models based on threshold voltage extractions in linear region and saturation were compared to compact-model based approaches (MOS Model 11). The first compact-model based fluctuation model deployed a full extraction of the MOS Model 11 miniset (no scaling) parameters. The full miniset extraction resulted in fluctuations in 10 parameters. This full extraction was then optimized using Pareto analysis resulting in a model where 7 parameters fluctuated, this approach have advantages in terms of extraction. All different modeling approaches were analyzed using RMS calculations and fluctuation sweeps. The result shows that the basic model can be improved significantly by including the gate field dependency on the mobility. If a very precise description of the fluctuations is wanted a compact-model based approach should be employed.

10. Sammanfattning

Denna avhandling handlar om simulering och mätning på avancerade halvledarkomponenter. För att förstå och utveckla komponenter räcker det i allmänhet inte med att göra enkla beräkningar. I de flesta fall så måste man använda sig av datorsimuleringar av både tillverkningsprocessen samt det elektriska beteendet hos komponenten. Denna gren av vetenskapen kallas TCAD (Technology Computer Assisted Design) som kan översättas till Datorstödd teknologidesign. I arbetet som ligger bakom denna avhandling har jag använt mig av de flesta förekommande typerna av TCAD program. Dessa datorsimuleringar har utförts både i 2D och 3D. Jag har även designat några datorprogram som används för att genomföra statistiska TCAD simuleringar. En annan typ av simulering är kretssimulering denna simulering syftar till att beskriva en krets beteende. För att kunna simulera en krets behövs modeller för de ingående komponenterna, kompaktmodeller. Dessa kompaktmodeller är baserade på enkla ekvationer för att beskriva komponentens beteende. Enkelheten hos kompaktmodellerna är avgörande för hur stora kretsar som kan simuleras.

Mätningar på moderna halvledarkomponenter utförs både för att säkerställa prestanda samt för att vidarutveckla existerande komponenter. I detta område har jag arbetat med en speciell typ av mätningar. Denna typ av mätningar kallas 'matchnings' mätningar och syftar till att mäta skillnader mellan komponenter som antas vara identiska. Pga flera olika faktorer är komponenter som designas identiskt lika ej lika. Denna skillnad utgörs ofta av mikroskopiska skillnader hos komponenten såsom: linjebredds variationer, korngränser hos polykisel-styret samt slumpmässiga dopvariationer. Dessa effekter studeras bäst med speciella mätstrukturer såsom det matchade paret. I ett matchat par sitter komponenterna väldigt nära varandra och har en likartad omgivning. Matchningsmätningar är en av de mest utmanande mätningar man kan göra, då man ofta mäter storheter som ligger långt under instrumentens noggrannhets specifikation.

10.1 Artikel I

"Investigation of the electrical behavior of an asymmetric MOSFET" Denna TCAD studie beskriver det elektriska beteendet hos en asymmetrisk MOS-

FET. Asymmetrin skapas genom att vinkla implantationsvinkeln för source och drain under processimuleringen. Denna asymmetri ökar MOSFET komponentens genombrottsspänning för vissa LDD doser. Undersökningen visar att det existerar ett optimalt område för LDD doser där den asymmetriska komponenten har en högre genombrottsspänning samt cut-off frekvens jämfört med den symmetriska MOSFET komponenten.

10.2 Artikel II

"Substrate Resistance Modeling for Noise Coupling Analysis" I denna artikel presenterar vi en fysikalisk Z-parameter modell för en tvåport med alla kontakter på ytan av ett lågdopat substrat. Simuleringar indikerar att kopplingen mellan kontakterna ej går mot noll då avståndet ökar, utan att ett mättnadsvärde på kopplingen erhålls. I denna artikel visar vi även att ett enkelt Pi nätverk ej kan beskriva kopplingen kvantitativt.

10.3 Artikel III

"Design and implementation of an ultra high precision parametric mismatch measurement system" I denna artikel studerar vi konstruktionen och implementeringen av ett parametriskt mismatch mätsystem med ultra hög precision. Detta system har även en integrerad statistisk utvärdering av mätdata samt övervakning av precisionen för mismatchmätningen. Genom att justera antalet observationer för varje mismatchbestämning kan precisionen justeras till nivåer som ej tidigare publicerats. Detta även för extremt känsliga komponenter som bipolära transistor par. I denna artikel rapporterar vi mätningar av precisionen på nivåer under 10 ppm, för att åstadkomma en sådan precision behövdes en ny algoritm som presenterades i denna artikel. Detta system öppnar nya möjligheter att mäta mismatch på stora komponenter.

10.4 Artikel IV

"Identification of a new BJT parametric mismatch phenomenon" Under arbetet som resulterade I artikel III påträffades komponenter från en 0.25 μm BiCMOS teknologi som uppvisade en avvikelse från areaskalningen för basströmmen för endast en geometri. Analysen av denna avvikelse ledde till Artikel IV. Denna artikel baseras på TEM och elektriska mätningar. Slutsatsen var att avvikelsen berodde på mikroskopiska fluktuationer av avståndet mellan emitterns $TiSi_2$ lager och dess gränsskikt mellan poly-mono. Detta var första gången som denna nya mikroskopiska fluktuation presenterades.

10.5 Artikel V

“Development of a random dopant fluctuation simulation system-’dr’“ För att kunna simulera slumpmässiga variationer i dopkoncentrationen med hjälp av TCAD behövs en simulator. I denna tekniska rapport beskriver jag utvecklingen av en sådan simulator som kallas ’dr’. Genom att analysera komponentstrukturen och använda en Poisson slumptalsgenerator kan strukturer som uppvisar slumpmässiga variationer av dopkoncentrationen genereras.

10.6 Artikel VI

“TCAD assisted evaluation of MOSFET fluctuation models” I Artikel VI studerades olika modeller för att beskriva fluktuationer hos MOSFET komponenter. Vi använde ett system som utvecklades för detta syfte SiSPET (Simulated Statistical Parameter Extraction Tool) där programmet från Artikel V var en viktig beståndsdel. Vi studerade enkla modeller med parametrar från extraktioner av tröskelspänningen och jämförde dessa med modeller baserade på kompaktmodeller (MOS Model 11). Genom att använda ytterligare en parameter i de enkla modellerna kunde dessa förbättras med en faktor 4 i det lineära området. De modeller som baserades på MOS Model 11 visade sig vara överlägsna då det gällde att prediktera fluktuationerna i utkarakteristiken jämfört med de enklare modellerna.

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