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Potential-Induced Degradation and possibilities for recovery of $CuIn_{1-x}Ga_xSe_2$ thin film solar cells

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Licentiate thesis

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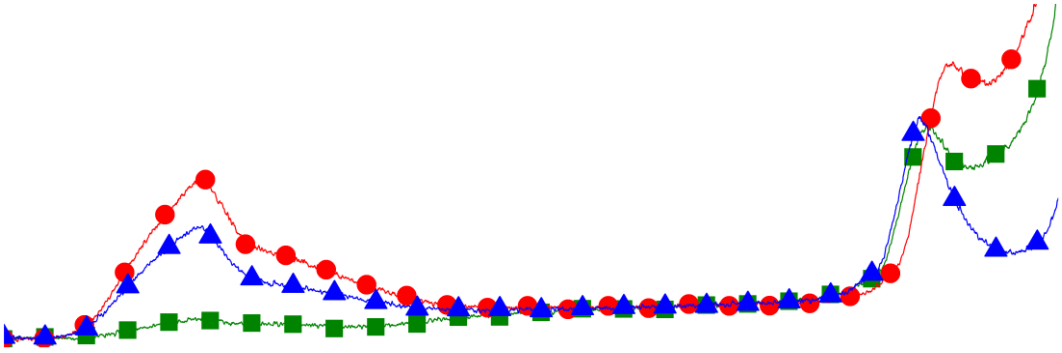

Abstract

The long-term performance of solar modules is of key importance to achieve profitable solar power installations. In this work, the degradation mechanism potential-induced degradation (PID) was investigated for $CuIn_{1-x}Ga_xSe_2$ (CIGS) thin film solar cells. PID is caused by a combination of certain system voltage situations and environment conditions, such as temperature and humidity. The conditions for PID were reproduced in the lab, using small test cells. A voltage was applied between the solar cell back contact and the rear side of the glass substrate while heating the samples to a temperature of 85°C.

Similar to crystalline silicon technology, CIGS solar cells were found to be susceptible to PID. One critical parameter for the degradation behavior is the choice of substrate and its ability to release Na during applied bias. The degradation was found to be linked with Na migration from the substrate into the devices. Solar cells, which were fully deteriorated in terms of electrical performance by PID, were found to have a substantially increased Na concentration. However, solar cells grown on Na free and high resistivity substrates were observed to be PID-resilient.

The degradation was shown to partly be non-permanent. Fully degraded CIGS solar cells could recover electrical performance to a certain degree. Three different recovery methods were applied *(i)* a passive recovery in darkness at room temperature, *(ii)* accelerated recovery with a reversed bias as compared to the PID treatment and *(iii)* etching and replacement of the top window layers followed by reversed bias. Recovery to over 90% of the initial efficiency was possible. However, the recovery rate varied depending on the recovery method. The accelerated method was found to reduce the concentration of Na in the buffer layer and interface volumes. The etch recovery method, which consists of renewing window and buffer layers further strengthen the hypothesis that a major part of the degradation could be attributed to the buffer layer and its interface to CIGS.

The importance of the buffer layer in PID was further highlighted in the experiment where the standard CdS buffer layer was substituted with Zn(O,S). Both types of solar cells degrade in the PID conditions. Zn(O,S) cells exhibited ohmic current-voltage relationship (no diode characteristics) in the degraded state, while the CdS counterpart had some degree of diode behavior. During recovery with the accelerated method, the CdS cells restored both current-voltage and capacitance-voltage behavior to larger extent than the Zn(O,S) cells. For the latter, the efficiency stayed close to zero throughout the recovery period.

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1. Introduction

1.1 Background

The global demand for energy has been ever increasing since the industrial revolution started in the 18th century. Throughout this period, the vast part of the world's energy supply has been based on fossil fuels in all sectors such as industry, transportation, and electricity. We all know that fossil fuels are a limited resource and in the last decade, more sustainable energy technologies have gained impact.

Technology advances within, for example, the fields of electric and hybrid vehicles, energy storage, energy efficiency, and smart grids, enable the potential of renewable electricity sources and increase the importance of electricity as energy carrier. Electricity production is still dominated by fossil fuel but in relative numbers, the aggregated production from wind, solar and geothermal increases the most [1].

The solar cell market has grown from installing less than 1 GW_p of photovoltaic (PV) capacity in 2003 to installing 40 GW_p in 2013. The world's accumulated installed PV capacity is now 140 GW_p, producing 0.87% (165 TWh) of the worlds´ total electricity [2]. This is still only a small fraction of the total PV potential and the market continues to grow. So far, crystalline silicon (c-Si) technology has dominated the market, but thin film technologies are being developed with the potential to cut PV production cost.

The semiconductor $CuIn_{1-x}Ga_xSe_2$ (CIGS) is one of the absorber materials used in thin film PV (TFPV) and it has the highest reported lab scale solar cell efficiency amongst the thin film technologies, 21.7% [3], [4]. To become a successful technology in the PV market, not only efficiency is important. In the end, the economics of a PV installation have three key parameters: efficiency, reliability and lifetime which all influence the ultimate measure of a PV installation - the levelized cost of electricity (LCOE).

To illustrate the importance of stability in PV, three cases are outlined. First imagine an installation with a certain initial capacity of 100% and a lifetime of 25 years. Then consider the three cases: 0%, 1% and 2% annual degradation. For all the cases, every other aspect of the installation is considered the same and the only difference is the annual degradation rate. The produced electric energy per year, normalized to the first year, is depicted in Figure 1. After 25 years of operation the installation with 1% annual degradation rate produces at 75% of initial installed capacity, while the installation with 2% annual degradation rate only produces 50%.

The total produced electric energy of each installation can be calculated as the plant capacity versus year integrated over the 25 years of operation. The results are presented in Table I, where the installation with 2% degradation rate is considered the reference installation. Compared to this case, the 1% installation produces 17% more electric energy (dark grey area in Figure 1) and the non-

degrading installation produces 33% more (dark grey + light grey areas in Figure 1)

These facts imply consequences for the economical calculations and profitability of the installation that any potential PV plant buyer must consider. Since the income of an installation is directly proportional to the produced electrical energy, a more productive installation motivates a higher purchase price. If the 1% installation is less than 17% more expensive than the 2% installation, it is still the most economically favorable choice. Further, it would be worth to invest 33% more in a completely degradation free installation, compared to the 2% degradation case.

The cost of the solar modules constitutes approximately 30% of the total system cost [5]. Under the assumption that all system degradation can be attributed to the solar modules, module prices of +57% and +110% are motivated. This is clearly of importance to the solar module producers, where a more reliable product with more generous warranties motivates a higher selling price.

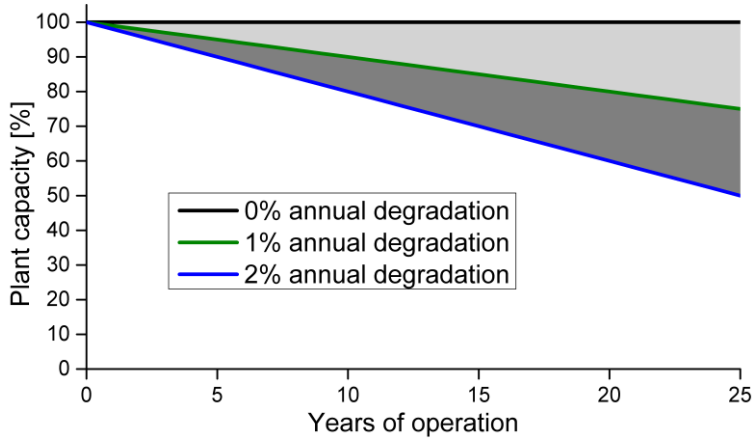

Figure 1. Plant capacity in the cases with 0%, 1% and 2% annual degradation respectively. The gray shaded areas illustrate the difference in produced electric energy between the three cases.

Table I. Quantified extra energy yield of the different cases, when compared to the installation with 2% annual degradation rate.

Annual degradation rate	**Extra energy yield**
0%	+33%
1%	+17%
2%	Reference installation

A solar module can fail or degrade due to various mechanisms. The cover glass and frame can break due to mechanical load, the encapsulant can turn yellow due to UV irradiation, interconnects can break and hot-spots can occur just to name a few. For c-Si modules, these and other degradation mechanisms are tested in the IEC 61215 standard testing protocol [6] and a module producer may estimate module lifetime and warranty based on the results. Thin film modules are tested according to the IEC 61646 standard [7].

Potential induced degradation (PID) is a degradation mechanism, which is not covered in the IEC standards above, but an IEC test procedure for PID is under development. PID is related to the high system voltages in a PV installation (typically 600-1000V) and is one of the factors important to the reliability of PV. In this licentiate thesis, PID for the CIGS technology is investigated on lab scale solar cells to gain insight into the origin of this degradation mechanism.

1.2 Solar cell basics

1.2.1 The pn-junction

To convert solar radiation into electricity, the first step is to absorb the photons. In a semiconductor like CIGS, electrons in the valence band are excited to the conduction band when photons are absorbed by electrons. A hole (absence of an electron) is thereby created in the valence band. Absorption in the semiconductor can occur if the energy of the incident photon is higher than the bandgap of the CIGS. Lower energy photons are transmitted through the CIGS material.

Once the electron-hole pair has been created, the electron needs to be separated from the hole and collected before recombination occurs. In all major PV technologies on the market, separation and collection of charges are achieved through a solid-state pn-junction. A pn-junction is created when a p-doped semiconductor comes into contact with an n-doped semiconductor, either of the same material (homojunction), e.g. n-Si/p-Si, or of different materials (heterojunction), e.g. n-CdS/p-CIGS.

Different Fermi level positions with respect to the conduction and valence band edges on both sides of the junction (due to the different doping) and the fact that they must be aligned in equilibrium, lead to formation of a built-in electrical field. When CdS is brought in intimate contact with CIGS, electrons from the n-doped CdS start to diffuse into the CIGS due to the concentration gradient, leaving ionized dopant atoms (donors, N_D) in the CdS close to the interface between the two layers. The opposite holds true for the p-doped CIGS with holes diffusing towards the CdS and leaving ionized dopant atoms (acceptors, N_A) in the p-CIGS close to the interface.

As more and more uncompensated static charge appears on both sides of the junction, the potential difference leads to a growing electric field, which counteracts the diffusion. At some point equilibrium is reached and the region with the electric field is almost completely void of free charges. This region is referred to as the depleted layer and can extend on both side of the interface as illustrated in Figure 2.

Charge neutrality must be preserved, so the total charge on the n-side must equal the total charge on the p-side according to Equation (1). This means that the depleted layer extends further into the lower-doped side of the junction. In the CIGS/CdS pn-junction, the CdS is often assumed to be significantly higher doped than the CIGS ($N_D \gg N_A$). This is, in normal devices, approximated as a single-sided junction, where the depleted layer only extends into the CIGS. The total width of the depleted layer of an arbitrary pn-junction is given by Equation (2).

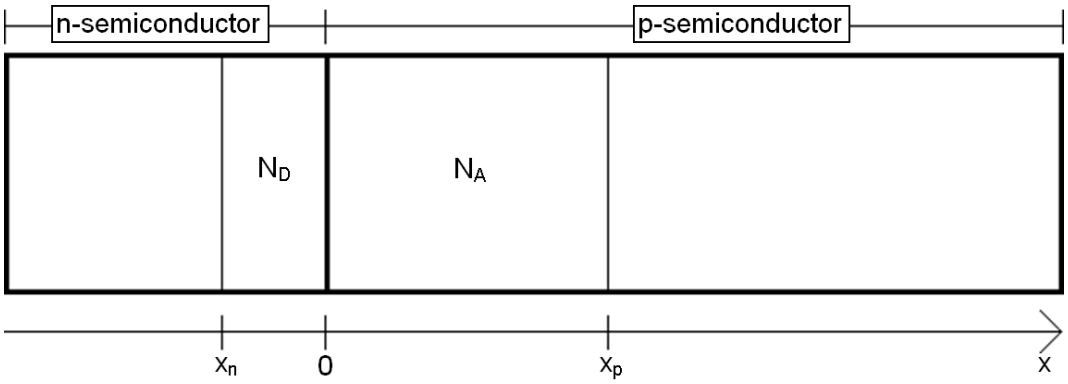

Figure 2. Principal view of a pn-junction and the depleted layer extensions on both sides.

$$N_A|x_p| = N_D|x_n| \quad (1)$$

$$W_D = |x_p| + |x_n| \quad (2)$$

1.2.2 Measuring the depleted layer width of a pn-junction

For a single-sided pn-junction with lowly doped p-side, the depleted layer width under DC-bias is derived in [8] and here reproduced in Equation (3)

$$W_D = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{qN_A}\left(\Psi_{bi} - V - \frac{2kT}{q}\right)} \quad (3)$$

The applied DC-voltage, *V*, is considered positive for a forward-biased junction and negative for a reverse-biased junction. In Equation (3), this means that the width of the depleted layer is reduced or increased when the junction is in forward or reverse bias respectively. This is the core of the capacitance-voltage technique (C-V), where the pn-junction is viewed as a parallel plate capacitor with the depleted layer as the dielectric. Once capacitance is measured, the corresponding depleted layer width is calculated according to Equation (4).

$$W_D = \frac{\varepsilon_0\varepsilon_r A}{C} \quad (4)$$

To measure capacitance at a given DC bias an AC voltage is applied, superimposed on the DC bias. The AC signal generates a small charge change at the edge of the depleted layer and from the current response, charge and hence capacitance can be extracted. In this work, a C_P-R_P model is used, i.e. a capacitor is in parallel with a resistor. The measure of quality is the phase angle, since a pure capacitor would shift the current 90 degrees from the voltage. Phase angles close to 90 degrees are seldom observed for the CdS/CIGS pn-junction, with values around 80 degrees being more common.

1.2.3 Ideal pn-junction under bias and illumination

The most important characteristics of a pn-junction are obtained by using current–voltage (I-V) measurements. Preferably, I-V measurements are done in a four-point-probe setup, where voltage is applied between one pair of probes and the current is measured in the other pair. This eliminates the influence of contact

and cable resistances and ensures high quality measurements. The I-V relationship of an ideal pn-junction is given by the Shockley equation, the ideal diode law:

$$I = I_0\left(e^{qV/kT} - 1\right) \tag{5}$$

An ideal solar cell in darkness behaves as a regular pn-diode and follows Equation (5). In reverse bias, the electric field across the junction becomes stronger and the barrier for the majority carriers increases. This reduces the majority carrier diffusion current and ideal pn-junctions under reverse bias have essentially insulating properties. Only a very small reverse current, the reverse saturation current, I_0, can flow through the negatively biased junction. In forward bias, the barrier for the majority carriers is decreased and diffusion of majority carriers over the junction is increased. The current increases exponentially with a linear increase in voltage, as seen in Equation (5).

Under illumination electron-hole pairs are generated from photons with higher energy than the bandgap of the semiconductor and these can, upon separation, contribute to a current. For p-type absorbers, free electrons excited in the neutral bulk of the absorber, i.e. away from the depleted layer, first must diffuse to the edge of the depleted layer from where the electric field can sweep them to the other side of the junction. In the simplest view, this light generated current, I_L, is independent of junction voltage and is an additional minority-carrier current that is superimposed on the ideal diode characteristics.

Two points on an I-V curve, shown in Figure 3, are especially important for characterizing illuminated solar cells: the zero-bias point and the zero-current point. The former gives the short circuit current (I_{sc}) of the device, which in the ideal case is equal to I_L. The latter gives the open circuit voltage (V_{oc}) of the device, at which I_L cancels out the forward diode current depicted in Equation (5). Between these two points is the operating range of the solar cell, where the incident light is converted to electrical power by the device. At any point on the curve, the produced power is the product of voltage and current. The output power peaks at the maximum power point (MPP), with corresponding voltage and current values, V_{mpp} and I_{mpp} respectively. The fill factor (FF) is defined as the ratio $FF = \left(V_{mpp}I_{mpp}\right)/(V_{oc}I_{sc})$.

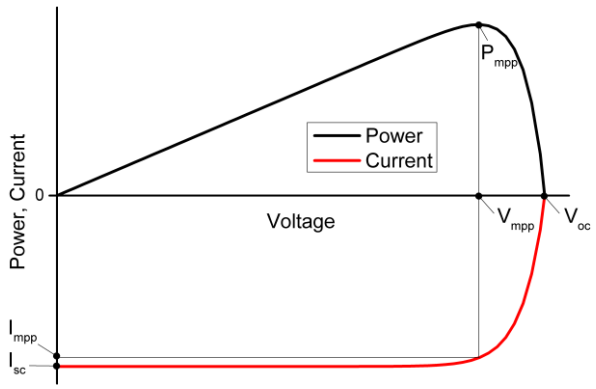

Figure 3. I-V and P-V curves of a ideal solar cell and how the different parameters are extracted.

1.2.4 The one-diode model

The previous section considered an ideal solar cell and its relation to the ideal diode law. However, in real solar cell devices parasitic resistances are always present. One common way to electrically describe a solar cell is with an equivalent circuit consisting of a light-dependent current source, a diode and two resistors. This is referred to as the *one-diode model* and is depicted in Figure 4. Considering this equivalent circuit, the relationship between current and voltage can be derived from the ideal diode law in Equation (5) by including voltage loss over the series resistance and current loss through the shunt resistance. The current-voltage relationship according to the one-diode model is depicted in Equation (6).

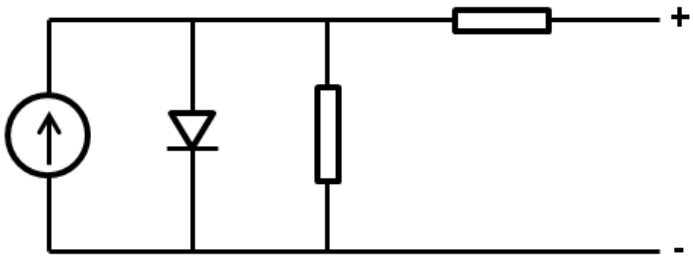

Figure 4. Equivalent circuit used in the one-diode model.

$$I = I_L - I_0\left(e^{\frac{q(V+IR_S)}{nkT}} - 1\right) - \frac{V + IR_S}{R_{SH}} \quad (6)$$

From Equation (6), four characteristic parameters of the device can be identified: R_{sh} (shunt resistance), R_s (series resistance), n, and I_0 (the diode parameters). Shunt resistance represents the sum of conductive paths between the p- and n-terminals. Through these paths, current can pass internally in the device rather than in the external circuit. Ideally this resistance is infinite, meaning that there are no conductive paths between the contacts.

The series resistance is the sum of all resistance that the current experiences while being extracted from the device. Charge carriers are generated over a large volume and during the travel to the terminals of the device, the solar cell materials impose resistance. Typically, this is due to limited conductivity of front and back contacts but it can also result from very low doping of the absorber.

The influence of R_{sh} and R_s on I-V characteristics is visualized in Figure 5a) and b), respectively, with Equation (6) used to calculate the curve. All parameters, except R_{sh} and R_s, respectively, were kept constant. In a) FF is decreased when R_{sh} is decreased. Severely shunted devices exhibit V_{oc} loss and the characteristic linear slope is observed for negative and moderate positive voltage. In b) FF is decreased when R_s is increased, since the slope of the I-V curve around V_{oc} decreases with increased R_s. In both cases, the conversion efficiency of the solar cell is decreased.

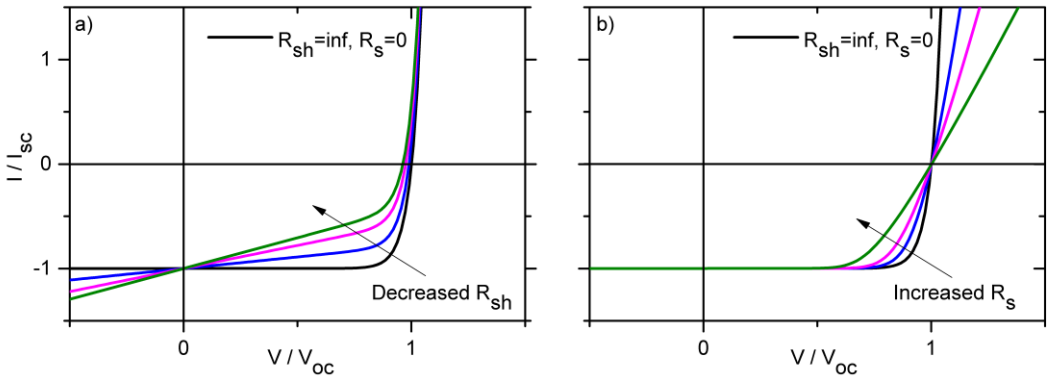

Figure 5. Impact of a) R_{sh} and b) R_s on I-V curves according to the one-diode model. The black curve in both plots represents the ideal case without parasitic resistances.

To relate the diode parameters, n and I_0, to physical attributes is a bit more complex. In a wider sense, these parameters describe the quality of the p-n junction. The ideality factor, n, is a parameter that indicates how closely a pn-junction device follows the ideal diode law. During the derivation of the ideal diode law in Equation (5), recombination in the depleted layer is assumed to be zero, which yields n = 1. On the other hand, when recombination in the depleted layer dominates, n = 2. In the one-diode model, the ideality factor is used as a fitting parameter to describe the recombination mechanisms present in the device. The saturation current, I_0, is related to the amount of recombination and it is a measure of how much current leaks through the device in reverse bias, assuming ideal diode behavior. The larger the recombination is at reverse bias, the larger I_0 becomes as more current can flow through the device.

1.3 The CIGS based solar cell

The thin film stack, constituting our typical CIGS-based solar cell is shown in Figure 6. Starting from the bottom of the stack, a substrate is used to support the structure. Mo back contact, CIGS absorber layer, CdS buffer layer, and ZnO front contact structure are deposited onto the substrate.

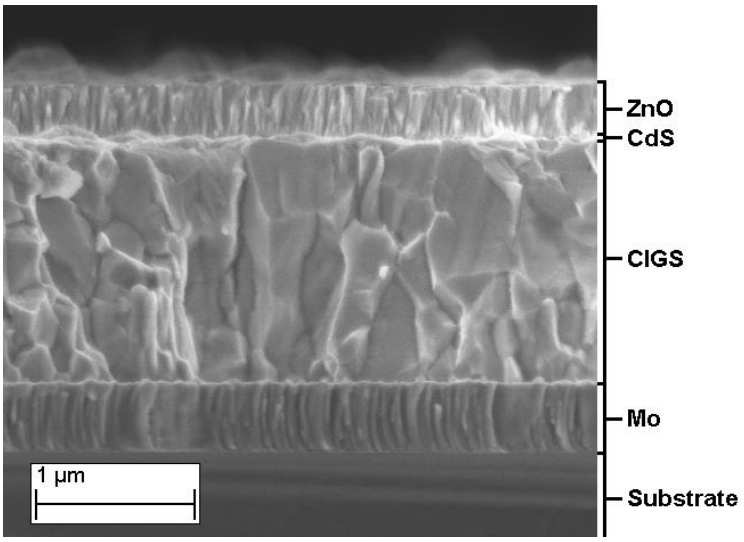

Figure 6. Cross section of a CIGS solar cell as seen with Scanning Electron Microscopy (SEM)

1.3.1 Manufacturing CIGS cells in our lab, the baseline process

In the baseline process, described in detail in [9], we use soda lime glass (SLG) substrates with a thickness of either 1mm or 2mm. The first step in the process is to clean the substrate. This is a very important step because it removes contaminants from the substrate that would be detrimental to the solar cell performance. Cleaning includes heating of substrates to 60 °C in water with a detergent, applying ultra-sonic to the cleaning bath, several rinse steps in heated water and ultrasonics followed by a drying step.

Mo back contacts are deposited in an inline DC magnetron sputtering tool. Inside the sputter chamber, substrates are mounted vertically on a holder that during deposition pass in front of stationary targets. Deposition processes are controlled with a programmable logic controller (PLC) and the tool offers good possibility to vary the process parameters, such as pressure, power, gas composition and scan speed.

Currently, the lab comprises two different tools for depositing the CIGS layer by co-evaporation. The CIGS deposition tool that was used in this thesis work is a batch tool, where the Mo coated substrates are placed in a stationary holder above the four stationary evaporation sources. Quartz IR lamps supply heat to the substrates and the temperature is controlled via a calibrated thermocouple inserted in the substrate holder. This batch tool uses a mass spectrometer to measure the evaporation rates of Cu, In and Ga, while Se is evaporated in excess. The signals from the mass spectrometer together with a feedback control loop are used to regulate the power to the metal sources to achieve the set evaporation profiles. Virtually any CIGS process can be realized in this system and both the evaporation and temperature profiles are defined in a computer file. The computer is equipped with a logging system so the integrity of each deposition can be investigated by examining the process log files.

The pn-junction of the CIGS device is formed by applying a CdS buffer layer. This is accomplished in a chemical bath deposition (CBD) where the samples are immersed in a process beaker containing a mixture of three aqueous solutions: CdAc as the Cd source, $SC(NH_2)_2$ (Thiourea) as the S source, and NH_3 as complexing agent and for process pH control. The beaker is subsequently immersed in a heated water bath at 60°C and the film growth is stopped after 8 minutes and 15 seconds, where after the sample is thoroughly rinsed and dried.

Finally, a front contact is deposited on top of CdS. A highly *resistive* un-doped (intrinsic) zinc oxide layer (i-ZnO) is first deposited with RF magnetron sputtering to minimize conductive paths from front to back contacts, i.e. to minimize shunt conductance. A highly *conductive* aluminum-doped zinc oxide layer (ZnO:Al) is the transparent conductive oxide (TCO) then used as the front contact. These two layers are often referred to as the window layer and are deposited subsequently in the same RF sputter tool.

To enable the use of a thin TCO layer, i.e. highly transparent but also more resistive, a current-collecting metal grid with a contact pad for the measurement probe is deposited on top of the TCO. The grid is a Ni/Al/Ni stack, evaporated with electron beam onto the TCO through a shadow mask.

1.3.2 The CIGS process used in this work

In this work, all CIGS absorber layers for all samples were deposited in our batch tool, described in section 1.3.1. The same evaporation rate profiles and substrate temperatures were always used. This process is designed to mimic the deposition in the CIGS deposition tool described in [9]. In this tool, three spatially dispersed and directional metal sources, one for Ga, Cu and In respectively are used. The process in the in-line tool was investigated in previous work: substrate temperature and metal evaporation rates were measured as function of time. With this information, it was possible to transfer the process from the true in-line tool to our batch reactor.

Normalized measured metal rates and substrate temperature of the simulated three-source in-line process are shown in Figure 7. In the grey-shaded areas, part of the heat-up and cool-down parts of the process is shown. Deposition of the CIGS layer onto the substrates takes place within the time-frame of the white-shaded area, which is less than 20 minutes. This process yields a linearly band-gap graded CIGS absorber with a [Ga]/([Ga]+[In]) ratio from approximately 20% at the CdS/CIGS interface to approximately 60% at the CIGS/Mo interface, because of the offset between Ga and In rates. It is a process that never experiences a Cu rich stage during the growth, i.e. the accumulated [Cu]/([Ga]+[In]) ratio is throughout the process always below unity.

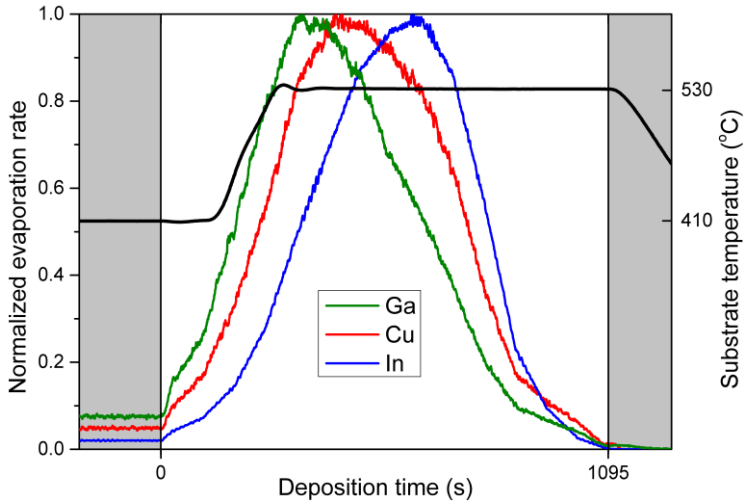

Figure 7. Normalized evaporation rates of the three-source in-line CIGS process used in this work (left y-axis) and substrate temperature (right y-axis).

1.3.3 Na in CIGS

One of the first reports on Na in CIGS is from Hedstrom et. al. in 1993 [10], where CIGS was grown on SLG, borosilicate, sapphire and sintered alumina substrates. The highest solar cell efficiency was observed for the SLG substrate, along with increased preferential orientation of the chalcopyrite crystals in the 112-direction as seen with x-ray diffraction (XRD). Importantly, Na was found in the CIGS layer grown on SLG. At that time, the authors could not decouple the effect on electrical performance from the texturing of the crystals and the Na concentration. Later, it was shown that the presence of Na increased V_{oc} and FF compared to the Na-free counterparts and the best solar cell devices in the study were made on Na-containing CIS layers [11].

Another study at that time (1994) confirmed the effect of Na on the electrical properties of CIGS. Na was implanted to the level of $1 \cdot 10^{15}$ atoms/cm^3 in CIGS deposited on sapphire substrates, and this increased the conductivity of the layer to similar values as CIGS grown directly on SLG. CIGS grown on sapphire substrates without subsequent Na implantation displayed several orders of magnitude lower conductivity [12].

Since then, numerous reports on the topic have been published. The effect of Na on conductivity, V_{oc} and FF was also observed by Contreras et. al. [13]. Furthermore, the authors could identify a higher free carrier concentration in the CIGS layer and they proposed that the beneficial impact on solar cell performance of Na, was that it reduced the number of compensating donors, e.g. In_{Cu}, and hence increased the effective p-doping. This has been supported by several other studies [14]–[16] and is the most widely accepted theory of the role of Na in CIGS.

However, too much Na in CIGS has been shown to have detrimental effects on the solar cell performance. The positive effect on V_{oc} and FF was observed for moderate Na concentration in CIS, while an excessive amount was shown to degrade the performance [17]. One proposed explanation is that after suppressing the major part of the In_{Cu} donor defects, adding more Na leads to reduction of copper vacancies [18], which in turn have been proposed to be the major intrinsic acceptor dopant of CIGS [19], [20].

Na can be introduced prior, during and post fabrication of the CIGS absorber layer and depending on the substrate, various Na supply methods can be used. In the case of SLG substrates, high temperature during CIGS deposition causes Na to diffuse from the SLG through the Mo back contact and become available for incorporation in the growing CIGS film. The properties of the Mo layer, such as porosity and presence of oxygen have been shown to greatly impact the Na diffusion process [21]–[24].

If non-Na-containing substrates or if Na barriers are used, other methods for Na incorporation are applied. For example, Na-doped Mo can be used as the back contact [25], NaF can be deposited on top of the Mo back contact as a precursor layer prior to CIGS growth [26] and Na can also be introduced with a post-deposition treatment of the CIGS layer [27]. Each incorporation method carries features that govern the limitations, possibilities, drawbacks and controllability of that specific method.

2. Potential Induced Degradation

2.1 Introduction

A conventional grid-connected PV system consists of several series-interconnected solar modules. By connecting the modules in series, the voltage is increased by a factor equal to the number of modules, while the current is kept at the level of one module. With this configuration, resistive losses in the cabling can be kept at a minimum, since these losses scale with the square of the current in the system. High system voltage is also considered economically favorable because of reduction of wiring and inverter costs [28].

The DC power from the modules is fed into an inverter, which transforms the PV-generated DC into AC with desired properties for feeding power to the local electric grid. Three possible grounding schemes can be used in an installation: negative functional grounding (negative contact of PV system connected to ground), positive functional grounding (positive contact of PV system connected to ground) or floating (no grounding of the PV contacts). The chosen grounding scheme affects the potential difference for each module with respect to ground according to Figure 8. Each module will be at a certain potential above or below ground, depending on the position in the string and type of grounding scheme.

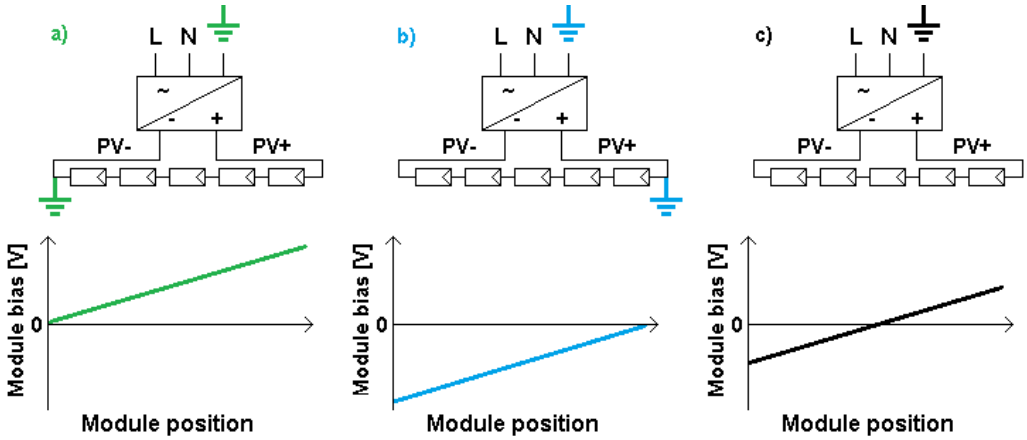

Figure 8. Module bias with respect to ground for a) negative functional grounding, b) positive functional grounding and c) no functional grounding, respectively.

Regulations from the European Union state that all metal parts of the installation such as mounting structure, brackets and module frames should be connected to ground for safety reasons. Since the modules are deployed outdoors, humidity can create a conductive layer on the back and front of the modules. This will connect these areas of the module, via the mounting brackets and frame, to ground. Based on Figure 8 and with the backside of the module connected to ground, a voltage, dependent on the position in the string, between the backside of each cell and backside of the glass is established. Even though the encapsulating materials are selected to be insulators, a leakage current can be observed from the active solar cells to ground. Several different leakage current paths from the solar cells in the module can be identified and are described by del Cueto [29].

Different module encapsulation schemes will have different possible paths for the potential-difference induced leakage current. The magnitude of these currents will be governed by the properties of the encapsulant materials. It is also known that the environmental factors at the installation site, such as temperature and humidity will influence the magnitude of the leakage current [30], [31] in conjugation with the voltage level in the installation determined by the module connection scheme and solar irradiation. The influence of the environmental parameters on the total leakage current was measured from 5pm to 9am by Hacke et. al. [32]. The leakage current strongly peaked during morning hours when the module face was covered with morning dew.

Crystalline silicon cells are commonly equipped with a silicon dioxide (SiO_2) front surface passivation layer and a silicon nitride anti-reflection layer. In this case, Swanson et. al. names the origin of the degradation due to system voltage and leakage current as a *polarization effect* [33]. The SiO_2 layer, as deposited, comprises a fixed positive charge at the solar cell front interface to repel positive charge carriers (holes). This reduces surface charge recombination and hence increases efficiency. The fixed positive charge in the SiO_2 layer can be compensated end even overcompensated by negative charge accumulation due to the leakage current, which will diminish the field effect passivation of the SiO_2 layer. As a consequence, the surface charge recombination will be increased and the efficiency of the silicon solar cell will be reduced.

In the literature there are several reports on the effect and origin of PID for the silicon technology, but for TFPV technologies little has been reported up to now with respect to PID. Since TFPV modules also are used in high voltage system configurations, negative effects due to high voltage stress, similar to those encountered in silicon, are imminent also for TFPV. Olsson et al. present an investigation on CdTe modules, where modules operated at negative bias suffered from degradation [34]. The larger negative bias, the larger the degree of degradation. In this case, the degradation mechanism is different from the polarization effect described by Swanson. Here, Na ions were hypothesized to migrate from the SLG superstrate, through the P1 laser scribes and into the semiconductor layers of the CdTe solar cell stack. This led to decreased shunt resistance of the module, which in turn led to reduction in efficiency.

From the reports cited above, it is clear that the polarity of the voltage between the module and ground is deciding if the modules suffer from PID or not. CdTe modules and modules with p-type Si solar cells degrade at negative bias, while n-type silicon modules degrade at positive bias. With Figure 8 in mind, the polarity of the module bias is determined by the grounding scheme and detrimental biases can be avoided by using correct grounding schemes. However, when using a transformer-less inverter, functional grounding is not feasible. The module string is in this case at floating potential, with half of the string at positive bias and half at negative bias. Development of PID-free solar modules, regardless of system configuration, will promote a larger degree of freedom of system designs and alleviate constraints on inverter choice. Hence it is important to understand the root causes of PID and to find inexpensive methods to mitigate them.

Even though most of the research on PID has been dedicated to crystalline silicon technology, thin-film solar modules are also prone to system voltage degradation mechanisms. Leakage currents and ionic transport could also occur for CIGS modules, since part of the materials used in the module package is the same as for Si and CdTe modules. In the case of CIGS modules, SLG is commonly used as both substrate and front cover in industrial production. Alternative substrate materials are used both in industry and research, for example stainless steel [35], [36], polyimide film [37] or alkali-free glass.

2.2 Experimental details

As described in the section 1.3.3, the effects on material and electronic properties due to Na in CIGS absorbers have been extensively studied. We found yet another aspect of Na in CIGS, namely that Na migration from the substrate can be the cause for solar cell degradation during PID. For the other alkali element of interest, K, we could not identify any trend that relates K migration to solar cell degradation. In the study in Paper I, we used five different substrates with varying alkali Na and K compositions, as listed in Table II. The SLG substrate was commercially available glass supplied by Thermo Scientific Fisher, while all the other glasses used in this study were research glasses supplied by Corning Incorporated.

Table II. Alkali contents of the substrates and efficiency of the CIGS solar cells as grown.

Substrate name	**Na_2O concentration [mol%]**	**K_2O concentration [mol%]**	**Initial median efficiency**
SLG	~14	~1	15.8%
High Na	>10	<5	12.9%
Na only	>10	not intentionally added	14.3%
Alkali free	not intentionally added	not intentionally added	16.2%
Low Na	<5	<10	13.8%

Due to the large differences of Na content in the substrates, a precursor layer of NaF was used in order to supply Na to the CIGS grown on all substrates, except the SLG reference. Previous work [38] showed that for the CIGS process at hand, a NaF layer thickness of 15 nm is adequate when an alkali-free substrate is used. The intention with the NaF precursor layer was to have similar efficiencies for all the substrates in their initial state, but also to check if the amount of Na provided by the precursor layer could cause the degradation. The resulting cells had median efficiencies of 13 % or higher, but we observed some variations.

Possible explanations for the varying cell results could be other properties than the concentration of Na and K that differed between the substrates. For example, the coefficient of thermal expansion (CTE) has been shown to impact CIGS solar cell efficiency in a previous study [39]. The sample series was processed three times, all with similar trends and spread in efficiency. It is important to point out that in this case, no optimization of the CIGS process was made for the different substrates. The other layers in the solar cell stack were deposited with Ångström baseline processes [9].

2.2.1 The PID contacts

In order to subject the samples to an electrical field across the thickness of the glass, similar to what the solar modules would encounter in a PID situation, two electrical contacts for the external voltage had to be applied. One contact is made to the Mo layer in the cell stack and the other contact to the backside of the glass. The former is trivial and is established by soldering a cable to the Mo as seen in Figure 9a). Since all the cells on the sample share the same back contact, the cable electrode is connected to the back contact of all the cells on the sample.
To establish the contact to the backside of the glass, the first step was to clean the back surface. In our deposition process of the CdS buffer layer, not only the surface of the CIGS, but also the backside and edges of the sample are coated, since the sample is completely immersed in the bath. In industrial production the CdS can be grown on the CIGS surface only, since only that area is exposed to the CBD chemicals.

In order to transfer as many similarities to industrial modules as possible, the rear side and edges of the sample were cleaned by removing the CdS with a hydrochloric acid etch. The cleaned back surface was made conductive by applying a layer of aluminum tape with conductive adhesive. For reproducibility, this step is crucial. Special care was taken to try to achieve good contact over the whole surface to ensure that the applied potential is evenly distributed over the area. Onto the first layer of aluminum tape, a cable with spread wires was placed and covered by another layer of aluminum tape as illustrated in Figure 9b). A schematic cross-sectional view of the sample is seen in Figure 9c). With these contacts, the polarity of the applied external bias can be arbitrarily chosen. For degradation, the rear side of the substrate was connected to the positive output of the power supply and the Mo was grounded. Referring to an in-field installation, this would correspond to the cells being at negative bias with respect to ground.

Figure 9. Electrical contacts implemented for a) Mo and b) rear side of the glass. In c), the schematics are shown.

2.2.2 Treatments

For each of the five substrate types listed in Table II, identical sets of solar cells for three different treatments were prepared: *a)* no stress, *b)* heat stress and *c)* heat plus substrate bias stress, where the latter corresponds to the PID condition. In these experiments, samples with treatment *b)* and *c)* were placed in a furnace at 85°C. Additionally, in the case of treatment *c)* an external substrate bias of 50V was used. Samples with treatment *a)* served as references and were only exposed to ambient temperature and stored in darkness. With these three treatments, effects from the PID treatment could be separated from the ones due to storage in ambient conditions and heat treatment only. The conditions are summarized in Table III. Samples that had been subject to elevated temperature were allowed to cool down to room temperature prior to measurement. The measurements were

carried out for one sample at the time and the samples were placed back in the furnace directly when the measurement was completed.

Table III. Summary of the treatments used in this study.

Treatment name	Letter	Temperature	Voltage bias
Reference	a)	Room temperature	-
Heat only	b)	85°C	-
PID	c)	85°C	50V/mm glass

2.3 Results

The electrical performance of the solar cells was measured initially and after 1, 7, 24 and 50 hours respectively. Samples with treatment *a)* and *b)* showed no changes in electrical performance other than those associated with measurement errors. However, when both substrate bias and heat were used as stress conditions (i.e. PID) the performance of the solar cells degraded.

2.3.1 Electrical characterization

Figure 10 depicts the dependence of the J-V parameters on PID stress duration. At each measurement occasion, stated above, all cells per sample were measured and Figure 10 shows the median value normalized to the initial value.

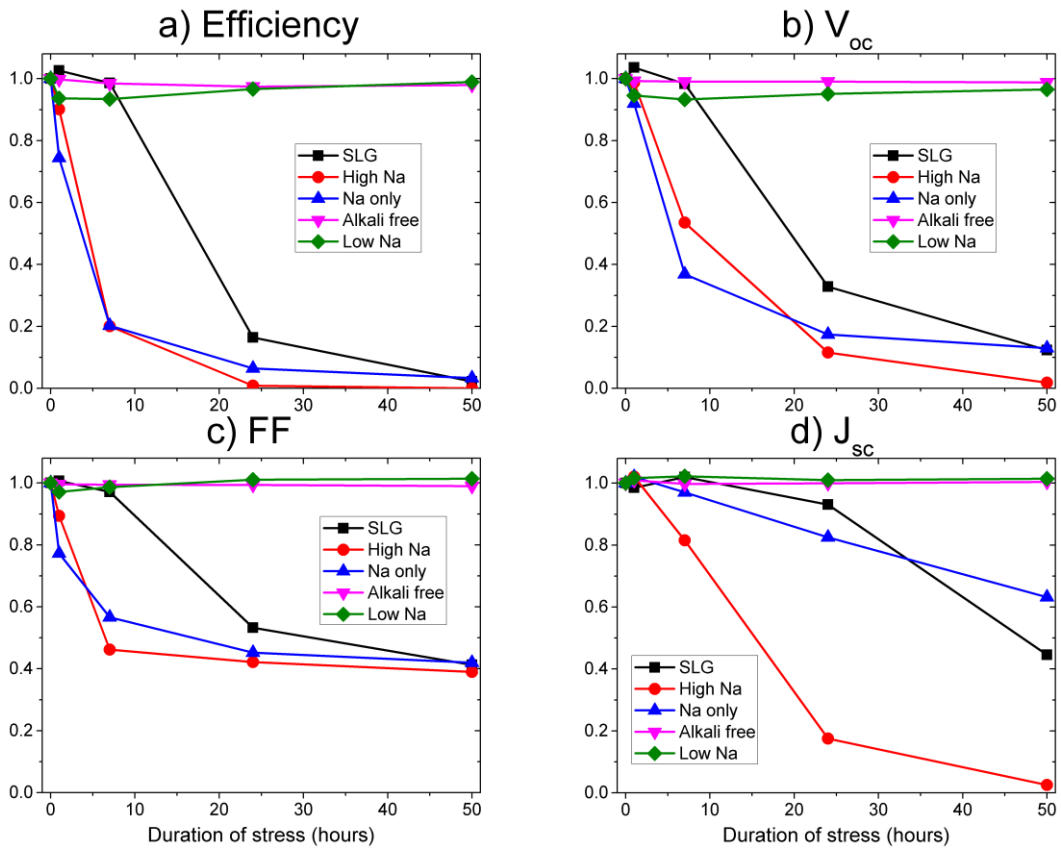

Figure 10. a) efficiency, b) V_{oc}, c) FF and d) J_{sc} of the solar cells grown on the various substrates used in this study during 50 hours of PID stress.

From Figure 10a), two groups of samples can be identified; one group that is mostly unaffected by the PID treatment and one group that suffers severe

degradation down to close to 0% efficiency after 50 hours. The former non-degrading group consists of the Alkali free sample (~0 mol% Na) and the Low Na sample (<5 mol% Na). Throughout the duration of stress of these samples, there are only minor changes to the J-V curves, as can be found in Paper I. After 50 hours of PID stress, these samples are at 97% and 100% of the initial efficiency respectively. During the stress duration, only small changes to the median values of the other J-V parameters could be identified for these samples.

The other group consists of the high Na containing substrates; Na only and High Na (>10 mol% Na) and SLG (~14 mol% Na). Solar cells deposited on these substrates were severely degraded after 50 hours of PID treatment and the median efficiencies were close to 0%. Degradation could be observed in all J-V parameters and in Figure 10b), the V_{oc} is plotted. Comparing Figure 10a) to Figure 10b), we observe a strong correlation between V_{oc} and efficiency degradation and the evolutions of these two parameters are very similar for all samples. Also the FF follows the same typical behavior as the efficiency and V_{oc}, but with a lower threshold saturation value at 40%.

A closer look at Figure 10 reveals a differentiation amongst the degraded samples, the High Na sample is more heavily degraded than the Na only and SLG. The high Na sample approaches zero percent efficiency already after 24 hours and further PID stress continues to decrease both V_{oc} and J_{sc}. With the scale of Figure 10, one can also see a small difference in the efficiency after 50 hours of stress, where the high Na sample is slightly more degraded than the Na only and SLG. At this point it is important to point out that all the data points in Figure 10 represent the median value. There was a spread in I-V measurement from cell to cell on the degrading sample at any given measurement occasion and investigating the J-V curves clarifies these small differences.

In Figure 11, a selection of J-V curves was chosen to illustrate the differences between the degraded samples, and the spread for the cells on each sample. For cells that were subject to 50 hours of PID, J-V curves are plotted in red. The J-V curve of one representative un-degraded cell per sample, close to median performance, is plotted in green for comparison.

The most severely degraded sample, the High Na, is plotted in Figure 11a). This sample had the smallest cell spread and the J-V curves of the degraded cells pass very close to Origo. Therefore, V_{oc} and J_{sc} values are close to zero, which also can be deducted from the median values in Figure 10b) and d) respectively. The interpretation of FF for these curves is dubious, since these devices basically lack any part of the J-V curve in the fourth quadrant. Un-degraded devices on this substrate exhibit the characteristic “roll-over” effect, seen at high positive voltages. This blocking of current is often seen for Na-poor devices [40]. In this case, this roll-over effect can be attributed to properties of the High Na substrate itself, since the CIGS process was not optimized for any of the substrates. We observed the roll-over effect for the High Na substrate in this particular CIGS process throughout our experience with this substrate, whether a NaF precursor layer was used or not.

Un-degraded devices of the Na Only and SLG samples are more well-behaved as seen in Figure 11b) and c) respectively. For these samples, the spread in the degraded state is larger than the High Na sample. For example, V_{oc} is in the range of 50 – 150 mV for both samples, and the SLG exhibits lower J_{sc} values (10 – 25 mA.cm^{-2}) than the Na Only (20 – 30 mA.cm^{-2}). Typically we experienced this type of spread in other PID experiments as well. The solar cells on a particular sample reacted in various degrees to the treatment and normally there was no spatial trend, e.g. edge cells more affected, but rather randomized in location on the sample.

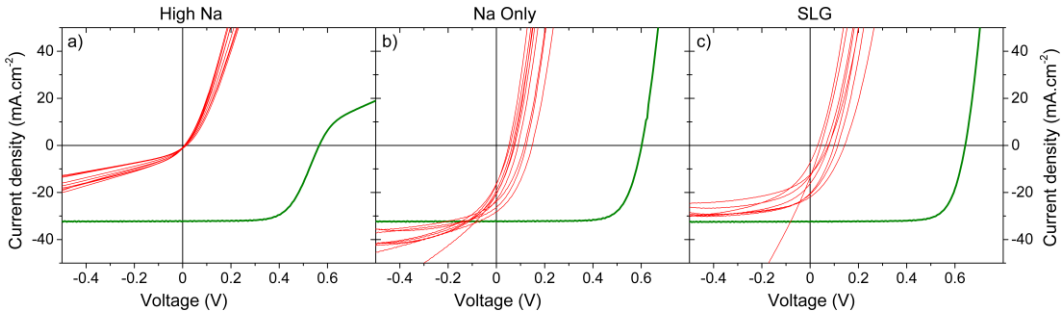

Figure 11. J-V curve of one typical un-degraded cell (green) and J-V curves of degraded cells (red) for a) High Na, b) Na Only, and c) SLG substrates respectively.

2.3.2 Material characterization

Since we found this interesting correlation between substrate composition and solar cell degradation, we decided to investigate the elemental depth profiles before and after 50 hours of PID with GD-OES measurements. The same two groups identified in Figure 10a), PID prone and PID resilient substrates are also distinguishable in Figure 12 where the Na depth profiles are shown.

Solar cells that degraded after 50 hours of PID show significantly higher Na levels throughout the layer stack, as compared to un-degraded devices. At this point there was no quantification routine available to correlate the intensity of the GD-OES with the Na atomic concentration. However, qualitatively, it is clear that samples within the degraded group exhibit higher Na concentration in the CdS buffer layer and also in the CIGS layer.

At this point it is important to remember that the external voltage is applied between the rear side of the substrate and the Mo layer in the solar cell stack (see Figure 9). The electrical field is only present in the substrate, as the Mo is conductive and efficiently screens the electrical field. We suggest that mobile ions in the glass, if existing, can drift by the electrical field in the glass towards the Mo layer. An accumulation of Na in the Mo layer will then create a driving force for Na to diffuse into the other layers and that is a likely reason for the increased Na levels seen in the layers outside the applied electrical field. Also note that also for the samples with Na-free or very low Na containing substrates, we added a NaF precursor layer. Thus all cells contain Na in sufficient or close to sufficient amounts to produce good solar cells.

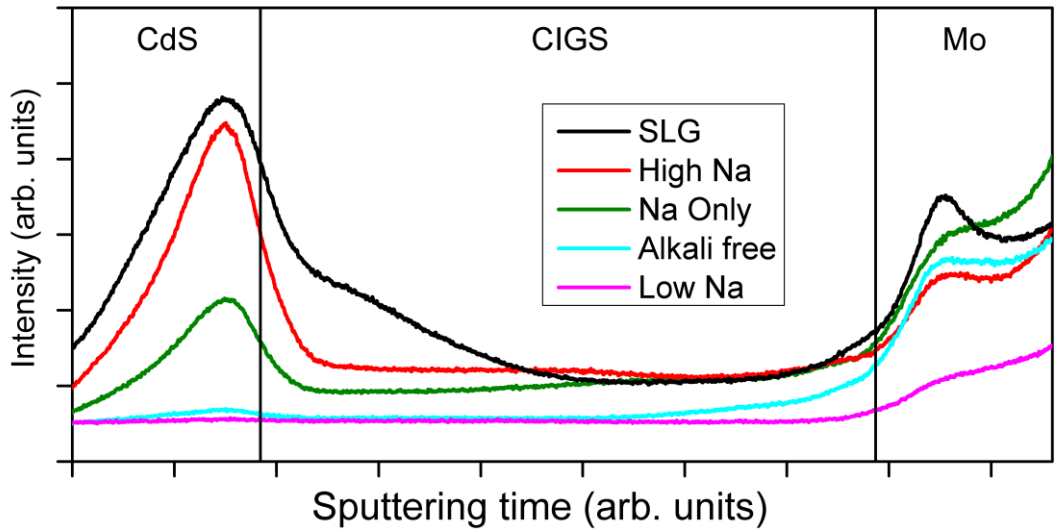

Figure 12. Na depth profiles, obtained with GD-OES, for all samples after 50 hours of PID. Vertical lines were added to the figure to indicate the position of the CdS/CIGS and CIGS/Mo interfaces. There lines are plotted at half the intensity of Cd and Mo respectively.

Since the first reports on Na in CIGS in 1993, another alkali metal, K, was rather overlooked due to the belief of its lower importance to the electrical properties of CIGS. However, in recent studies, the effect of K on solar cell performance was shown to be beneficial [41]–[44] when used in a KF post-CIGS-deposition-treatment. Three of the substrates in this work: SLG, High Na, and Low Na contain intentional K in the form of K_2O in the glass composition. In contrast to the Na result, no trend could be correlated between K and the electrical results.

The ratio of K intensity after and before PID, as measured with GD-OES, is plotted as function of absorber depth in Figure 13. In Figure 13a), the ratio, calculated from raw data, is plotted in light grey for the SLG sample. In green, the data has been modified with a moving average to smooth out the curve to clarify the results. This has been applied to the data for all substrates in this figure. A ratio below unity, at any depth, implies lower K concentration after PID, compared to the as-grown CIGS. This is the case for the Low Na substrate, which also has the highest K concentration in the glass composition. All the other substrates show only small changes to the K profiles, seen in Figure 13 as the ratio being close to one throughout the CIGS layer.

The K result from the Low Na substrate is surprising and deserves further discussion. For this sample, K is removed from CIGS during the PID treatment. This is in direct contrast to the observation for Na, where concentration on the same level or higher is observed in the CIGS after PID for any of the substrates. So, despite the fact that Na and K possess the same charge when ionized, their movement during PID differs. The K data for the full layer stack (not shown) indicate that K migrates towards and into the Mo back contact. However, the driving force cannot be identified. Since there are negligible changes to the Na profiles before or after PID for the Low Na sample, no ion-exchange mechanism can be used to explain the movement of K. Neither can the applied external electric field, as it would impose force in the same direction for K and Na ions due to their equal charge.

Amongst the substrates, the Low Na is the only one that exhibits changes to the K profiles during PID. On the other hand, the electrical parameters of solar cells on the Low Na sample only show minor changes as seen in Figure 10. Amongst the substrates without changes in K profiles, there are degrading samples (SLG, High Na, and Na only) as well as unaffected samples (Alkali free). From these ambiguities, we cannot identify any clear effect of K in PID on the electrical performance of the solar cells.

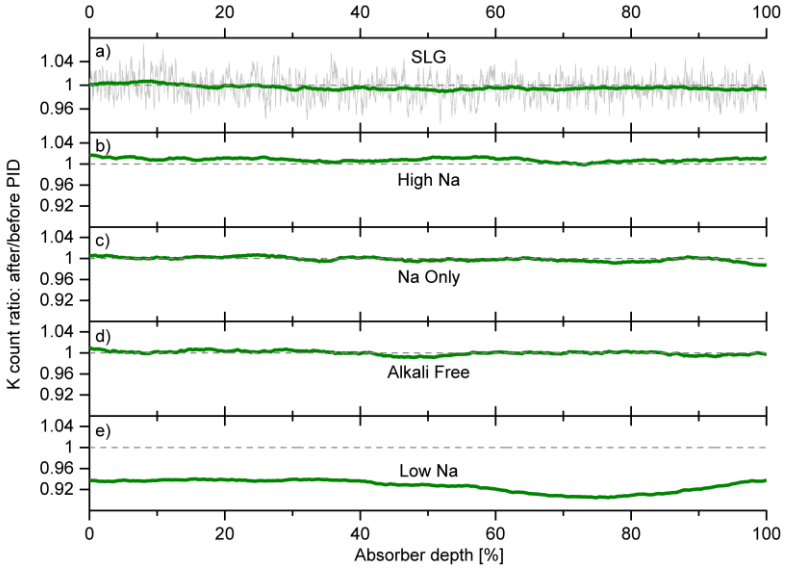

Figure 13. K count ratios: after/before PID, for a) SLG, b) High Na, c) Na Only, d) Alkali Free, and e) Low Na respectively.

From the Na profile results, it is clear that the substrate properties impact the devices´ response to PID stress. From Figure 10a) and Figure 12, we can distinguish two groups of samples: (i) one where the solar cells degrade electrically and significantly higher Na levels are found and (ii) one group where the devices are virtually resilient to PID and with only minor changes in the Na profiles. Since there is no other possible Na source for the additional Na concentration during PID than the substrate itself, it was important to get insight in the glasses' ability to release Na during PID. The potential Na flux is governed by the mobility of Na in the glass as well as the Na concentration. Hence, the potential Na flux should correlate with the resistivity of the glass and the resistivity values at T=300K are shown in Table IV. Measurements at lower temperatures are shown in Paper I. The three substrates with the lowest resistivity values were indeed the ones that suffered from degraded devices after PID; Na only, High Na and SLG. These were also the samples with elevated Na levels in the device structure after PID. On the other hand, the PID resilient devices were grown on either the Low Na substrate (with resistivity in the order of 10^{17} Ω*cm) or the Na free substrate. For the latter sample, no resistivity measurements were carried out, but since it is made from an alkali-free composition, it basically lacks conductive ions and the resistivity should because of that be even higher than the one of Low Na.

Table IV. Resistivity of the substrates obtained at T = 300K. *Extrapolated from measurements

Glass type	Resistivity (Ω·cm)
Na only	10^{10}
High Na	10^{12}
SLG	10^{13}
Low Na	10^{17*}
Na free	N/A

2.4 Conclusions

The substrate used for CIGS devices plays a critical role in how the solar cells respond to PID stress. CIGS solar cells grown on substrates with a low resistivity and high Na concentrations (>10 mol%) degrade to close to 0% efficiency after 50 hours of PID stress. Within this group of substrates there are differences in J-V response in the degraded state. The substrate with lowest resistivity, Na Only, exhibited almost fully shunted devices with only little diode behavior. For the other two substrates, High Na and SLG, diode behavior is identified and some part of the J-V curve is in the power-conversion fourth quadrant. Nevertheless, in practice these devices are useless as solar-to-electricity converters.

The observed degradation was linked to increased Na concentration in the CIGS and CdS buffer layers. Mobile Na ions in the substrate are suggested to readily migrate due to the applied bias. A model is proposed where Na ions drift in the electrical field to accumulate in the Mo back contact of the CIGS solar cell structure. This accumulation implies a non-equilibrium state and creates a driving force for Na to diffuse into the layer stack.

In contrast to Na, we did not find any correlation between K migration and solar cell degradation. Only one substrate exhibited significant changes in K distribution after PID. It was the substrate with the highest K_2O concentration in the glass composition. In further contrast to Na, K concentration was lower in the solar cell layers after PID, despite the same positive ionic charge of the two elements.

One method to mitigate PID of CIGS solar cells is to use substrates that do not release Na during the stress. Examples of such substrates are glasses with a Na free composition or glasses with high resistivity.

3. Recovery

3.1 Introduction

Initial measurements showed that the PID effect on the CIGS devices was at least to some degree reversible. The SLG sample used in the above experiment had a median efficiency before PID of 15.8% and after 50 hours of PID stress, the efficiency was close to zero. Two months later, after storing the samples in darkness in ambient office conditions, the median efficiency was 11.6%. This was a recovery to approximately 75% of the initial value. Another SLG sample was treated a similar way; 50 hours of PID stressing followed by 6 months of office storage, and this sample showed a recovery of approximately 92% as mentioned in Paper I.

Several other reports, on silicon PV technology, also showed that the PID effects in those cases were reversible [45]–[47]. Since we (as shown in Paper I) found the degradation to be linked to Na migration from the substrate and Na accumulation occurred in the buffer layer region of the stack, we wanted to understand if this was related to the recovery as well.

After the initial measurements mentioned above, we had no explanation or understanding of why the efficiency increased again once the PID stress condition was removed. However, our reasoning was that what caused the degradation in the first place was a reversible process and with time of relaxation, the affected materials would migrate in the direction towards its original properties.

3.2 Recovery methods

To try to understand the recovery process, we set up an experiment where we defined three different recovery methods as listed below.

i. *Un-accelerated recovery*. We named the process where we observed the recovery in the first place un-accelerated recovery, i.e. the fact that CIGS samples recover efficiency by passively storing them in darkness at office temperature (22°C) and without exposing the samples to any other treatment.

ii. *Accelerated recovery*. In contrast to the un-accelerated recovery, this is a method that involves active treatment of the sample. After degradation, with the rear side of the glass at a *positive* potential compared to the Mo back contact, the polarity of the applied bias is, in this recovery method, reversed. This implies that the rear side of the glass is at a *negative* potential compared to the Mo and the electrical field in the glass is reversed compared to the PID treatment. Further, this method includes that the samples were placed in the furnace with a temperature of 85°C.

iii. *Etch recovery*. The idea behind this recovery method stems from the fact that in the degraded state, Na was strongly accumulated in the CdS buffer layer. Etch recovery consists of removing the front contact and buffer layers with a chemical etch; immersing the sample in a hydrochloric acid (HCl) solution for one minute and then rinsing it thoroughly with de-ionized water. The HCl etch removes both the TCO and buffer layers so the sample, after the etch treatment, consists only of the Mo back contact and CIGS absorber on top of the substrate. Subsequently, the removed

layers were replaced with new layers, following the baseline procedure. Solar cells were finalized with current collecting grid and cell area definition.

3.3 Experimental details

To investigate the recovery methods listed above, new samples were processed. In this experiment we used 1 mm SLG substrates for all samples and the solar cell layers were deposited in the same way as in Paper I, i.e. following the baseline procedures. Also in this experiment with the exception of the CIGS layer which was deposited in our batch tool. However, for the etch recovery, the sample preparation was stopped after the TCO deposition for the reasons listed below. One sample, containing 12 individual solar cells, was used for each of the other recovery methods. The samples were equipped with the same type of contacts for the external voltage as developed in Paper I, pictured in Figure 9.

Implementation of the Etch recovery method required the samples to have no current collecting Ni/Al/Ni grid on top of the TCO and be without any cell area definition. Otherwise, the grid would disturb the etching process, and if there were already individual cells defined on the sample, it would be practically difficult (note: not impossible) to deposit the grid on the exact same location as before the etch recovery. Instead, the Etch recovery sample to be stressed with PID was processed up to the TCO layer. This implied that we were not able to obtain any I-V measurements before or directly after the 50 hours of degradation. Instead, for the two initial data points, a reference sample was used. The reference sample was processed in as similar conditions as possible as the sample for the Etch recovery. For these two samples, the Mo layer was deposited onto the same 10 x 10 x 0.1 cm^3 glass substrate and each sample was cut out from this Mo coated SLG pane. For the CIGS and CdS layers as well as the TCO layer, the samples were included in the same deposition batches to minimize the sample-to-sample variation between the Etch recovery sample and its reference.

After 50 hours of PID stress and I-V measurements, each sample was subject to its respective recovery treatment; the sample for un-accelerated recovery was covered to darkness and placed in office storage, the sample for accelerated recovery was placed in the furnace and the polarity of the external bias was reversed and the etch recovery sample was taken directly from the stress to the process laboratory for implementing the treatment. Three hours later, the TCO and CdS buffer layers had been removed and replaced with new layers, the Ni/Al/Ni grid had been deposited and the individual 0.5 cm^2 solar cells had been defined. Following the I-V measurement of this sample, it was further treated with accelerated recovery. An overview of the sample treatments is presented in Table V.

Table V. Treatments and intervals used in the recovery study.

Sample name	Treatment 0-50h	Treatment 50h and onwards
Un-accelerated	PID Stress	Darkness and room temperature storage
Accelerated	PID Stress	Reversed polarity of electric field in the substrate
Etch	PID Stress	Etch recovery, followed by accelerated recovery

3.4 Results

3.4.1 Electrical characterization

The first two data points (at 0 and 50 hours respectively) of the green-colored data set in Figure 14, shows the evolution of the reference of the Etch recovery sample. After three hours, the required time to execute the etch recovery, the dashed green line visualizes the efficiency increase up to approximately 80% of the initial value.

The HCl solution removes the CdS and TCO layers within a matter of a few seconds and the CIGS surface is then exposed to the etch for the remainder of the minute. After re-depositing the layers, the degraded solar cell stack is in a state where the CdS and TCO layers have been removed, the CIGS surface has been subject to a HCl etch and the stack has been completed with new layers on top of the CIGS. The results show that this restores approximately 80% of the efficiency. Further recovery of this sample occurred upon applying the accelerated method and the efficiency continued to slowly increase. At the last measurement point in this plot, the etch recovery sample had recovered approximately 90% in total, which is similar to the sample which had undergone the accelerated recovery.

One interpretation of these facts is that the PID can be attributed to at least two mechanisms. One mechanism that is connected to an aggregated degradation of the TCO, CdS buffer layer and CIGS surface, being recovered by the etch recovery. Without further analysis, the root cause of this part of the degradation cannot be pinpointed. However, we can speculate that high Na concentrations in the CdS and CdS/CIGS interface degrade the properties of the pn-junction. The other mechanism can be attributed to degradation of the CIGS layer itself, which can be recovered by the accelerated recovery method.

The accelerated method also recovers completely degraded samples, without any prior etch treatment as seen by the black-colored data set in Figure 14. This data set represents the sample that, directly after 50 hours of PID and subsequent I-V measurements, was placed in the furnace with reversed substrate bias. Initially, the recovery is slower than the etch recovery, but within a timeframe of 200 hours of recovery, these two samples both have recovered approximately 90% of the initial efficiency.

The notation *Accelerated recovery* is motivated from the comparison to the un-accelerated, passively recovered sample, represented by the red-colored data set in Figure 14. Despite no active treatment to this sample, the potential induced degradation in this sample is slowly recovering. The observant reader realizes that

if the seemingly linear recovery curve would continue, the recovery to 75% would take much less time than the two months stated in the introduction of this chapter. This reflects the sample-to-sample variation that we observed in several of our PID experiments.

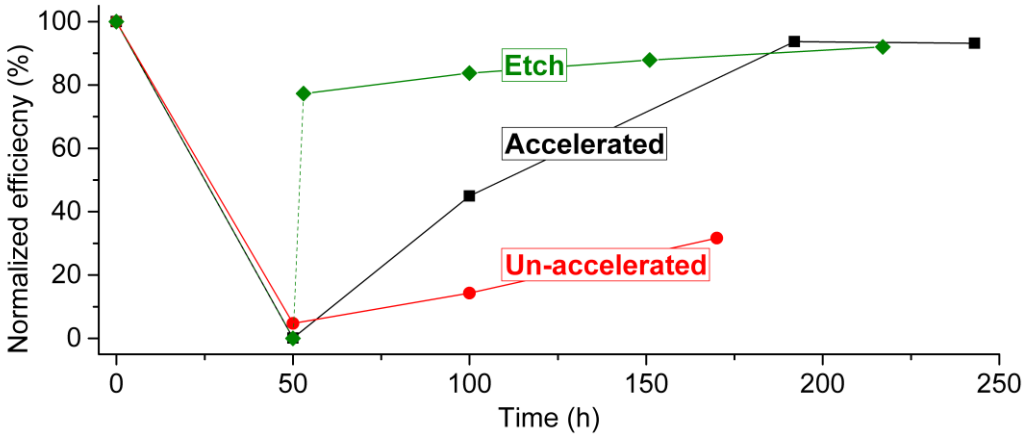

Figure 14. Efficiency evolution for the samples with various recovery schemes.

In Figure 15, the evolution of the etch recovery samples is shown in more detail. Three solar cells were chosen at each measurement point (0, 50, 53 and 218 hours respectively) to illustrate the spread. J-V curves in the initial and degraded state are from the Etch recovery reference sample. Indeed, this sample has degraded to the point of zero percent efficiency after 50 hours of PID, indicated by the red curves passing through Origo. The etch recovery process restores, as mentioned, approximately 80% of the initial efficiency, manifested by the cyan J-V-curves. The major part of J_{sc} is recovered at this point, 95%, but V_{oc} is only recovered by 85%. Further recovery, executed with the accelerated method, increased both V_{oc} and J_{sc} values, the latter to even higher values than initially.

The spread of the J-V response is larger in both the degraded and recovered states, compared to the initial state. Samples from the baseline process (e.g. the etch recovery reference sample in the initial state) normally have a minor [Ga]/([Ga]+[In]) gradient across the sample, yielding a typical V_{oc} spread of 15mV and a J_{sc} spread of 0.5mA-cm^{-2}. However, our experience with PID and recovery cycles is that the spread is significantly increased, which is exemplified in Figure 15. For example, the spread in series resistance in the two recovered states is clearly larger than initially, manifested by the curve spread at high positive voltages. Recalling that the front contact is renewed and should in principle have the same properties as in the initial baseline case, we have no reason to blame the increased spread in R_s to the front contact. Instead, one possible explanation for the increased spread in series resistance could be spatial variations of Na distributions in the Mo back contact, since Na has been observed to reduce the conductivity of Mo layer. We presented a discussion about the spatial variation in Paper II but without further analysis, since the explanation for the spread cannot be pinpointed.

At this point the observant reader realizes another discrepancy, namely the sample-to-sample variation. Comparing the degraded state in Figure 15 to Figure 11c) in section 2.3.1, there is a clear difference. Despite that in both cases, *a)* SLG

is used as a substrate, *b)* device fabrication is according to the baseline process, and *c)* the PID stress conditions are intentionally as similar as possible, the results differ. In Figure 15 the curves pass through Origo, while in Figure 11c), the curves have at least some part in the fourth quadrant. From other experiments we observed an un-quantified but clear correlation between CIGS thickness and PID degradation rate which is a possible explanation for the sample-to-sample variation in this case.

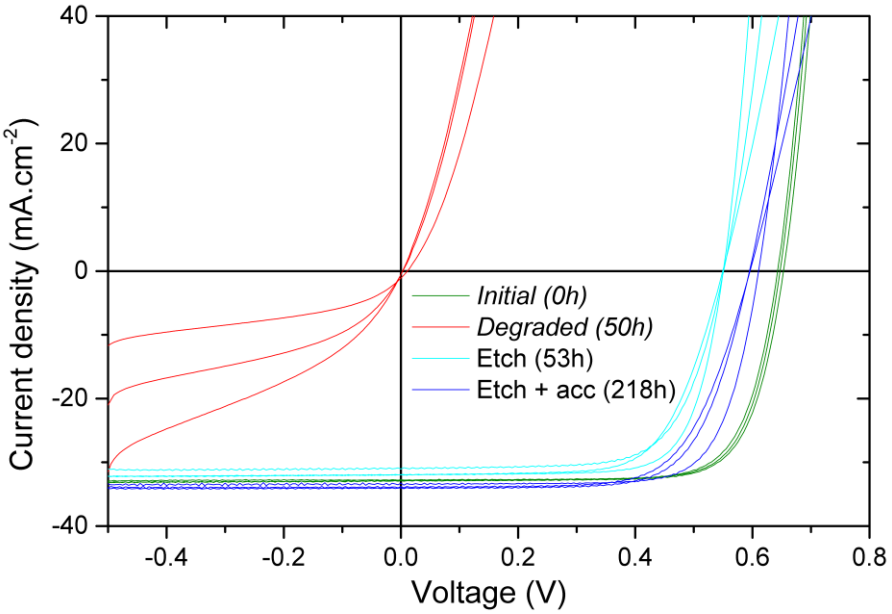

Figure 15. A selection of J-V curves from the Etch recovery experiment in the initial, degraded, etch recovered, and etch + accelerated recovered state respectively.

3.4.2 The differences before and after recovery

The sample presented for accelerated recovery represents the typical behavior for our baseline solar cells, where a recovery to slightly below the initial value can be obtained. Longer time with accelerated recovery normally does not change the parameters significantly and even if the samples recover to more than 90 % of their initial efficiency values they do not recover fully. We focus this section on an investigation of the differences that constitute this non-reversible part of the degradation, i.e. an analysis of the differences between the sample in the initial and recovered states.

In Figure 16, a selection of seven J-V curves is shown for the initial state and the state after PID and accelerated recovery. The efficiency loss is attributed to all J-V parameters, which are listed in Table VI. A zoom-in of the higher positive voltages, seen in Figure 16b), reveals an increased spread in the slope compared to the initial state, similar to what was observed in the etch recovery experiment (Figure 15). The J-V curves of these cells were fitted to the one-diode model, using the least-square-fit method described by Hegedus and Shafarman in [48]. Average values of the one-diode model parameters are can be found in Table VI and the distribution is presented in Figure 17.

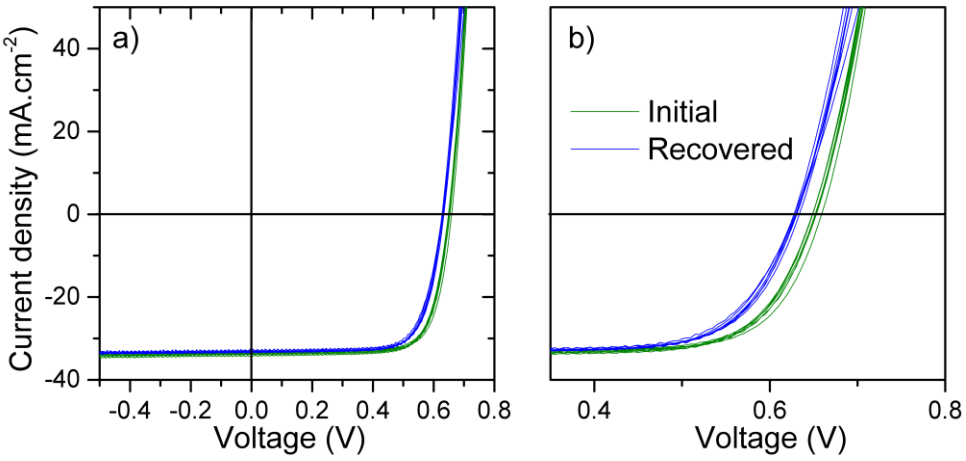

Figure 16. a) J-V curves of the seven cells used in the one-diode fitting work and b) a zoom-in of the J-V "knee", before and after PID plus recovery.

Table VI. Average J-V and one-diode model parameters of the selected devices. *Median value.

Parameter	**Initial value**	**After recovery**
V_{oc} [mV]	652	630
J_{sc} [mA.cm^{-2}]	33.7	33.1
FF [%]	75.4	74.3
Eta [%]	16.5	15.5
$^{*}J_0$ [mA.cm^{-2}]	$1.6 \cdot 10^{-6}$	$5.9 \cdot 10^{-6}$
A [1]	1.51	1.57
R_s [Ω]	0.68	0.91
R_{sh} [Ω]	2600	3400

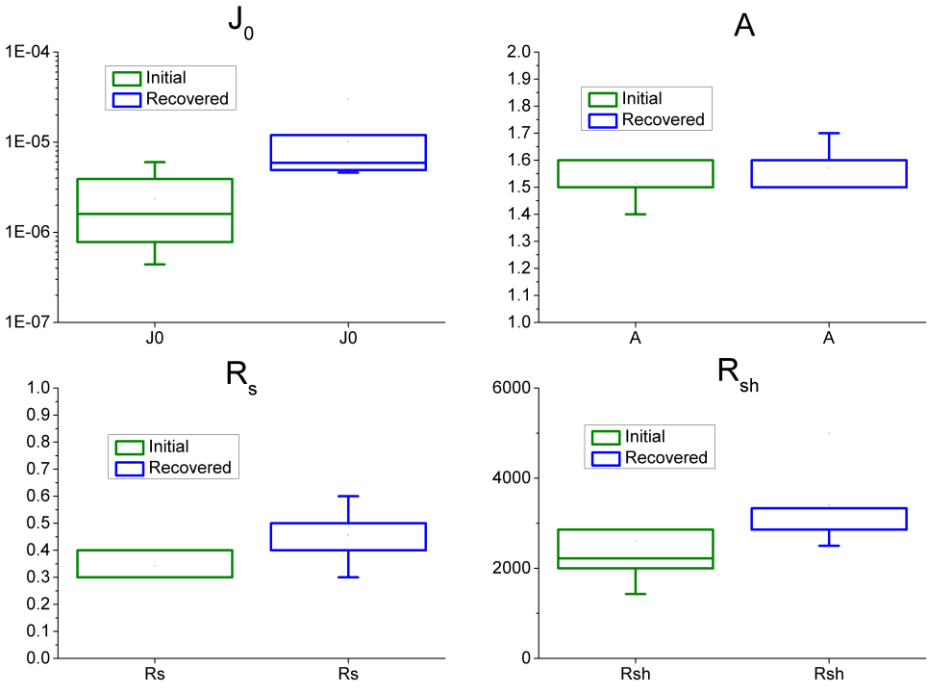

Figure 17. Parameters extracted from fitting the light J-V data of seven cells to the one diode model.

The non-recoverable part of V_{oc} can be attributed to increased recombination in the recovered state, seen by an increase in saturation current. However, there is no significant difference in the ideality factors before and after degradation plus recovery. Therefore we cannot distinguish any differences in terms of the relation between depletion region and bulk dominated recombination mechanisms. In addition to the loss in FF implied by the lower V_{oc}, series resistance is increased to further reduce FF. The shunt resistance values are higher in the recovered state but without a sensitivity analysis, the impact of each parameter on the model cannot be fully determined.

The Na depth profiles, measured with GD-OES reveal other clear differences as seen in Figure 18. The PID treatment increases the Na concentration in the buffer layer and top part of the CIGS, similar to what we reported in the substrate degradation experiment in chapter 2. Applying the accelerated recovery led to reduced Na concentration, but not down to the initial level. Instead, the concentration is elevated and the signal in the buffer layer and CIGS is closer to the degraded state. Despite this, solar cells with this Na distribution have recovered over 90% of the initial efficiency. The discrepancy between Na signal and cell efficiency makes us unable to un-ambiguously link the Na level to cell efficiency in PID and recovery. Hence, further studies are needed to pinpoint the effect of Na on the microstructure level in CIGS during PID and recovery.

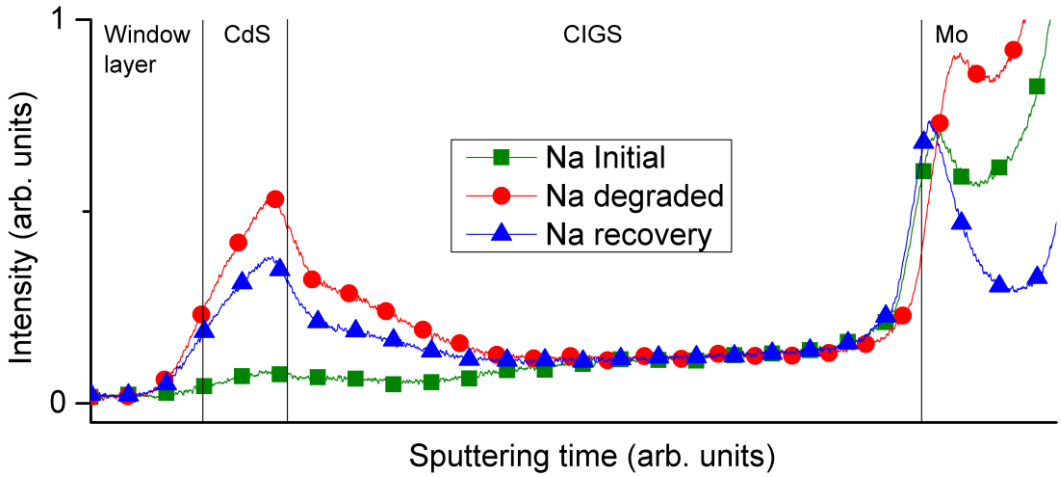

Figure 18. Na depth profiles of the sample used in the accelerated recovery. The Na profiles are shown for the initial state, after 50 hours of PID as well as after recovery to almost the initial efficiency.

3.5 Comparing CdS and Zn(O,S) buffer layers in recovery

Up to this point, the thesis has been focused on PID of our standard, baseline solar cell configuration; substrate/Mo/CIGS/CdS/i-ZnO/ZnO:Al/grid. In parallel to the experiment with the three recovery methods, we investigated PID for a slightly modified solar cell configuration; the CdS buffer layer was replaced with Zn(O,S). Our research group holds several years of research on alternative buffer layers [49]–[53]. The idea behind using these materials as buffer layers is to move away from the use of Cd containing compounds since Cd is a toxic heavy metal. In our experience, using alternative buffer layers instead of CdS yields solar cells with higher J_{sc}. This is because of a higher band gap of these materials, which reduces parasitic absorption in the buffer layer. Further, V_{oc} and FF are reduced,

explained by a less favorable CIGS/buffer band alignment [54]. This finding highlights the importance of this interface on the device, also outside the PID topic.

Because of the previous results, where the buffer layer region seemed to have a central role in PID, we were supposing to gain more knowledge when replacing the CdS buffer layer with another material and subject the devices to PID. The results were indeed fruitful. Samples with Zn(O,S) buffer layer degraded in a similar way to CdS samples, i.e. completely degraded after 50 hours of PID. However, despite the fact that the accelerated recovery method was used also on the Zn(O,S) sample, no recovery of efficiency could be observed within 200 hours of recovery time. This is clearly in contrast to the CdS sample. Still, the samples showed clear differences that will be outlined below.

3.5.1 The CIGS/buffer layer interface

Besides the obvious difference in material properties and elements, the deposition processes of the two buffer layers are also different. The CdS layers are deposited in a chemical bath. Since the CBD solution is alkaline due to the inclusion of ammonia, the CIGS surface is etched prior to CdS nucleation and film growth, which removes some Na-compounds and oxides. In contrast, we deposit Zn(O,S) with atomic layer deposition (ALD), a technique which does not comprise any treatment of the CIGS surface.
During previous, non PID-related experiments, we found that the alternative buffer layers deposited onto CIGS absorbers from our batch tool, yielded solar cells with greatly lower efficiencies compared to their CdS counterparts, typically at half the efficiency of the CdS reference cells. This difference is much smaller, a few tenths of percent, with CIGS absorbers from our inline tool [9], despite the fact that for both CIGS evaporators, vacuum is breached between absorber and buffer layer depositions. At that time we decided to briefly investigate different etch processes of the CIGS from the batch tool in combination with alternative buffer layers. We used 1 minute of etch time and four different chemical solutions: water, ammonia, hydrochloric acid and potassium cyanide (KCN). The latter was shown to produce cells with the highest efficiency and for this PID work, we employed this KCN etch treatment of the CIGS surface prior to ALD of Zn(O,S).

We did not study the effects of the KCN etch in detail, but others have found that impurities are removed from the surface as well as CuSe secondary compounds [55]. Since we deposit our CIGS layers with a composition below stoichiometry, there should be no CuSe to remove with the KCN etch. In our case it is likely to clean the surface from surface oxides and Na compounds, both at the CIGS surface and in the grain boundaries in the near surface region. This creates a more favorable interface with the Zn(O,S) buffer layer. With this treatment, we were able to produce Zn(O,S) cells with similar results as from our inline evaporator, i.e. slightly lower V_{oc} and FF and higher J_{sc} compared to CdS references

3.5.2 Results

To illustrate the common behavior during degradation, the cell closest to the median efficiency from the CdS and Zn(O,S) samples were selected and plotted in Figure 19 a) and b). In the initial state, i.e. before degradation, two well-behaved

J-V curves are observed. Lower V_{oc} and FF, as well as higher J_{sc} for the Zn(O,S) sample can easily be seen when comparing the two J-V curves from the initial state.

After 50 hours of PID, both cells exhibit virtually zero percent efficiency. The corresponding J-V curves pass through or very close to Origo. However, the shapes of the curves are different. For Zn(O,S) it is a straight line, without any diode behavior. This is exactly corresponding to J-V measurement of an ohmic device (resistor). The CdS cell on the other hand still exhibits diode behavior to some degree, even though the efficiency in practice is zero.

Also in recovery, the cells respond differently to the treatment. The Zn(O,S) cell regained some diode properties after 50 hours of accelerated recovery but with more time, only small changes can be identified. After 200 hours of total recovery time, the Zn(O,S) cell is still at zero percent efficiency while its CdS counterpart has regained more than 90% of its initial efficiency.

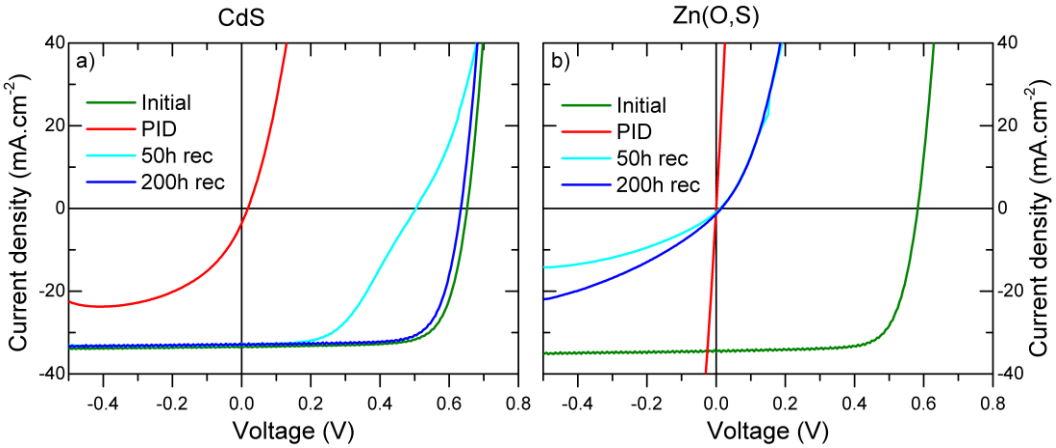

Figure 19. J-V curves throughout the PID and accelerated recovery cycle of one cell on the a) CdS and b) Zn(O,S) samples respectively.

C-V measurements provided further insight on the degradation and recovery processes and matched the general J-V trend to some extent. In Table VII the depleted layer width at 0V bias is depicted. For both samples, the depleted layer width was increased after PID, corresponding to lower effective p-doping of the CIGS layer. For the CdS sample, recovery was possible also in this respect but for Zn(O,S), recovery of the depleted layer width was not seen within 200 hours. In Paper II, we present a more thorough discussion about CV and GD-OES measurements of these samples.

Table VII. Depleted layer width at 0V bias, calculated from CV-measurements.

State	**Depleted layer width [µm]**	
	CdS	Zn(O,S)
Initial	0.2	0.2
Degraded	1.8	1.0
50h recovered	1.9	1.0
200h recovered	0.3	1.2

3.6 Conclusions

Part of the potential-induced degradation was shown to be non-permanent for CIGS solar cells. Recovery of the electrical performance was possible. The recovery characteristics of three different methods were investigated: un-accelerated, accelerated and etch recovery. The un-accelerated method showed that samples could regain efficiency by storing the samples in ambient office conditions, without any active treatment. The recovery rate varies from sample to sample and in one particular case, after being completely degraded by PID, a recovery of 92% was possible within 6 months of storage.

It is possible to increase the recovery rate by using the accelerated method. Typically, accelerated recovery saturates slightly above 90% of the initial efficiency after 150 hours. The permanent degradation could be attributed to reduction of all J-V parameters (V_{oc}, Jsc, FF) but mostly dominated by V_{oc} loss. The one-diode model showed an increased dark saturation current density after recovery, but similar ideality factor. Based on this data, we attribute the V_{oc} loss to increased recombination, but without change in the distribution between bulk and interface recombination. Part of the FF loss could be attributed to increased series resistance of the devices.

With the accelerated recovery method, the elevated Na concentration from PID was reduced. Na concentrations in the buffer layer and top third of the CIGS were lowered, but not to the initial levels. This discrepancy between GD-OES Na signal and electrical performance of the devices make us unable to unambiguously link the level of degradation to the level of Na.

The importance of the buffer layer and the buffer layer/CIGS interface was highlighted. Degraded samples with CdS buffer layers regained 80% of the initial efficiency by the etch recovery. The features of the etch process is an acidic (HCl) surface treatment of the CIGS surface and renewed window layers. From the fact that further recovery to over 90% was possible with the accelerated method, we draw the conclusion that the degradation can be linked to at least two mechanisms. One part is degradation of the buffer layer and the interface, which we from this experiment cannot differentiate. This part of the degradation could be recovered with etch recovery. In addition, persistent degradation of the CIGS layer after the etch recovery could be partially recovered with the accelerated method.

The importance of the buffer layer in PID was further demonstrated when the CdS buffer layer was replaced with Zn(O,S). Unlike the CdS sample, a degraded Zn(O,S) sample exhibited completely resistor-like behavior. Recovery of this sample with the accelerated method could restore diode behavior to some extent, but the efficiency stayed at zero percent throughout the time-frame of the experiment. While the CdS sample could recover also in terms of reducing the depleted layer width, the capacitance response of the Zn(O,S) was barely changed after more time with recovery. The depleted layer width stayed, within this experiment, always at an elevated level as compared to in the as-grown state.

4. Suggestions for future work

With this work we have shown that CIGS solar cells are susceptible to PID and the root cause was found to be Na migration from the substrate into the devices. Hence, one way to mitigate this effect is to use substrates that do not release Na during the stress conditions. The degradation is to some degree reversible and three recovery methods were investigated. The buffer layer and the interface between the buffer layer and CIGS play a key role in the degradation and recovery characteristics. For example, substituting the standard CdS buffer layer with Zn(O,S) alters Na distribution during PID, changes capacitance response and inhibits recovery.

To further extend our understanding of the PID mechanism and Na migration, an experiment with the charge and discharge characteristics of a Mo/SLG/Mo parallel plate capacitor could be beneficial. Since we believe that Na is mobile in the form of ions, a current in the bias circuit could be used as an estimation of the Na flux from the glass to the negatively biased Mo. If Na ions migrate to the negatively biased Mo, counter-ions would migrate to the positively biased Mo layer to maintain charge balance. Would this ion be oxygen since the source of Na in SLG is NaO_2? Elemental depth analysis of the Mo layers in such a stack could help us to answer that question.

A technique to find the volumes in the stack with high Na concentration would be valuable. Is Na transported at the CIGS grain boundaries and is there an accumulation in those regions? And what is the detailed impact of Na in the CdS buffer layer and CIGS/CdS interface on the properties, except that it is detrimental? Hall measurements of CdS with Na implanted at the same level as after PID could give valuable information. Is the as grown n-CdS compensated by Na to p-type?

To understand the recovery process better, an etch-recovery experiment of a Zn(O,S) sample would give valuable input on differentiating the degradation mechanisms in the CIGS from the buffer layer. Further electrical characterization is clearly needed to pinpoint the mechanisms on the device level.

In the wider picture, other methods to mitigate PID could be addressed. For example module mounting structures, electrical insulation of the module rear side, Na barriers between the glass and Mo, and reverse bias (i.e. accelerated recovery) during the night for example.

5. Sammanfattning på svenska

Solcellsmarknaden domineras sedan länge av tekniker baserade på kristallint kisel, men det finns även tunnfilmstekniker på marknaden. Jämfört med kiselceller kan dessa solceller göras ca 100 gånger tunnare, eftersom de är mycket bättre på att absorbera solljus. Att använda mindre mängd material öppnar möjligheter för en billigare och mindre energikrävande tillverkningsprocess.

Oavsett val av solcellsteknik så är en av förutsättningarna för en god ekonomisk kalkyl för en solelinstallation att solcellsmodulerna har lång livslängd och inte förlorar verkningsgrad över tid. Det finns flertalet olika mekanismer som kan leda till degradation av solcellsmodulernas elektriska prestanda. Denna licentiatavhandling behandlas *spänningsinducerad degradation* (SID) för tunnfilmsmaterialet $CuIn_{1-x}Ga_xSe_2$ (CIGS). SID är en degradationsmekanism som i fält orsakas av en kombination av modulernas potential relativt nollpotentialen (skyddsjord) och omgivningsfaktorer såsom luftfuktighet och temperatur. Förhållandena för spänningsinducerad degradation reproduceras för små testceller genom att lägga på en elektrisk spänning mellan cellernas bakkontakt och baksidan av glassubstratet. Proverna placeras sedan i en ugn som är uppvärmd till 85°C.

Degradationen av solcellerna kan kopplas till en ökad natriumkoncentration i solcellsstrukturen efter behandlingen. Natriumjoner drivs ut ur glassubstratet av det elektriska fält som uppstår när spänningen läggs över glaset. Den enskilt viktigaste egenskapen hos substratet i detta fall är om det kan frigöra och avge natriumjoner eller inte. Ett mått på detta är glasets resistivitet. Solceller som är deponerade på glas med hög resistivitet eller natriumfria glas degraderar inte av SID.

Resultaten visar också att degradationen åtminstone delvis är reversibel. Det är möjligt för helt degraderade solceller att återfå elektrisk prestanda. I denna avhandling presenteras och undersöks tre olika metoder för detta. Den ena är passiv återhämtning i mörker och rumstemperatur. Den andra är en accelererad metod där riktningen på det elektriska fältet är omvänd jämfört med under degradationen. Mätningar visar att natriumkoncentrationen i detta fall är reducerad, jämfört med efter degradation. Den tredje metoden innebär att fönster- och buffertlagren etsas bort och ersätts med nya, opåverkade lager. Alla dessa metoder ledde till återhämtning av den elektriska prestandan, men återhämtningstakten varierade mellan metoderna. Från att ha varit helt degraderade var det möjligt att typiskt återhämta ca 90% av den initiala verkningsgraden.

Återhämtning med ets-metoden indikerade att buffertlagret och dess gränsyta mot CIGS har en central roll i SID. Denna roll bekräftades med ett experiment där två olika buffertlager testades, CdS och Zn(O,S). Resultaten ovan är för CIGS med CdS som buffertlager men när det byts mot Zn(O,S) kunde inte de degraderade solcellerna återhämtas med den accelererade metoden.

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7. List of papers

I. *Potential-Induced Degradation of $CuIn_{1-x}Ga_xSe_2$ Thin Film Solar Cells*

Viktor Fjällström, Pedro Salomé, Adam Hultqvist, Marika Edoff, Tobias Jarmar, Bruce G. Aitken, Kan Zhang, Kim Fuller, Carlo K. Williams

IEEE journal of Photovoltaics, volume 3, number 3, pp. 1090-1094 (July 2013)

Personal contributions to the article: Device fabrication, electrical and part of the material characterization, analysis and part of writing

II. *Recovery After Potential-Induced degradation of $CuIn_{1-x}Ga_xSe_2$ Solar Cells With CdS and Zn(O,S) Buffer Layers*

Viktor Fjällström, Piotr Szaniawski, Bart Vermang, Pedro Salomé, Fredrik Rostvall, Uwe Zimmermann, Marika Edoff

IEEE journal of Photovoltaics, vol. 5, no. 2, pp. 664-669 (March 2015)

Personal contributions to the article: Device fabrication, material and part of the electrical characterization, analysis and writing.

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