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Graphene Implementation Study in Semiconductor Processing

PATRIK AHLBERG

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Abstract

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Graphene, with its two-dimensional nature and unique properties, has for over a decade captured enormous interests in both industry and academia. This work tries to answer the question of what would happen to graphene when it is subjected to various processing conditions and how this would affect the graphene functionality. The focus is placed on its ability to withstand different thin-film deposition environments with regard to the implementation of graphene in two application areas: as a diffusion barrier and in electronic devices.

With single-layer graphene films grown in-house by means of chemical vapor deposition (CVD), four techniques among the well-established thin-film deposition methods are studied in detail: atomic layer deposition (ALD), evaporation, sputter-deposition and spray-deposition. And in this order, these methods span a large range of kinetic impact energies from low to high. Graphene is known to have a threshold displacement energy of 22 eV above which carbon atoms are ejected from the lattice. Thus, ALD and evaporation work with energies below this threshold, while sputtering and spraying may involve energies above. The quality of the graphene films undergone the various depositions is mainly evaluated using Raman spectroscopy.

Spray deposition of liquid alloy Ga-In-Sn is shown to require a stack of at least 4 layers of graphene in order to act as an effective barrier to the Ga diffusion after the harsh spray-processing. Sputter-deposition is found to benefit from low substrate temperature and high chamber pressure (thereby low kinetic impact energy) so as to avoid damaging the graphene. Reactive sputtering should be avoided. Evaporation is non-invasiveness with low kinetic impact energy and graphene can be subjected to repeated evaporation and removal steps without losing its integrity. With ALD, the effects on graphene are of different nature and they are investigated in the field-effect-transistor (FET) configuration. The ALD process for deposition of Al_2O_3 films is found to remove undesired dopants from the prior processing and the Al_2O_3 films are shown to protect the graphene channel from doping by oxygen. When the substrate is turned hydrophobic by chemical treatment prior to graphene transfer-deposition, a unipolar transistor behavior is obtained.

Patrik Ahlberg, Department of Engineering Sciences, Solid State Electronics, Box 534, Uppsala University, SE-75121 Uppsala, Sweden.

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List of Papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I Hinnemo M, Ahlberg P, Hägglund C, Wencai R, Hui-Ming C, Zhang S-L, Zhang Z (2015) Scalable Residue-Free Graphene for Surface Enhanced Raman Scattering. *Carbon* Vol. 98, p 567-571

II Ahlberg P, Hinnemo M, Song M, Gao X, Olsson J, Zhang S-L, Zhang Z (2015) A two-in-one process for reliable graphene transistors processed with photo-lithography. *Applied Physics Letters* Vol. 107 203104

III Ahlberg P, Hinnemo M, Zhang S-L, Olsson J (2016) Unipolar Behavior in Interface Controlled Graphene Field Effect Transistor *Manuscript*

IV Ahlberg P, Johansson F.O.L, Zhang Z, Jansson U, Zhang S-L, Lindblad A, Nyberg T (2016) Defect Formation in Graphene during Low-Energy Ion Bombardment *APL Materials* Vol. 4 046104

V Ahlberg P, Nyberg T, Jansson, U, Zhang S-L, Zhang Z (2016) Toward synthesis of oxide films on graphene with sputtering based processes *Journal of Vacuum Science and Technology B* Resubmission after minor revision

VI Ahlberg P, Jeong S.H, Jiao M, Zhigang W, Jansson U, Zhang S-L, Zhang Z (2014) Graphene as a Diffusion Barrier in Galinstan-Solid Metal Contacts. *IEEE Transactions on Electron Devices* Vol. 61, nr. 8, p 2996-3000

Contents

Abbreviations

SLG	Single layer graphene
DLG	Double layer graphene
MLG	Multi-layer graphene
IC	Integrated circuit
XRD	X-ray diffraction
Tg	Glass transition temperature
PMMA	Poly(methyl methacrylate)
SEM	Scanning electron microscope
G-FET	Graphene field effect transistor
V_{Dirac}	Dirac voltage
I_D	Drain current
V_{DS}	Source-drain voltage
V_{BG}	Back-gate voltage
V_{TG}	Top-gate voltage
g_m	Transconductance
g_D	Channel conductance
C_{ox}	Oxide capacitance
N	Carrier concentration
N_A	Acceptor doping concentration
N_D	Donor doping concentration
μ_{FE}	Field effect mobility
μ_{Eff}	Effective mobility
Qn	Charge density
q	Elementary charge
PDMS	Polydimethylsiloxane

1. Introduction

The basis of modern electronic industry is the implementation of integrated circuits (IC); the idea is that a number of electronic components interconnected on a common substrate can be parallel-manufactured. This allows for higher quality of the circuit than if the devices were manufactured individually and enables routine shrinking of the devices. The development route for the electronics community is governed by a principle called Moore's law, after Gordon Moore who stated in 1965:[1] the number of transistors per IC would double every two years, this implies that the price per transistor also should drop by half. This has today been given a broader interpretation but still, this philosophy of exponential progress is being followed. At the moment of writing the industry is at the 14 nm technology generation[2] while 7 nm has been reported produced in a laboratory.[3] To be able to keep up with this trend the industry has had to reinvent itself over and over again. This has meant that there has been an accumulation of techniques and experiences over the years, leading to everything from a great flora of thin film deposition methods to a deep understanding of device designs. It has for example led to the switch from planar structure to a tri-gate one in today's complementary metal–oxide–semiconductor (CMOS) structure, in order to keep improving the performance.[2]

However, Moore's law is now in danger of becoming obsolete. In 2015 Intel disclosed that they would not be able to deliver the 10 nm technology in time and has so far postponed the release.[4] The reason for this slowdown is that as the dimensions shrink, physical phenomena that were previously not an issue all of a sudden starts affecting the performance. One of these is the dielectric performance; if a barrier becomes thin enough the leakage current through the transistor gate will become non-negligible.[5]

Whether or not Moore's law is failing, many groups both in academia and industry have shifted their focus away from microprocessor and memory development, and into alternative areas where the experiences from production and design could prove useful. This concept has even been given the fitting name of "More-than-Moore".[6] A promising field is the development of flexible electronics which could find its place in everything from solar cells and touch screens to smart packaging and low cost diagnostic tools, Fig. 1.1 is an illustration of a flexible display. The basic idea is to make simple assembled devices on primarily polymer substrates at a low cost, due to the fact that it can be manufactured in a roll-to-roll type of production.[7, 8]

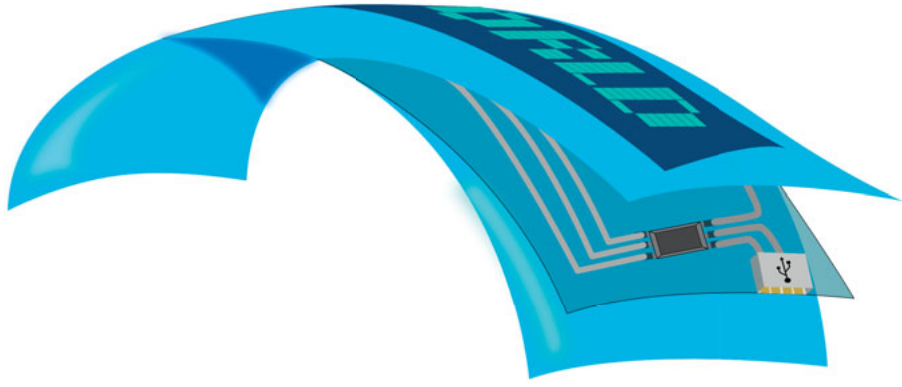

Figure 1.1 An illustration of a flexible screen with a combination of bendable circuitry and rigid components laminated together.

One particular aspect of flexible technology is organic based semiconductors which have already been utilized in non-flexible systems. The introduction of organic conductors and semiconductors in the 70's showed that C based materials were a viable base for making circuits.[9] There are however still some problems when it comes to the use of organic semiconductors, one of the major ones is the short shelf life of the chemicals.[10] Substantial amount of care has to be taken to ensure that the organic material is protected from O, molecular or otherwise. This is usually solved with thick glass sheets combined with epoxides to encapsulate the device. Special interest has also been given to transparent screens that are relevant for another emerging technology, namely augmented reality.[11] To be able to meet the challenges from these new fields of electronics, new materials as well as new production methods need to be introduced. With this progress, one of the factors will be the ability to tie new concepts into old knowledge thus lowering the barrier between industry and academia.

In 2004, two scientists named Konstantin Novoselov and Andre Geim introduced the world to the first method of making graphene, an atomically flat two dimensional (2D) crystal, and by doing this revolutionized how we look at our pencils.[12] By using what is called the "scotch tape" method with normal graphite, which can be found in normal pencils, they were able to create a single layer graphene (SLG) on top of an oxidized Si wafer. These first flakes ranged in the μm size and exhibited several noteworthy properties. The mobility was substantially higher than that of any other material and the material showed a "strong ambipolar electric field effect".[12] In 2009 came the breakthroughs that made it possible to produce high quality graphene in large scale.[13-15] Graphene was made by chemical vapor deposition (CVD) on a metal substrate, i.e. Cu and Ni, at 1000 ^{o}C with a mixture of Ar, H_2 and C containing gases see (chapter 2). The low solubility of C in Cu allowed the process to be self-controlled and resulted in a single layer of

coalesced graphene flakes. However with this easy technique of manufacturing large scale, good quality graphene came an additional problem; how to transfer the graphene from the initial Cu foil to a desired substrate? Fortunately, this problem was quickly solved and in one of the first CVD papers a successful graphene transfer from a metal film was published.[15] The graphene film is covered by a layer of support polymer, the growth metal is removed and the graphene is placed on the desired substrate, see chapter 3 for more details. With these two available techniques, graphene could not only be made available to a larger community of researchers but also allowed graphene to be tested for industrial implementations. To this date several publications have shown how graphene can be utilized in one way or another in wafer scale manufacturing.[16, 17]

In 2012 Novoselov et. al. published the first roadmap for graphene,[18] which has since been continuously updated. In the latest roadmap Ferrari et. al. stake out three objectives for the graphene community to conquer.[19] The first objective concerns material technologies with the aim to find new 2D materials and new means of production. The second objective is to implement graphene into devices as well as identifying new types of device that can benefit from graphene's special properties. The third objective is systems integration, where the aforementioned devices are implemented in end products. Objectives one and two have already made significant progress while the third objective has been estimated in the 2014 roadmap not to be met until latest in 7-10 years' time.

Graphene's extreme properties can be linked to its special structure. In a C based molecule, there is always one or more of three hybridizations possible, due to C's electron configuration, [He] $2s^2$ $2p^2$. However graphene is a crystal consisting of solely sp^2 hybridized C. In a larger network of sp^2 hybridized C the π-electron from each atom will become delocalized. These electrons will orient themselves together with the other delocalized electrons into two separate 2D electron clouds.[20] It is how these electrons in the 2D gas interact with the periodical potential of the honeycomb structure of nuclei that accounts for the high mobility.[21] Unfortunately, graphene has besides an extreme mobility, a complete lack of bandgap. In a metal the conduction band overlaps with the valence band, in an insulator they are significantly separated and in a semiconductor they are slightly separated, usually below 5 eV. In perfect graphene the bandgap is 0 eV,[22] which means that standard semiconductive behavior does not apply where graphene is the channel of a field effect device.[23] The lack of a proper bandgap and the symmetrical shape of the conduction and valence band (Fig. 1.2) lead to an ambipolar transfer characteristic where the electrons and holes can be conducted almost equally well. This in combination with the fact that graphene, when it is the channel in a field effect transistor, has shown to have no off-state i.e. a region of sufficiently low conductivity in the transfer characteristic, makes it a challenge to utilize.

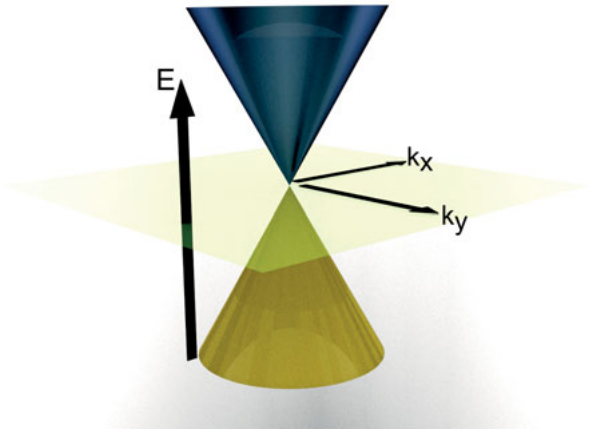

Figure 1.2 Graphene band diagram close to the Dirac point, yellow for the valence band and blue for the conduction band. Note the lack of gap between these two bands.

However, for a suspended sheet of graphene the theoretical mean free path is close to 1 μm, [24] meaning that if it were to be introduced into today's processors the electron transport would be nearly ballistic. At the same time when graphene is scaled down in channel width, edge effects set in. This means that the bandgap would be opened up but also lead to a reduction of the mobility.[25]

These aforementioned problems of introducing graphene into established devices do not mean that graphene cannot be used in future circuitry. Graphene has been incorporated into several novel devices that utilize its special traits. Two of these are the barristor [26] and hot electron transistor,[27] which reportedly have shown an on/off ratio over 10^5 and 10^4, respectively. Both of them belong to the group of vertical FET, where the gate, source, channel and drain are stacked on top of each other.

Many publications following the 2004 Nobel prize awarded article revealed other novel properties of graphene. Graphene is an excellent diffusion barrier, able to contain He[28] and even deuterium ions[29] with just a single layer. This ability has made several groups interested in using graphene as a compliment in displays and touch screens to prevent the oxidation of organic electronics and thus prolong its shelf life. The barrier effect combined with the fact that it also has a published stretch ability up to 20 %[30] while being 97.7 % transparent,[31] makes it interesting for the development of flexible electronics. It has also been shown that highly doped stacked four layer graphene can deliver a sheet resistance of 30 Ω/sq [32] on flexible substrates meaning graphene could play both the role of conductor as well as semiconductor in future devices. Graphene holds all these properties while its tensile

strength is so high that a square meter of perfect graphene could support a grown cat.[33]

Graphene has now by many accounts past the point of maximum hype.[19] This two dimensional wonder material will soon have to start deliver on its promises. There has been to this date over 25 000 patents filed regarding graphene. Will these come to fruition or are they just the product of misplaced optimism? We face the question if graphene can be processed and utilized in a way that is reasonable in the modern CMOS industry or is there even a place for it in the "More-than-Moore" development? Can it be incorporated and deliver the next generations' electronics and if so what will be its role and limitations? These are the big questions, too big for one thesis. This work is limited to the question of how different thin film materials, some common and some new, will interact with the graphene interface. How will thin film deposition of metals and oxides affect the very special abilities of graphene? What differences can be found among methods such as atomic layer deposition, evaporation, sputtering and spraying? Under what circumstances do the graphene risk oxidation or tearing? Are there other types of damage that can occur? With all this in mind, this thesis is organized in the following way. Chapter 2 covers the production of graphene, mainly focusing on the CVD method. This introduction to the production should shine some light on the benefits and problems with utilizing the CVD methodology for device manufacturing. In chapter 3, the transfer methodology is covered. In this part, there will be a thorough discussion on how article I settles a common misconception about the mechanisms behind graphene transfer. Chapter 4 will cover the standard methodology of graphene evaluation with emphasis on Raman spectroscopy and electrical characterization. Chapter 5 will cover the actual studies of graphene's interactions with other materials. This will bind articles II to VI together and show just how important processing is when it comes to graphene. Chapters 6 will summarize the previous chapters and also cover my perspective regarding graphene's future in electronics.

2. Graphene production

Producing graphene is something that has been the focus of many groups and there are today a wide range of methods to produce graphene. These methods have different strengths and weaknesses and the choice of method must be made by compromises depending on the type of application. Unfortunately, at the moment of writing, there is still no method for creating wafer size mono crystals that could be utilized in the processor industry. The methods available today can be divided into two groups; bottom up and top down production. The first time graphene was made, it came from a novel top down method named micro mechanical cleavage, or more popularly the scotch tape method.[12] A piece of standard office tape was used to break off layers from a graphite crystal and placed them on a SiO_2 surface. Repeating this process resulted in a mono layer of graphite. Like the original process, almost all following top down production has been based on the idea of breaking down graphite crystals into graphene layers. The most common strategy is breaking down large quantities of graphite in liquids which later on can be deposited onto substrates. All of these top down methods deliver low quality graphene, where large area graphene films are made up by overlapping crystals without covalent bonds binding them together. Another method that should be mentioned is that of silicone carbide (SiC) graphene. It works by preferentially sublimating Si from the SiC substrate leaving a surface excess of C to crystallize.[34] The SiC technique in contrast to graphite suspensions delivers high quality graphene. However, the drawback with the SiC technique is that so far, it has not been possible to perform a large scale, high quality transfer of it from the bulk SiC, while at the same time as the bulk is not insulating.

The bottom up approach consists of different types of strategies where the chemical vapor deposition technique (CVD), in which a C carrying gas is decomposed at an elevated temperature in a hot-wall system, has been the most successful. The CVD technique delivers single layer films of covalently bonded graphene crystals that can be designed to meet any size requirements needed.[32] Engineers have been making graphene for decades in CVD systems without knowing it [35, 36]. Looking back at publications, C based flakes, which could possibly have been graphene, have been identified on furnace walls without further evaluation. CVD is an established thin film process that has been used for different materials for years. The reactions are controlled through adjustments of the gases' flowrates, chamber pressure

and the temperature. Through control over these parameters, a chemical process where a C carrying gas can decompose on a substrate surface can take place. It is desirable to have a surface controlled reaction mechanism as opposed to the reactions taking place in the gas stream which is a less controllable system. A stable and even control of the temperature is achieved by hot-wall system where the furnace encircles the reaction center. The gases' flowrates can either be controlled through careful sublimation of solids or by mass flow controller units coupled to stable gases.

Metals such as Ni,[15] Cu,[13] Pt,[36] Pd,[36] Ir[37] and Ge[38] have been the most successful growth substrates. One of the reasons is their catalytic ability to provide a medium where the C containing molecules can decompose while having a reasonably low C solubility. One of the requirements for the metal base growth medium is that it can lower the activation temperature of the C source used. CH_4, one of the most commonly used C sources, is a stable compound with a high C-H bond energy (440 kJ/mol)[39] and without a catalytic metal to facilitate the reaction it will decompose above 1200 ^oC. CH_4 decomposition in an heated Cu chamber has been studied and it has been estimated that from 700^oC and upwards the gas consists only slightly ($\leq$2%) of CH_4.[40]

Ni was one of the first metals to be successfully used as a growth catalyst; its lattice mismatch to a graphene crystal is below 1% which is unusually good, most metals have a much higher level of mismatch.[41] However, its high C solubility of 0.6 wt% at 1326 ^oC makes it difficult to find process conditions that do not lead to an uncontrollable amount of layers. Losurdo et. al. used spectroscopic ellipsometry as a real time measurement of the amount of C on the respective surfaces of Cu and Ni in a CVD system(see Fig. 2.1).[42] At the point marked "CH4 off" the C feed gas was stopped and the temperature was reduced so that the system was let to cool down. It here becomes obvious that the dissolved C is diffusing out to the surface of the Ni whereas in the Cu the C level remains stable. From the Raman data (see chapter 4.1) it is shown that the resulting number of layers of the graphene is close to one for the Cu foil but much higher for the Ni film. Pt has a low C solubility and has been shown to grow graphene at lower temperatures than Cu, indicating that it is a more efficient catalyst to decompose CH_4. It is, however, a significantly more expensive metal, which is why it is only in recent years that some groups have adopted it as their standard catalyst. With a good control of the CVD growth and the development of non-destructive transfer methods, (see chapter 3) more expensive growth substrates can be adopted.

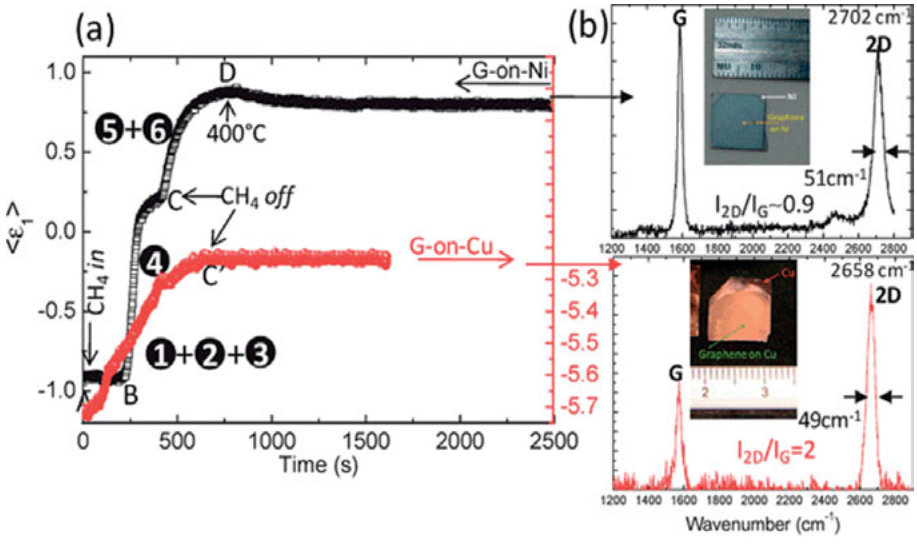

Figure 2.1 a) C concentration on Cu and Ni surfaces evaluated by real time ellipsometry and b) Raman evaluation of the corresponding graphene films. Reprinted with permission from ref [42]

Cu has, due to its low cost and extremely low C solubility (see Fig. 2.2), quickly become the most utilized catalyst for graphene CVD production. As shown in Fig. 2.1., Cu easily delivers over 95% coverage of single layer graphene (see chapter 4.1) on most types of foils even with a purity as low as 99.8%. The low solubility of C in the metal catalyst is one of the most important properties of the Cu substrate. With the low solubility of C in Cu the film formation can be tuned to be self-limiting (see Fig. 2.1). It has however been shown that it requires that the temperature exceeds at least 800 ^{o}C for the seed crystals merge into high quality graphene.[43] It is this easy accessibility to graphene through Cu-processing that is the reason all graphene utilized in this work is manufactured in this way.

The CVD of graphene on Cu foil can be divided into 4 separate steps; Cu-foil pretreatment, annealing, growth and cooling. The purpose of pretreating the Cu-foil is to remove contaminants and defects that could lower the quality of the graphene grown on top of it. It can be rinsing the foil in HCl solution to dissolve the native oxide so as to get a crystalline surface for the growth.[44] It can also be electro polishing the surface in a suitable electrolyte. Electro polishing is a well-tested method that can fill up micro sized cavities in the foil that otherwise could result in multilayer growth.[45] However, in our work no such methods were applied. Both HCl washing and electro polishing were evaluated without resulting in any measurable improvements as seen by Raman or optical microscopy. The conclusion was that the high temperature H_2 annealing in the subsequent step was sufficient for the reduction of the native oxide, resulting in vapor leaving the

system.[46] From optical microscopy it was also apparent that the high temperature of the annealing was adequate in smoothing out any micro scratches. It was therefore concluded that the electro polishing, even though it did successfully flatten the surface prior to the growth cycle, was superfluous.

In the annealing step, the native oxide in the foil is not only reduced and microscopic defects are healed, the Cu-crystals are also increased in size and their orientation becomes more textured. However, the literature [41] and our own empirical data show that graphene can easily grow across the Cu-crystal boundary. In our work, and others as well, the 99.8% Cu-foil from Alfa Aeaser is used.[47] We have been able to show through x-ray diffraction (XRD) that this film turns almost completely to the Cu (100) orientation after annealing at 1000 ^{o}C for 15 min.

For the growth cycle, consideration has to be taken regarding temperature, pressure and feed gases. Through thorough reviews [48] [49] of the published methods, it becomes apparent that any pressure can be applied when growing graphene as long as the C concentration is appropriately compensated. The temperature on the other hand is usually kept at 1000 ^{o}C. It has been shown that the higher the temperature can be kept, the higher the quality of the graphene can be expected. Cu has a melting point of 1084 ^{o}C which is the reason most groups use 1000 ^{o}C and even a few uses 1050 ^{o}C. This increase in temperature, as can be seen in Fig. 2.2, does not significantly change the C solubility.

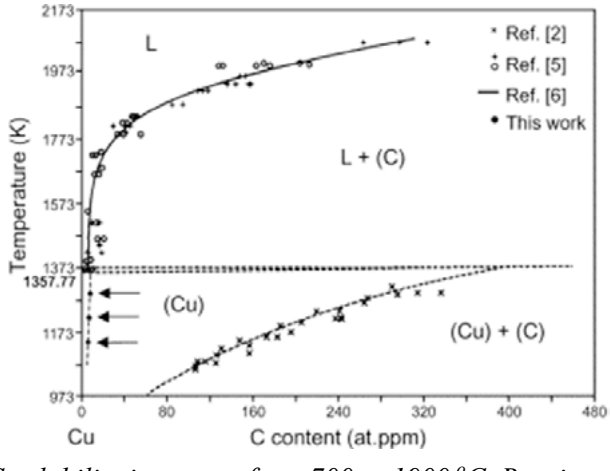

Figure 2.2 C solubility in copper from 700 to 1900 ^{o}C. Reprinted with permission from [50]

The route C takes to form graphene has been extensively studied, both in the gaseous phase and formation mechanisms on the growth medium. The normal way for evaluating the chemical route is by following isotope labelled C or H. In the literature several growth mechanisms have been published on the subject of graphene-CVD chemistry, a few of them indicating opposite reaction mechanism to each other. One suggested mechanism is that as the CH_4 adheres to the Cu-foil (Fig. 2.3 step 1), it will dehydrogenate and form a dimer (Fig. 2.3 step 2), followed by surface diffusion until coalescing with the crystal boundaries (Fig. 2.3 step 3).[42] [48]

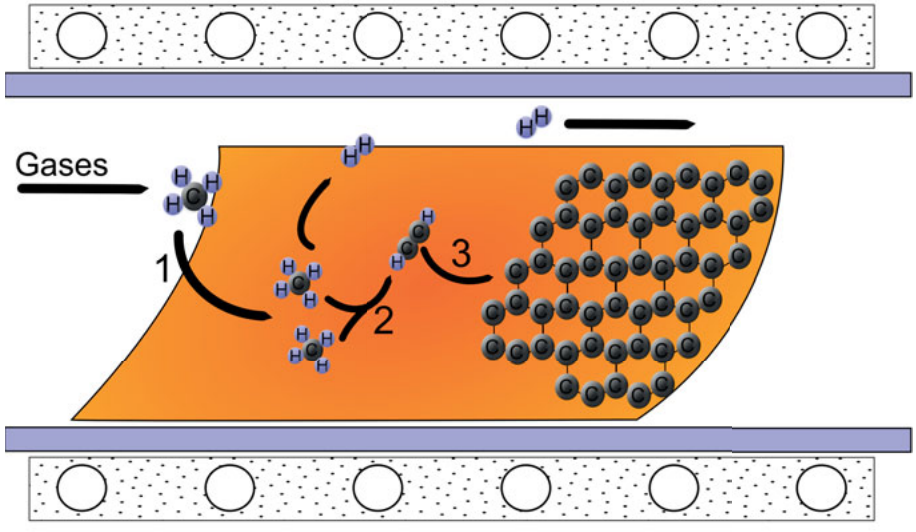

Figure 2.3 Illustration of the C route over a Cu foil.

In the last step of cooling it is important that the graphene is kept isolated from reactive species, e.g. O and H_2O, which could damage it. For this reason the cooling is usually performed under an inert atmosphere and not exposed to the ambient atmosphere until the system has reached less than 200 ^{o}C.

The growth of a graphene film over a self-limiting system, e.g. Cu foil, will have a growth cycle where the growth rate is dependent on the coverage. As the Cu becomes covered it will become increasingly difficult for the CH_4 to find a place on the surface to adhere. Isotopic labeling has shown that with gas compositions where the growth is optimized for single layer graphene the C is being added on to the sides of the seeds. However, if the growth allows for more than one layer to grow, the mechanism is less understood. The second layer always grows from the center of the first layer and always at a lower rate (Fig. 2.4). The growth mechanism of the second layer is still not clear.

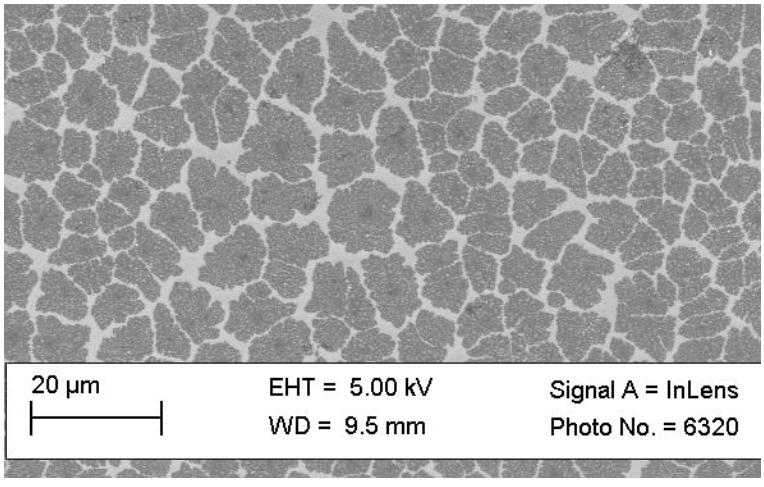

Figure 2.1.4 SEM image of non-finished graphene growth, transferred (see chapter 3) onto SiO_2. Note the darker spots in the middle of each crystal; these are the second layer of graphene growing out from the center

3. Graphene transfer

When implementing CVD graphene in a process there is need of transfer. This comes from the fact that the catalytic material, i.e. Cu-foil, might not be a desirable product substrate. In electronic applications, for example it is usually desirable to utilize the graphene on an insulating substrate, e.g. SiO_2 or a polymer. For this reason, several techniques for transfer have been explored,[14, 51] but none has been so widely adopted as the wet transfer technique described below.[17]

There are several precautions to take when designing a transfer method. Depending on which target substrate is intended, the support structure holding the graphene together during the process, solvents used and temperature need to be chosen carefully. For the common SiO_2 substrate (Fig. 3.1), almost no consideration needs to be made about temperature and solvents as it is fairly non-reactive. If the substrate intended is, for example, Polydimethylsiloxane (PDMS), it can be very sensitive to both chemicals[52] and temperature.[53] Both of these parameters can make PDMS swell which can damage the graphene. Perfect graphene can be stretched up to 20% without mechanical failure. However, in CVD-graphene this is reported to be close to 6%.[14] This means that graphene can, when placed on a surface that stretches during the transfer, be strained to a level where it is irreversibly damaged.

Figure 3.1 Photograph of a single layer graphene on 300 nm SiO_2/Si.

The idea of transfer comes from the carbon nanotube community where it had been implemented before it was adopted by graphene researchers.[54] [55] In the first publication regarding graphene transfer it was performed on micro-mechanical cleaved graphene and it was transferred from one SiO_2

surface to another, as a proof of concept. The following year it was published how this could be used for CVD-grown graphene and since then it has become a standard in the graphene community.[15] The transfer unfortunately can introduce a number of different defects to the graphene film (Fig. 3.2). When the graphene is grown on a polycrystalline metal film the surface will not have been uniformly flat. The graphene when it grows will conform to this topology, which will follow with the transfer to the new substrate. This can lead to wrinkles in the graphene film (green arrow, Fig. 3.2). If the foil contains unsolvable metal contaminants, they might form micro particles which can break the film or otherwise affect its properties (red arrow, Fig. 3.2). It is also virtually impossible to completely avoid tears and double folded areas (blue arrow Fig. 3.2,). Despite all these problems, the electrical behavior of CVD graphene is comparable to that of a higher quality of graphene where no such defects are present (see chapter 5.1 and 4.2).

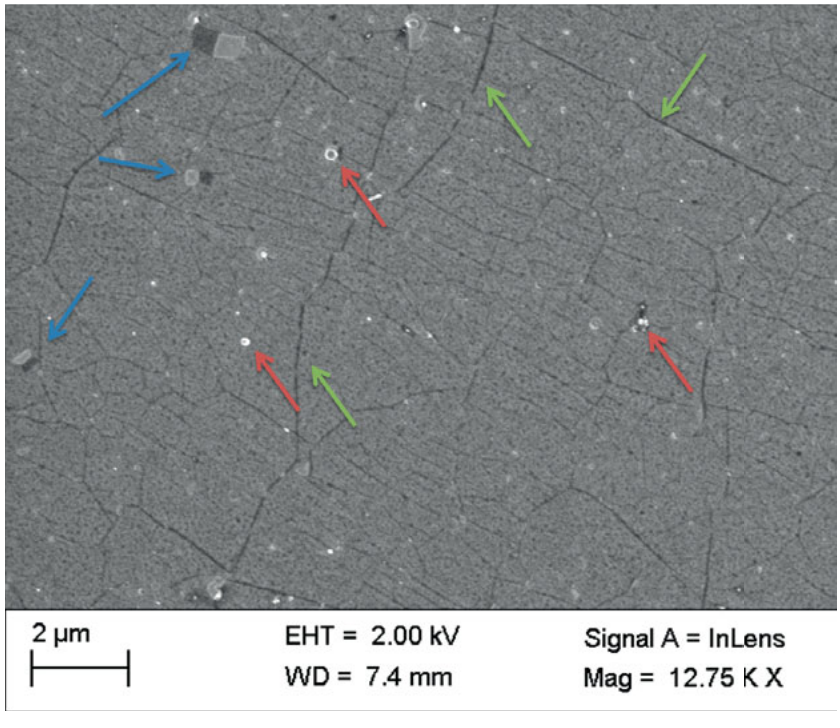

Figure 3.2 a) SEM image of a transferred graphene film on SiO_2. Blue arrows indicate micro tears, red ones indicate particles and green ones indicate wrinkles.

The outline of the transfer process consists of six steps. The first step is the addition of a support structure. The graphene is too fragile to be transferred without any type of support material holding it together. The most common method is that a polymer solution of poly(methyl methacrylate) (PMMA) is spin-coated onto the graphene while it is still on the growth metal and then

the sample is baked to cure the polymer (Fig. 3.3). Several polymers have been evaluated on the objective of finding the optimal polymer solution and curing conditions.[56, 57] A candidate that has been shown to deliver a cleaner end result than PMMA is poly(bisphenol A carbonate) (PC) dissolved in chloroform.[56] This method has, however, not caught on, likely due to the readily availability of PMMA in clean room laboratories, where it is used as photoresist, and due to the more severe health issues related to PC. An alternative curing approach that has been adopted by some groups is to use room temperature (RT) curing of the polymer solution, either overnight[17] or, as in our case, to utilize a low pressure chamber (see step 3). This soft-baking of the polymer makes it easier to remove from the graphene in the last step. It however means that the polymer film will display a significantly lower tensile strength, which we have seen increases the chances of the polymer film breaking during the transfer.

In the second step, the polymer/graphene is separated from the growth metal. This step is preferably performed in one of two ways. If the graphene has been synthesized on a low cost, low quality, easily accessible metal, e.g. Cu or Ni foil, the metal is simply etched away (Fig. 3.3). For Cu, $FeCl_3$ and $(NH_4)_2S_2O_8$ are the most commonly used etchants. An important part when choosing the etchant is that it dissolves the metal film carefully. $Na_2S_2O_8$ for example has shown to react too violently with Cu to be viable in the transfer process. The alternative approach applies when the growth metal is too valuable to sacrifice in the transfer. The polymer/graphene stack and the metal are in this case separated by means of electrolysis. The graphene stack is placed in an aqueous electrolyte together with a Pt counter electrode and current is passed between the Cu and Pt. This leads to H_2 gas bubbles forming at the graphene-metal interface which carefully separates them.[58] The second approach has become increasingly popular as it allows for re-using the metal foil. Expensive mono-crystalline metals can then be used to create a higher quality of graphene in the CVD process. In both methods, the polymer/graphene ends up floating on the liquid surface. Unless mentioned otherwise, the transfer method in this work has been utilizing the $FeCl_3$ solution.

The third step is cleaning to remove whatever chemicals were introduced in the second step (Fig. 3.3). Some groups have reported additional cleaning steps using aqueous solutions to increase the cleanliness, e.g. HCl and NH_4OH.[17] In this work no cleaning steps besides DI-water have been utilized. The polymer/graphene is transferred between water containers by sliding it up on a soft flat material and then sliding it down into the next container.

In the fourth step, the target substrate is cleaned from unwanted adsorbents that could negatively affect the graphene. This cleaning is most easily performed through O plasma processing or HF wet etching. For some substrates, this is not only about removing adsorbents. For SiO_2 and PDMS, it can also increase the hydrophilicity of the substrate. High hydrophilicity has

been shown to be very beneficial when graphene is placed on the substrate.[17] When the graphene is slid onto the last substrates surface the hydrophilic effect leads to a water cushion to form under the graphene. This cushion prevents the polymer/graphene film from wrinkling, working as a lubricator that allows the film to slide freely over the surface. This effect can be seen both at the initial point where the graphene is placed on the substrate as well as when the cushion evaporates away.

In the fifth step, the graphene is adhered to the substrate, commonly with a high temperature annealing at 90 ^{o}C or above. There was for some time a misconception off the understanding on how graphene actually adhered to the substrate during the transfer process. It was believed that a high temperature step was necessary before the support polymer could be removed, but conflicting interpretations on why this was important were published. Some believed that it was needed to allow the support polymer to relax for the graphene to adhere to the surface, e.g. heat the polymer to over the glass transition temperature (Tg).[59] A polymer heated above Tg will soften enabling the graphene film to relax onto the substrate. This would allow for a high contact area which would create an adequate adhesion between the graphene film and the substrate. The competing interpretation was that the wet steps in the transfer process introduced a thin film of trapped water at the interface between the graphene and the substrate. The function of the elevated temperature was therefore to remove the water barrier and as in the first interpretation increase the contact area.[17, 58] This was tested by our group in **paper I**, the thermal treatment for fusing the graphene to the substrate was replaced with a low pressure approach. Instead of heating the sample to the commonly used 150 ^{o}C in the fusing step, it was instead placed in a chamber with the pressure lowered to $2x10^{4}$ Pa while being kept at RT (Fig. 3.3). The Tg of the polymer is pressure dependent, but at this level it won't significantly affect the PMMA.[60] This approach was successful in delivering a continues graphene film with the same defect density as with the heated approach. An added effect from the RT approach was that the support polymer was not strongly bounded to the graphene film so it could easily be washed away with the same cleaning approach as before. This means CVD graphene can be used in a range of applications that otherwise would not be feasible. Polymers with low Tg that otherwise would swell or deform during high temperature processing, e.g. polystyrene or poly(vinyl acetate), can be utilized as substrates with this RT approach.

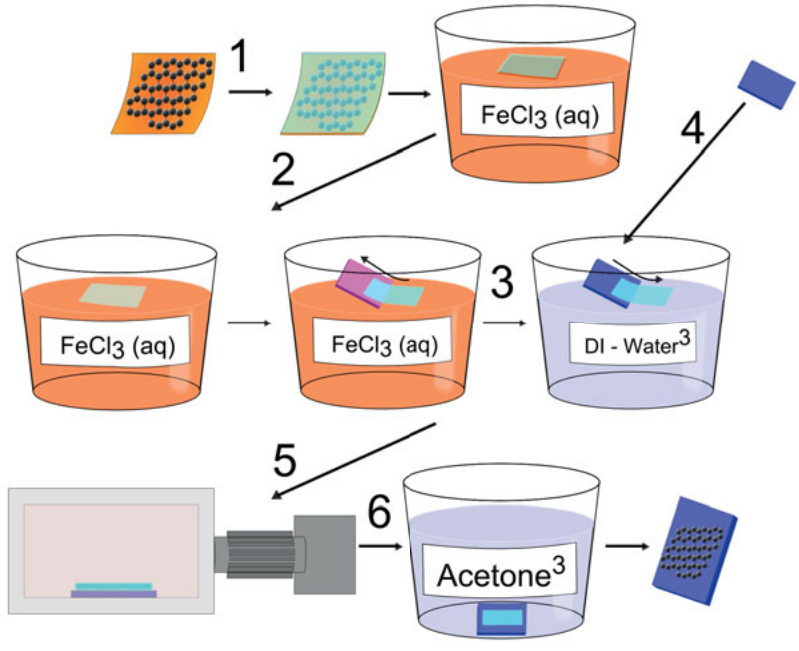

Figure 3.3 A schematic run sheet for graphene transfer. Steps 1 through 6 labelled in accordance with the text. The superscripted 3 indicates that the step is repeated 3 times.

Further evaluations of the new transfer method revealed that the low pressure could be combined with slight increases of the temperature to shorten the transfer time. At 40 ^{o}C, the transfer time could be decreased to as short as 5 min without any measurable loss in quality.

In the sixth and last step, the support polymer is dissolved. PMMA is commonly dissolved in acetone (Fig. 3.2) whereas if for example PC is used chloroform is the most efficient solvent. There have been mentioning in conferences on the benefits of stirring and heated solvents during the cleaning step. No such advantages have been noticed in our work.

4. Characterization techniques

Despite graphene being one of the strongest materials in the world, its extremely low thickness makes it very fragile. For this reason, the choice of evaluation methods is challenging; preferably it should be non-destructive while accurate. For the analysis and evaluation of graphene films some methods stand out more than others in their popularity. These methods deserve a closer look and are mentioned in the following sections.

However, there are methods that are frequently used but do not need the same amount of background information. Invaluable methods for the analysis of any kind of surface include scanning electron microscopy (SEM) and atomic force microscopy (AFM). SEM is particularly important as it can distinguish between graphene and less conductive materials where it is not possible to study the appearance optically. Due to its extremely low thickness and high transparency, graphene can be difficult to track visually on most materials, including metals and transparent substrates, unless a high contrast is achieved such as with a 90 or 300 nm layer of SiO_2 on Si.[61] SEM, on the other hand, can usually distinguish graphene from its substrate and deliver a direct image. In the present work, this is very advantageous when evaluating graphene growth on Cu-foil (Fig. 4.1).

AFM measures the height profile of a sample. This means that it can provide complementary information to SEM, with which height information can be difficult to obtain and even in some cases missed out completely.

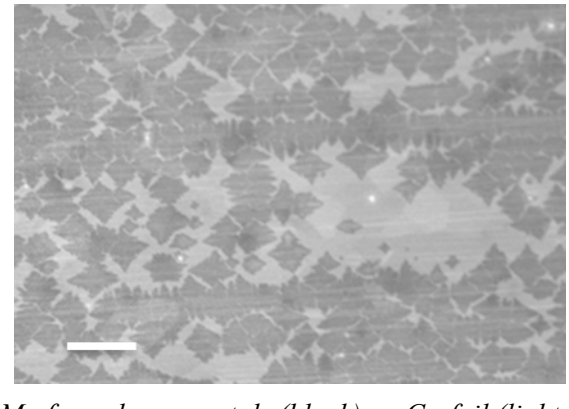

Figure 4.1 SEM of graphene crystals (black) on Cu-foil (light gray). Scale bar 100 μm.

4.1 Raman

Raman spectroscopy, after Chandrasekhara Venkata Raman, who discovered the underlying physical principle, has due to its non-destructive nature become the most trusted evaluation tool for graphene. The method analyzes the inelastic scattering as electrons are excited in graphene. Raman spectroscopy is both fast and nondestructive, while it simultaneously reveals information about the structural, chemical, and electrical properties of graphene.[62] The Raman measurement of the graphene lattice usually results in three distinct peaks, G, D and 2D peaks. These can be used to evaluate a number of parameters (Fig. 4.1.1). Most analyses are based on the intensity of these peaks, which in this work is approximated as the height difference between the baseline and the peak maximum. This is, for example, denoted I(G) for the G-peak. Sometimes the peak is too broad for the peak height to be representative and therefore the integral is used, denoted A(G). The G-peak, which can be found at 1600 cm^{-1}, originates from an in-plane breathing mode and has an intensity that is proportional to the amount of sp^2-sp^2 bound C, i.e. it is unrelated to the amount of layers or defects. This stability means that it is common to use the G-peak to normalize the spectrum intensity between different samples for comparison. The 2D-peak, which can be found at 2700 cm^{-1}, is only possible to see in the unharmed crystalline graphene and graphite layers and is sensitive to scattering effects. The 2D-peak is normally used to estimate the number of graphene layers present in the film. It is commonly accepted that if the intensity ratio between the 2D and G peak is greater than 2, i.e. $I(2D)/I(G) > 2$, and the 2D-peak is of a Lorentzian shape, the graphene can be classified as single layered.[62, 63] The D-peak, located at roughly 1350 cm^{-1}, also comes from an in-plane breathing mode of six atoms. This type of mode is normally not possible in graphene and a defect or edge needs to be introduced in its vicinity to activate it. For this reason its intensity is usually normalized to the G-peak intensity as an indicator of the defect density in the film, i.e. I(D) /I(G). A fourth peak that also is closely correlated to the presence of defects in graphene is the D'-peak. It is located at 1620 cm^{-1}, meaning that it is normally covered by the G-peak. For high enough defect density, it emerges as a peak superimposed on the G-peak (Fig. 4.1.1 L_D = 7.5 nm). Other peaks such as the C-peak, found at around 40 cm^{-1} and used to measure the number of layers, and the D''-peak, found at 2450 cm^{-1}, are mentioned in the literature but have not been used in this work. Another common peak to observe in the same range is found at 2330 cm^{-1}. This peak has been assigned to the Raman mode of N_2 gas surrounding the sample (Fig. 4.1.5).[64] The N_2 peak can typically be seen when there are defects in graphene or adsorbed molecules stuck to the surface. When graphene is processed, the crystal structure can be damaged by e.g. oxidation or tearing. This becomes visible in the Raman spectrum with the lowering of the 2D-peak in relation to the G-peak due to the loss of crys-

tallinity. Even the part of the graphene film which is close (~1 nm) to the defect can appear as without a 2D peak. Further, as now defects have been introduced which is necessary for the D-peak, it will start to increase. At some point, the D' peak will also become visible, overlaid on the G-peak. As more and more defects are introduced more states become possible, which can lead to a broadening of the G and D peaks, so that the G-peak effectively merges with the D'-peak (Fig. 4.1.1 $L_D < 5$ nm). This merged peak is commonly referred to as the G-peak only.

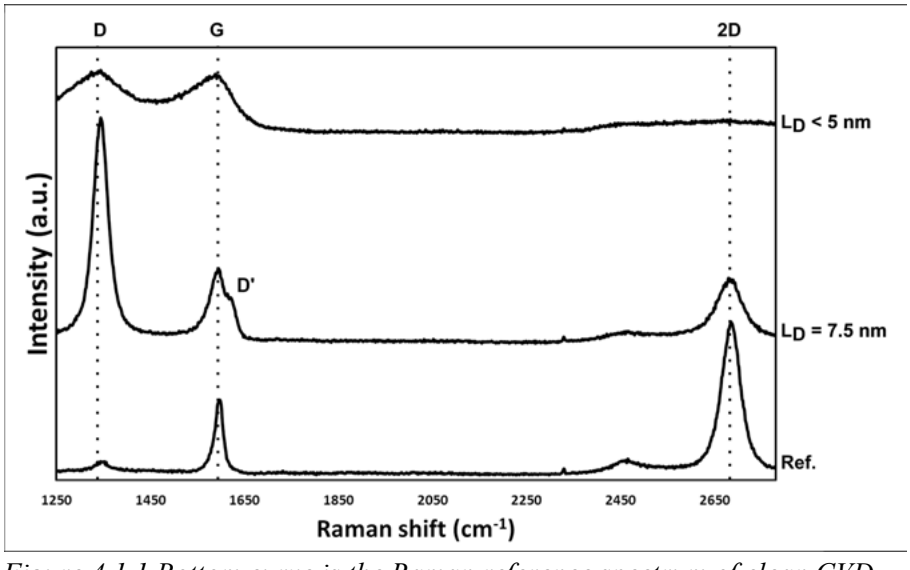

Figure 4.1.1 Bottom curve is the Raman reference spectrum of clean CVD graphene on a 300 nm thick SiO_2/Si surface. Upper curves are of the same system that has been bombarded with Ar^+ ions. L_D denotes here the average defect to defect distance in the respective graphene films (Eq. 4.1.1).

The position and full width half maxima of the G and 2D-peaks have been shown empirically to correlate to the Fermi level in graphene.[65, 66] This effective doping can be a result from process induced defects, by adsorbents (Fig. 4.1.2) or as a consequence of an external field shifting the Fermi level. Fig. 4.1.2 shows the G-peak position in two different situations. The one designated 'Vacuum' has been evaluated to be free from organic dopants as compared to the one denoted 'Heated' which is covered by a layer of PMMA (see chapter 3 and **paper I**).

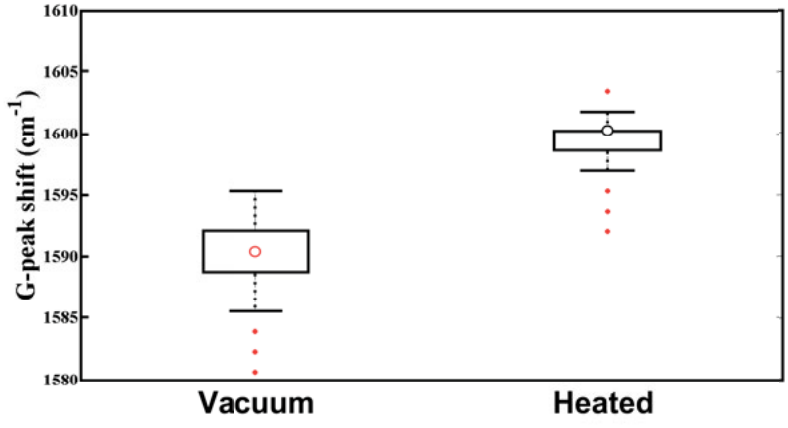

Figure 4.1.2 G-peak position in the Raman spectrum for different amount of PMMA doping of graphene. 'Vacuum' has less PMMA than the 'Heated' counterpart.

The defect density becomes a guiding parameter when evaluating the efficiency of graphene as a diffusion barrier. Ferrari et.al. published the equation below (Eq. 4.1.1) which describes how the average distance between defects in a graphene film can be estimated by the I(D)/I(G) ratio. Here, λ is the laser wavelength (532 nm) and k is a constant depending on the type of defect. For single vacancy defects, k has been estimated to be 1.8×10^{-9} nm^{-2} [67].

$$L_D = \sqrt{k\lambda^4 \frac{I_G}{I_D}} \qquad [4.1.1]$$

Depending on the model of the Raman system available, a combination of measurements can be conducted. The model available at the Ångström Laboratory supports the 2D mapping of samples. With this method, it is possible to evaluate the edges of graphene and identify crystal boundaries.[68] However, it is not a reliable method as it has been shown that zigzag edges cannot produce a D-peak. This is in contrast to armchair edges that not only show a D-peak, but its intensity is known to be proportional to the polarization of the Raman light. This can be seen in Fig. 4.1.3 where the I(2D)/I(G) ratio is significantly lower at the edges.

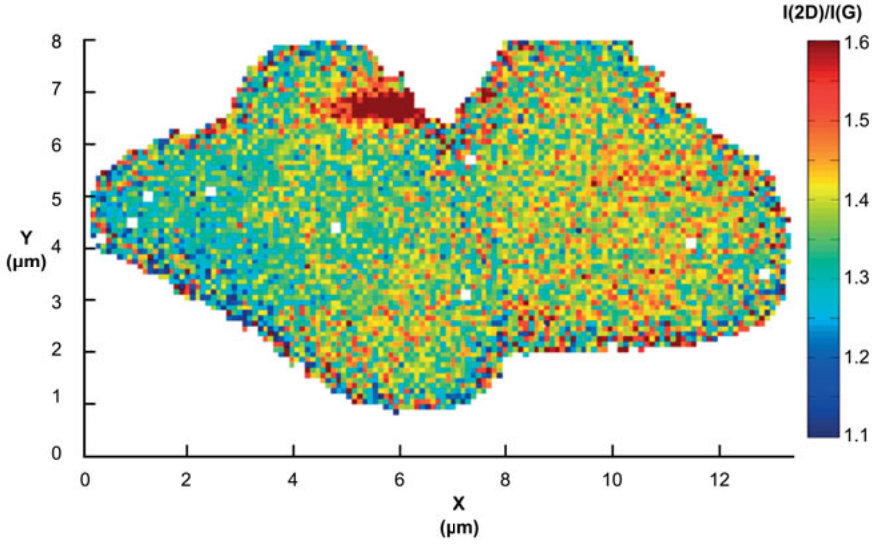

Figure 4.1.3 I(2D)/I(G) Raman mapping of a twin crystal of CVD graphene

If it is desirable to use Raman spectroscopy to evaluate the graphene surface but the conditions are such that the signal is too weak, surface enhanced Raman spectroscopy (SERS) can be utilized to enhance the signal strength. This can be achieved by having metallic nano particles deposited over the surface. The surface plasmon resonances (SPR) supported by such particles will create enhanced electromagnetic field in local regions which will strongly enhance the Raman signal. In **paper I**, Au nano particles are deposited by evaporation and it is shown that even very small distance changes (on the order of nanometers) between the graphene and the nano particles have a dramatic effect on the signal (Fig. 4.1.4).

These findings can be of great importance when utilizing a common evaluation method called tip-enhanced AFM. With standard AFM the system moves a tip over a sample and measures the height difference. In tip-enhanced AFM, the tip acts as a nano particle and the AFM can be combined with SERS measurement to simultaneously map both the Raman data and height of a sample.

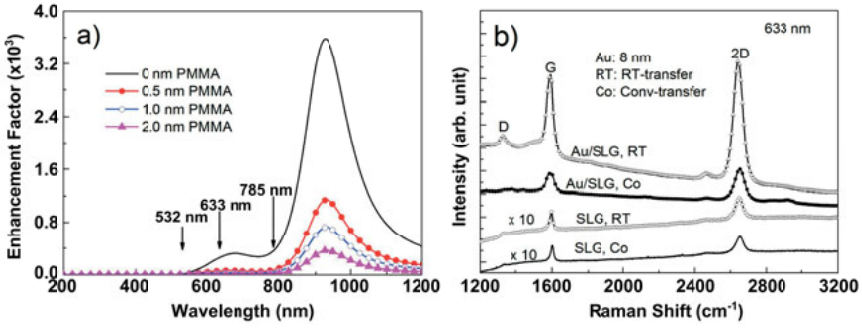

Figure 4.1.4 a) The calculated enhancement factor as a function of wavelength for different thickness of PMMA between the graphene and Au-particles b) Raman spectroscopy at 633 nm wavelength of clean graphene and graphene with a dirt layer of PMMA on it, shown with and without SERS effect.

In this work, it has been noticed that there is a negative effect on the Raman signal strength when graphene is placed on a metal film. It is normal that as the number of layers of graphene increases, the Raman spectra will start appear as that of graphite. When the number of layers surpasses 5, the multi-layer graphene should no longer be distinguishable from graphite.[69] However, when graphene is placed on Al the graphene signature only becomes more prominent when increasing the amount of layers (Fig. 4.1.5). This effect might originate from the Al quenching the signals coming from samples close to it, and the fact that the layers are added separately and therefore will behave more as single layers than a crystal stack.

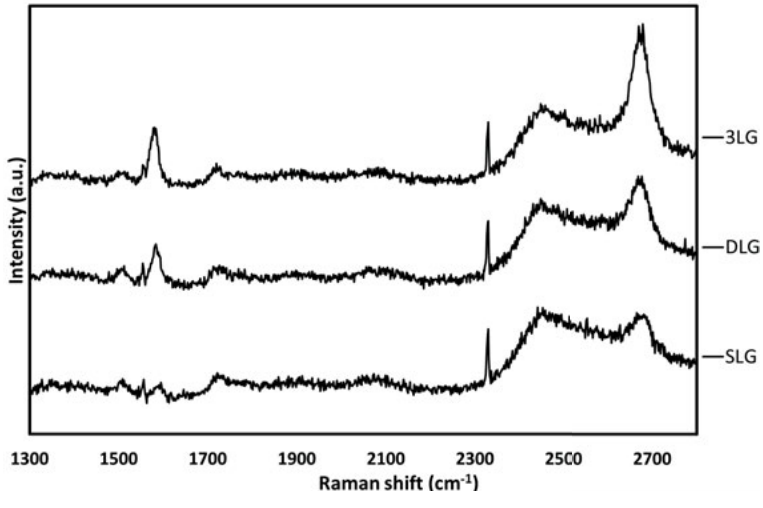

Figure 4.1.5 Spectra of different amount of layers of graphene on Al.

4.2 Electrical

To evaluate the parameters in graphene that are linked to its electrical behavior, e.g. doping level, Raman and other nondestructive analyses can be utilized. However, to get a correct measurement of these parameters, there is no alternative to direct evaluation of a graphene field effect transistor (G-FET). In this work, mostly a double gate G-FET structure has been utilized (Fig. 4.2.1). The reason for utilizing a top gate structure is that it can act both as a barrier to isolate the graphene channel from the surroundings as well as a top gate. Graphene can be sensitive to the surroundings and even ambient atmosphere can lead to severe doping of it. All electrical evaluations in this work were performed on an Agilent source measure unit (SMU), either model 1550C or B1500 for DC evaluations. Samples were placed in a Faraday cage and contacted through W probe needles and triaxial cables to the SMU. Backgate potential was controlled through the sample chuck.

Some considerations have to be taken into account when comparing published transistor behaviors. The length of the channel is of great importance as the mean free path for an electron in an ideal graphene channel is over 1 µm.[70] Some G-FETs utilize a channel length below 100 nm whereas in this work 20-200 µm is the norm. This choice in size is due to the interest of implementing graphene in macroelectronic systems.

Graphene became sensational news when it was first isolated mainly due to its astonishing electrical properties. The mobility was the highest ever measured, meaning it was an excellent conductor for being so thin, and the lack of a bandgap made it a special semimetal.[21]

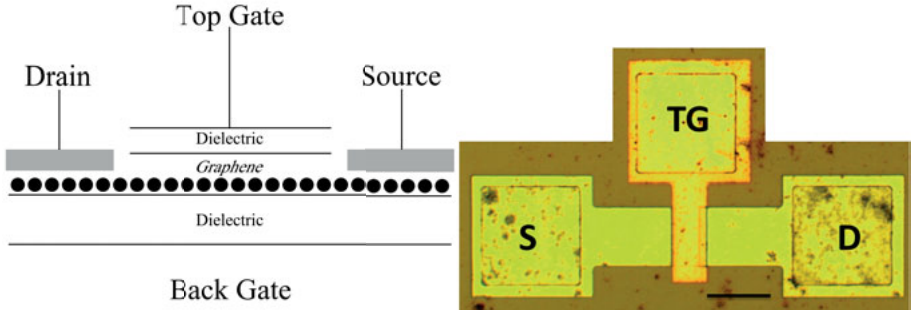

Figure 4.2.1 a) Standard layout for a double gated G-FET b) Photograph of an in-house manufactured G-FET, scale bar is 50 µm.

When graphene is exposed to a varying electrical field, its conductivity will change as in a semiconductor. This is due to the shift of the Fermi level in the band structure resulting in a change of the carrier concentration which is coupled to the conductivity. However, in graphene, unlike most other known semiconductors there is no bandgap and both holes and electrons have almost equal mobility. This results in an ambipolar field effect behavior which

is seen as V-like transfer curves (Fig. 4.2.2). The minimum conductance point is commonly referred to as the Dirac voltage (V_{Dirac}), it theoretically corresponds to the voltage when the Fermi level is balanced at the Dirac point in the band diagram. The Dirac point is the point in the graphene's band diagram where the conductance band meets the valence band (Fig. 1.2). The minimum conductance of a G-FET is commonly reported to be ~$4q^2/h$ = 0.16 $\mu\Omega^{-1}$ where h is the Planck's constant and q the electron charge. The fact that the conductivity is not 0 when the density of state (DOS) supposedly is, is still not perfectly understood. Mostly it is explained by carriers being thermally excited to the conductance band and doped puddles of carriers that arise from a non-perfect system.[21] The standard expression for conductivity of a semiconductor (Eq. 4.2.1) is stated as a function of mobility, μ_n and μ_p for electrons and holes respectively, q and the carrier concentrations, n and p for electrons and holes respectively.

$$\sigma = q(\mu_n n + \mu_p p) \qquad [4.2.1]$$

The transconductance, g_m, (Fig. 4.2.1, red curve) which is calculated from the field induced conductance (Eq. 4.2.2) can be used to find V_{Dirac} and the field effect mobility, μ_{FE}.

$$g_m = \frac{dI_D}{dV_G}|_{V_{DS}=constant} \qquad [4.2.2]$$

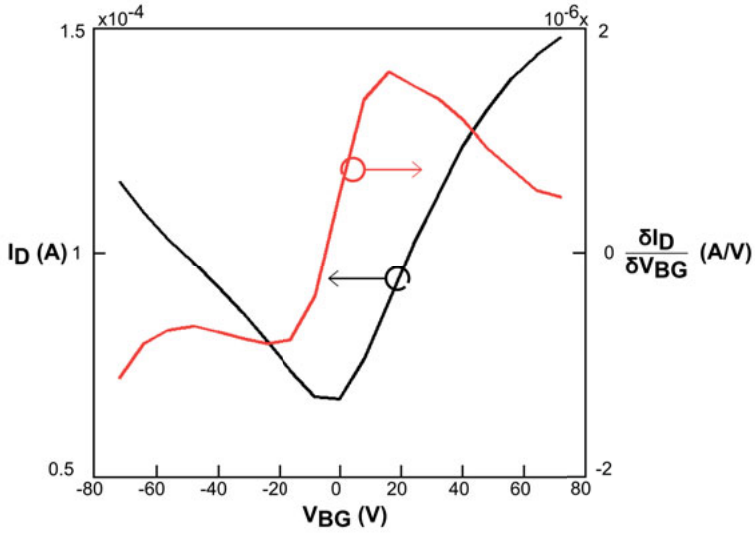

Figure 4.2.2 Black line: drain current vs. back gate voltage with grounded topgate in a double gated G-FET. Red line: corresponding transconductance. V_{DS} = 0.1 V.

To evaluate a transistor, it is common to extract the μ_{FE}. It is a direct value of the transistors respond to a field. This value can be extracted from the trans-conductance, oxide capacitance (Cox), source-drain voltage (V_{DS}) and the channel dimensions length (L) and width (W) in the following equation.[23]

$$\mu_{FE} = \frac{g_m L}{W C_{ox} V_{DS}} \quad [4.2.3]$$

However, the μ_{FE} usually results in a low mobility. It is therefore more common to use the effective mobility (μ_{eff}). A graphene channel behaves close to an ideal resistor, in the sense that its current will change linearly with the V_{DS}, when V_{DS} is sufficiently close to 0, i.e. 0.1 V. This linear behavior means that it is sufficient to approximate the channel conductance (Eq. 4.2.4) from the transfer curve.

$$g_D = \frac{dI_D}{dV_{DS}}|_{V_G=constant} \approx \frac{1}{R} \quad [4.2.4]$$

μ_{eff} can from these approximations be calculated (Eq. 4.2.5). In graphene, there is an intrinsic quantum capacitance that has been reported to be around 0.8 μF/cm^2. It stems from the extreme low DOS which as in all semiconductors result in a lowered charge density. The quantum capacitance can be relevant for devices with dielectric layers with higher capacitances. However, for the devices in this work, the oxide capacitance was sufficiently low to allow for the quantum capacitance to be negligible. The induced charge, Q_n, is approximated by the standard expression of $Q_n = C_{ox}|V_G - V_{Dirac}|$. It is in this approximation that the quantum capacitance would affect the calculation.[71] However, at low $|V_G - V_{Dirac}|$ the quantum effect is about one percent for the devices evaluated in this work, and drops exponentially as the voltage difference increases.

$$\mu_{eff} = \frac{g_D L}{W Q_n} \quad [4.2.5]$$

We can approximate that on each side of V_{Dirac}, the carrier is only of one type. Hence, the conductivity measured in Fig. 4.2.1 together with Eq. 4.2.1 and 4.2.5, can be used to estimate the carrier concentration (N) in a G-FET (Eq. 4.2.6, Fig. 4.2.2). For graphene the theoretical intrinsic carrier concentration at RT is $n_i \approx 9\text{x}10^{10}$ cm^{-2}.[72]

$$N = \frac{1}{\rho \mu_{eff} q} \quad [4.2.6]$$

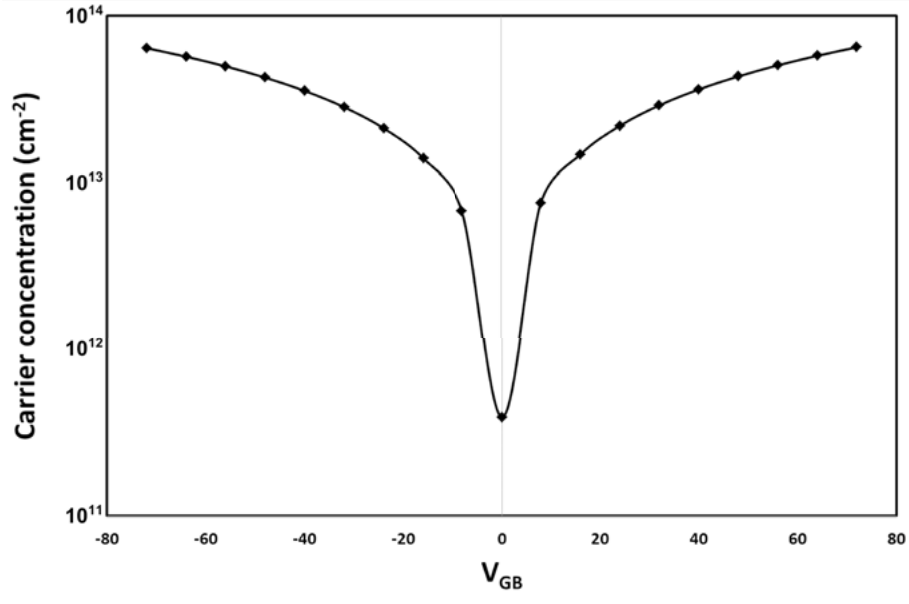

Figure 4.2.2 Carrier concentration in a G-FET vs. gate voltage as calculated from the data in Fig. 4.2.1

The effective doping level in a G-FET is measured as a function of the shift of V_{Dirac} from the 0 V position (N_D for donors and N_A for acceptors). It is desirable that the doping from a process is controllable in such a way that V_{Dirac} ends up at 0 V if that is the aim. This is due to the implication that if V_{Dirac} = 0 V, then the process has had no influence on the doping of the graphene. However, it can be difficult to determine if there was no influence from the process or if the dopants are just equally balanced. An effective sum of doping concentration lower than 10^{11} cm^{-2} will only negligibly add to the carrier concentration and not be detected with this approach. The net doping effect of a G-FET is estimated by its shift from the intrinsic transfer behavior (V_{Dirac} = 0 V). In Eq. 4.2.7 A is the channel area.

$$N_D + N_A = \frac{C_{ox} V_{Dirac}}{Aq} \qquad [4.2.7]$$

In most FET systems there is a measurable shift between a transfer curve when the gate voltage is swept forward and backwards. This is what is referred to as hysteresis. This hysteresis can arise due to several different reasons such as trapped interface charges (N_{it}) and oxide trapped charges. It is in this work calculated in accordance with Eq. 4.2.8 and 4.2.9.

$$\Delta V_{Dirac} = V_{Dirac,\ Forward} - V_{Dirac,\ Backward} \qquad [4.2.8]$$

$$N_{it} = {}^{\Delta V_{Dirac} C_{ox}}/_{2q} \qquad [4.2.9]$$

With the interface state charge calculated according to Eq. 4.2.9, the sweep range of the gate voltage is of interest. If the hysteresis increases with the range it is most likely originating from charge injection in the oxide and interface traps. A Si/SiO_2 system is expected to carry these types of traps in a density around 10^{11} cm^{-2} making hysteresis likely.[73]

The work function difference between graphene and Si is found to give a shift of V_{Dirac} which should not be ignored. The work function of Si is 4.6-4.9 eV and the graphene's is usually reported to about 4.5 eV. This correlates to a shift of V_{Dirac} up to 0.4 V.

It has been reported that for 2D channel field effect devices with a double gate structure, where the top gate is at a floating potential, special care has to be taken when evaluating the transistor parameters.[74] When sweeping the back gate voltage, a coupling to the top gate metal can induce unaccounted field effects leading to an over-estimation of the μ_{eff}. This means that the effective capacitance might differ from the gate capacitance and needs to be recalculated. In Eq. 4.2.10 the C_{bg} and C_{tg} are the capacitances between the channel and the back gate and top gate respectively. The C_{bt} capacitance comes from the contact pads overlap to the backgate. Here, it becomes apparent how two seemingly similar structures can exhibit different behaviors. For nano sized channels with thin dielectrics, the contact pad capacitance can be the dominating factor in Eq. 4.2.10. If otherwise, the channel is hundreds of μm^2, as in this work, the contact pad coupling effect can be considered negligible. In this work, the top gate and its contact pad is at fixed voltage if not otherwise stated so as to avoid these uncertainties.

$$C = C_{bg} + (C_{tg}^{-1} + C_{bt}^{-1})^{-1} \qquad [4.2.10]$$

4.3 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) works by measuring the bonding energies present in the sample. This allows the analysis to distinguish between not only different elements but also different chemical bonds.[75] It does this by exciting different orbital energy levels by means of x-rays which results in an emission of detectable photoelectrons whose energies can be correlated to the binding energies in the targeted sample.

XPS has become one of the standard methods for evaluating the effectiveness of removing the polymer in the end of a graphene transfer process. As it can distinguish between the pure sp^2-hybridized C of graphene and the O bonded C in PMMA, it can be used to quantify the level of polymer contamination. In Fig. 4.3.1, the difference between clean graphene and PMMA covered graphene is discernable. The integral of each peak is proportional to the mass present in the system curve fitting can therefore be used to estimate the ratio between graphene and contaminant.

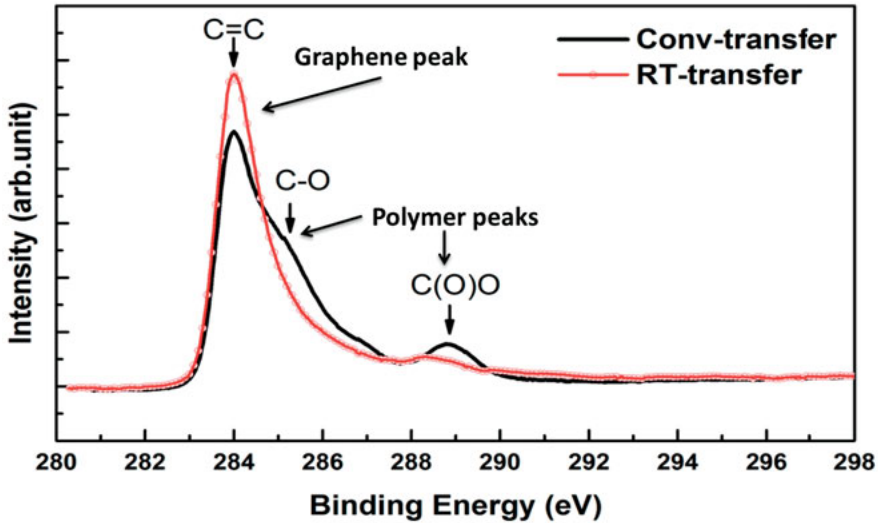

Figure 4.3.1 XPS data comparing a clean graphene film (red) from one that is contaminated by PMMA (black).

XPS is also very sensitive toward surface contaminants and can identify different compounds even at surface concentration below the level of saturation. In **paper II**, the level of I_2 present on the surface of graphene after different processes could be evaluated even though the mass present was less than one adatom per C.

5. Thin-film deposition

Thin-film deposition is the process of applying an arbitrary thin layer of some material. The thickness is commonly ranging from an atomic monolayer to a few microns. The first thin film depositions can be traced back tens of thousands of years to cave paintings. It is believed that paint was spouted from the mouth against their hand and so transferred the hand pattern to the cave wall. The idea of an aerosol based stencil painting method is still something applied in art and industry. Over the years, other techniques have been introduced and there is now a range of different approaches. There is now the possibility of optimizing a production processes so that high quality films can be manufactured in the most efficient way. In this work, the focus is on four of the most common methods, chemical deposition techniques, evaporation, sputtering and macro deposition. Chemical deposition is divided into two separate sections, 5.1 and 5.2, based on if the chemicals are carried by gas or liquid. Evaporation and sputtering, sections 5.3 and 5.4, respectively, are both physical vapor deposition methods, i.e. these depositions are carried out in vacuum systems. Macro deposition, section 5.5, represents the methods that deal with droplets or larger, e.g. air-brush or inkjet printing. Below are the physical vapor deposition methods covered in this work, illustrated by their possible kinetic energy at impact.

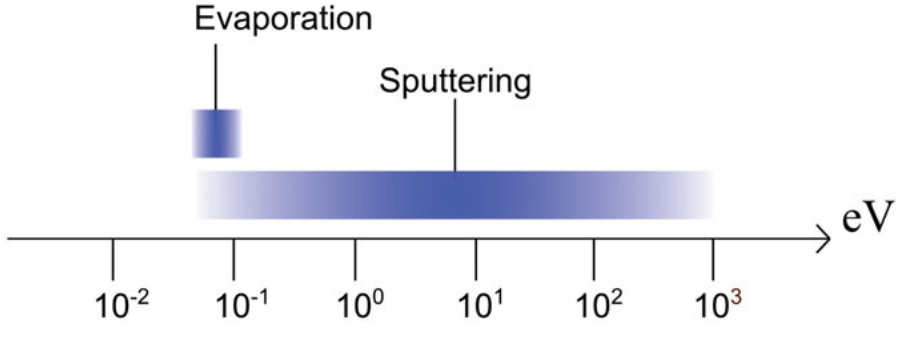

Figure 5.1 Kinetic impact energies for physical vapor deposition methods.

In thin-film deposition on graphene, the most direct concern is that of inducing damage to the graphene film. The deposition method can, if energetic enough, break the graphene lattice. The energy needed for displacing a C atom from the graphene lattice can be calculated by Eq. 5.1.

Here, E_d is the displacement energy, E_{min} is the lowest energy required for displacing C atoms in graphene, M the mass of the incoming particle and m_c is the mass of a C atom. E_d has been found to be ~22 eV through simulations[76], which is in the lower part of the sputtering region in Fig. 5.1. This means that for Ar, which is a common particle in sputtering processes, E_{min} is around 32 eV.

$$E_{min} = \frac{E_d(m_c+M)^2}{4m_cM} \quad [5.1]$$

As we can see in Fig. 5.1, the sputtering technique has the ability of exceeding the energy required for displacement. Sputtering will therefore, together with the macro spray deposition method, be considered high energy deposition. The high energy deposition methods will be scrutinized mostly based on their ability to be utilized without introducing significant damage into graphene, whereas the low energy deposition methods will be studied based on their chemical impacts.

In Fig. 5.2, the standard process flow that has been adopted in this work is outlined. This process relies on several thin-film deposition steps to be carried out directly onto graphene. To protect graphene from interacting with polymers in photo resist (PR), which is severely damaging to graphene, it is covered by a protective metal layer from the start. In **paper II** and **III**, this metal film is evaporated Au or Cu (Fig. 5.2 step 1). Some published strategies rely on a protective metal film being evaporated onto the graphene, before the transfer step to protect it from PMMA.[77] This, as we have evaluated, results in a stiffer film and worse transfer result. With a protective layer present on graphene a top-down production process is possible without introducing PR polymers directly onto the graphene surface (Fig. 5.2 step 2). The metal is patterned as desired by photo-lithography and wet etching (Fig. 5.2 step 3). Graphene can this way be patterned by reactive ion etching (Fig. 5.2 step 3). When graphene patterning is finished the metal is etched in such a way that the channel is uncovered and the residual metal is left as contacts (Fig. 5.2 step 5). This is followed by covering graphene with an Al_2O_3 layer by means of atomic layer deposition (ALD). The ALD Al_2O_3 is facilitated by the evaporation of an appropriate seed layer (Fig. 5.2 step 6). In the end, the Al_2O_3 is covered by a metal top-gate (Fig. 5.2 step 7).

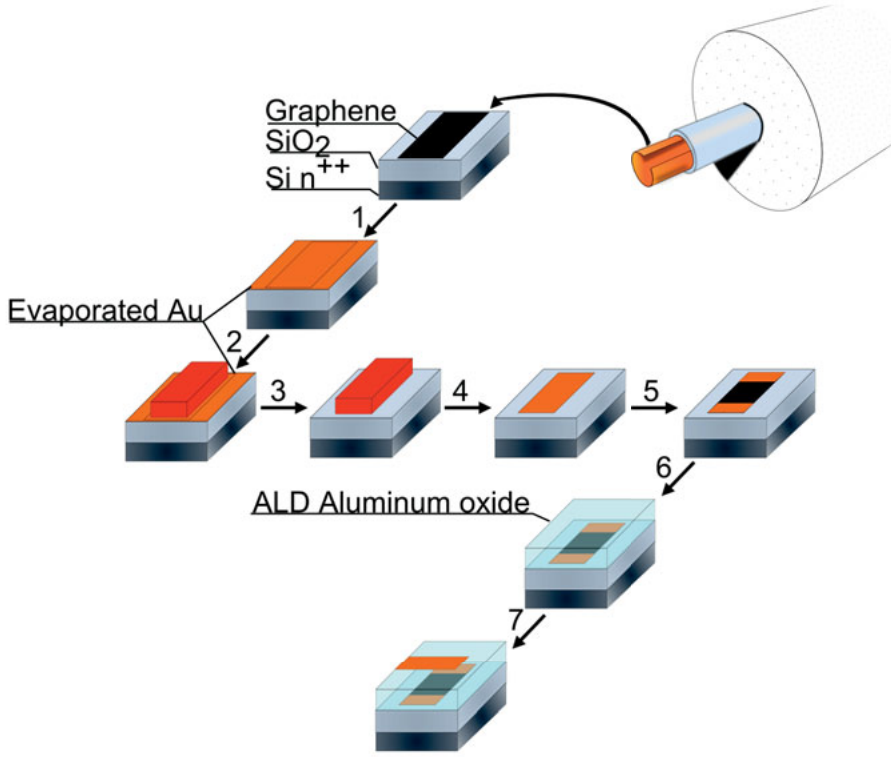

Figure 5.2 Standard process flow for manufacturing double gated G-FETs.

5.1 Chemical gas deposition

This section covers the ALD technique. The technique acts by pulsing a series of gaseous or aerosol chemicals with a purging cycle between each alternating pulse. When these chemicals react with each other they form a more or less amorphous film. The chemicals can either adsorb to the surface through physisorption or through chemisorption. On a graphene surface it is usually strived for physisorption as it otherwise would mean that the graphene lattice would have been disturbed. ALD is commonly adopted for oxide deposition purposes. The O part of the oxide can be taken from H_2O or H_2O_2.[78] Most commonly, H_2O is utilized due to its availability. Due to the high hydrophobicity of the graphene surface, it is therefore common to perform a preprocessing step to introduce reaction sites for the H_2O molecules to stick to. Several alternatives have been made available over the years. The graphene can be "activated" through O_3 which breaks the crystal and form oxidized sites that are reactive. The surface can be covered with a seed layer, preferably of the same material as the desired film. These seeds can be evaporated, in this work it is restricted to the evaporation of Al nano-particles (see chapter 5.3) that are spontaneously oxidized in air prior to the ALD process. The focus in this work has been on $Al(CH_3)_3$ (TMA) and H_2O deposition for Al_2O_3 formation.

An appropriate temperature has to be chosen for the target substrate so as to come as close as possible to a continuous mono-molecular coverage of the sample per pulse. Studies have been conducted showing that the hydrophobicity of the graphene surface can be balanced with the substrate temperature to form continuous water films. For a certain temperature window of 100-130 ^oC, H_2O molecules can deposit as a continuous film over graphene and thus making the Al-seed layer unnecessary.[79] However, it has also been shown that in order to achieve a high quality dielectric the substrate temperature should not be below 300 ^oC.[80] In **paper II**, the temperature was tested both at 100 and 300 ^oC throughout the deposition. The 100 ^oC recipe did not result in a functioning G-FET with intrinsic behavior. This is partly due to a lower quality of the Al_2O_3 with a higher concentration of trapped charges.

In **paper II**, an additional effect from the ALD process was identified. When performing step 6 in Fig. 5.2, the graphenes electrical behavior changed dramatically, going from metallic to semiconductive. This change was greater than what was expected from removing the ambient effect on graphene.[81] From XPS, it was concluded that the manufacturing process introduced I at the KI_3 etching in step 5 (Fig. 5.2), which after the ALD step had vanished. The deposition mechanism of Al_2O_3 and the Al + I chemical reaction on graphene is illustrated below (Fig. 5.1.1). In the first step, the TMA reacts and chemisorbs to present OH groups releasing one CH_4 in the process. In the subsequent intermediate step, a second CH_4 is released. When the H_2O is introduced in the third step it reacts with the remaining CH_4 group, resulting in a new OH group.

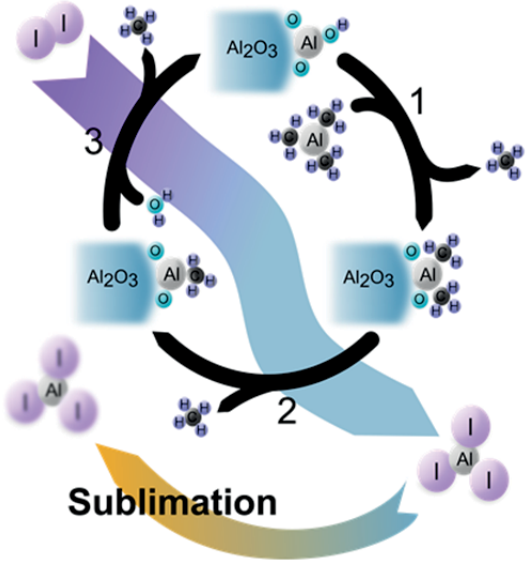

Figure 5.1.1 Illustration of the ALD cycle for forming Al_2O_3 from TMA and H_2O (black arrows). The suggested cleaning function for removing I_2 contaminants are given as a side reaction (colored arrows).

The electrical behavior of graphene changed from highly doped to intrinsic after the ALD process (Fig. 5.1.2). This mechanism is explained by the fact that ALD performed at 100 ^oC does not result in this intrinsic behavior but shows a V_{Dirac} significantly far away from 0 V. This is consistent with the proposed theory that low temperature ALD will reduce any water present on the graphene surface but does not allow AlI_3 to form. At 300 ^oC, the reaction results in the formation of AlI_3 which sublimates at the pressure in the ALD chamber. However, at lower temperatures (<234 ^oC) AlI_3 will not sublimate but will instead form the much more stable Al_2I_6.

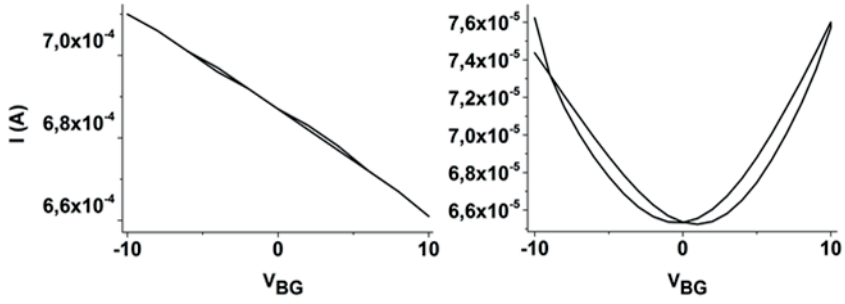

Figure 5.1.2 The electrical behavior of a G-FET a) before and b) after its been covered by an Al_2O_3 ALD film

The success of the ALD process is directly coupled to its ability to form continuous films of its feed gases. This becomes obvious when the ALD process is coupled with a hydrophobic substrate. Graphene, due to its extreme thinness, exhibits similar wettability as its substrate.[82] A common way to achieve a hydrophobic SiO_2 surface is to treat it with hexamethyldisilazane (HMDS) that bond covalently to the substrate surface. In Fig. 5.1.3, the change in the electrical transfer behavior of an ALD treated G-FET is compared between the two cases. Pure SiO_2 and HMDS treated SiO_2 is used as the substrates. The HMDS will affect the ALD process as it repels the H_2O molecules from the surface. As no reaction can take place in the graphene-Al_2O_3 interface, it will instead result in CH_3 groups remaining close to the graphene surface. These CH_3 groups can interact as dipoles on the surface, which have been shown to induce the unipolar behavior.[73]

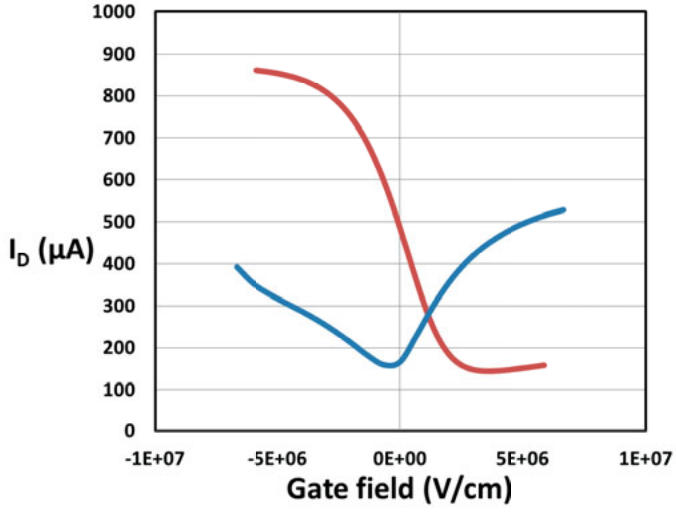

Figure 5.1.3 G-FET conductance vs. gate field for graphene on plasma cleaned SiO_2 (blue curve V_{DS}=0.1 V) and graphene on HMDS treated SiO_2 (red curve V_{DS}=0.12 V).

5.2 Chemical solvent deposition

Chemical solvent deposition is the deposition method of soaking an object in solvents of adhesive molecules or atoms. By controlling the temperature and the solvent concentrations the process can result in the desired surface concentration. The goal is not to build a device but rather to dope or functionalize the surface. The sp^2-hybridized structure of graphene opens up for different types of spontaneous chemical adhesions, e.g. MoO_3 and I.[83] The most well-known adsorption in this context is the π-π stacking where the delocalized π-electrons in graphene interact with the π-electrons in other aromatic molecules.[84] This has been shown to result in molecular layer depositions on the graphene surface. However, as already mentioned in the previous section on ALD, graphene is thin enough to allow for the substrate properties to shine through. Wettability is, by now, a well-known effect but there are indications that other properties can also be affected by the substrate. It has been noticed in our work that the adsorption of different molecules is influenced by the substrate under the graphene film. For instance certain molecules can stick on graphene on SiO_2 while not on graphene on Pd. This effect can be of interest as a strategy for self-directing functionalization, e.g. biolinkers or organic semiconductors. A likely explanation is that the SiO_2 atoms on the surface are oriented in such a way that O is overrepresented toward graphene thereby resulting in a charged double layer between the Si and O atoms. The O atoms will be negative and this charge can be transmitted to the top side of the graphene film. Pd is an inert metal and thus no such effect is present. This effect is not limited to aromatic systems such as sodium dodecyl benzenesulfonate (SDBS) but is also seen in the non-aromatic sodium dodecyl sulfate (SDS). In Fig. 5.2.1 the XPS data for graphene on different substrates that have been submerged in aqueous solutions of SDBS and SDS are presented. The different types of substrates are present on the same sample and the difference in S concentration on them is obvious. This suggests that it is the electrostatic charge in the adsorbent that governs such depositions.

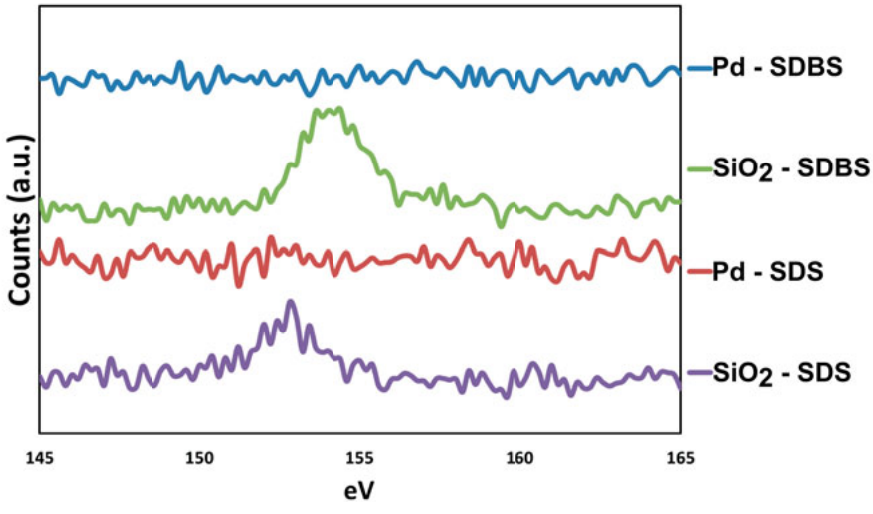

Figure 5.2.1 S presence on graphene, with either SiO_2 or Pd substrates, as evaluated by XPS for SDBS and SDS molecules. There is an S peak on the SiO_2 substrates but not on the Pd.

5.3 Evaporation

Evaporation is a very well established deposition method for metals and organic thin-films. The nature of the method where metals are heated to the point of sublimation under reduced pressure allows for low kinetic energies as can be seen in Fig. 5.1.[85] The substrate is placed facing the metal source and far enough away that most of the incoming atoms will hit the surface perpendicular to its plane, but still sufficiently close so as to obtain an acceptable growth rate. Conventional evaporation uses a thin deposition of Ti (<10 nm) as an adhesive layer between Si or SiO_2 substrate and the desired metal.[86] For graphene, the adhesive forces between it and the substrate is usually so low that an adhesive layer is considered redundant. Instead, in this work, contacts are formed directly on the SiO_2 substrate and then connected to the graphene structure. This results in a sufficiently mechanically stable system (Fig. 4.2.1).

In **papers I, II** and **III**, evaporation is used for applying metal nanoparticles onto graphene. As mentioned earlier (see section 5.1) whenever the ALD technique is utilized for graphene, a seed layer is crucial for the precursor molecules to have something to adhere to. Here, the key issues when depositing a seed layer are to not fully cover the surface (Fig. 5.3.1). In **paper II,** the non-invasiveness of the evaporation process is thoroughly put to the test as graphene is directly exposed to evaporation at two separate occasions (Fig. 5.2). At first it is covered with an Au film which is patterned (Fig. 5.2 step 1) and then removed by wet etching (Fig. 5.2 step 5). It is subsequently covered by a second seed-layer by evaporation of Al (Fig. 5.2 step 6). The resulting graphene presents no significant increase in the Raman D-peak nor does it exhibit any suspiciously low conductance.

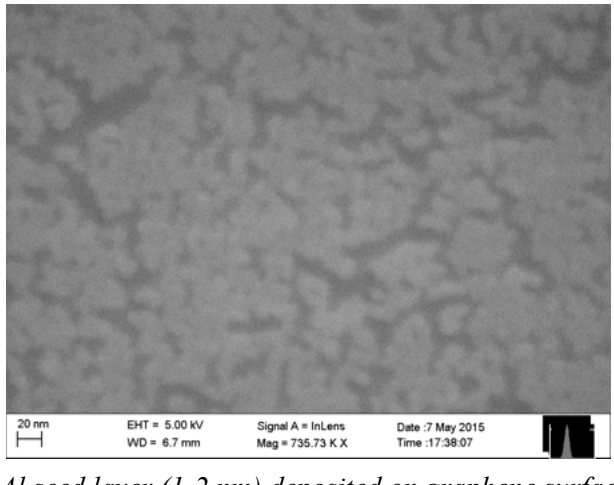

Figure 5.3.1 Al seed layer (1-2 nm) deposited on graphene surface by means of evaporation

5.4 Sputtering

Sputtering is today one of the most widely used thin film deposition methods due to its high rate and high scalability. It can be used for most metal based materials, e.g. metals, alloys and oxides. By applying a negative bias on the depositing metal (the target), energetic ions bombard the target and dislodge the target atoms. These atoms will then traverse the chamber and arrive at the substrate surface. By design, it is one of the most appropriate methods for thin film deposition in a roll-to-roll production as it can be placed above the substrate. As already shown in Fig. 5.1, sputtering is the technique that ranges across the energetic barrier which results in destruction of the graphene crystal. It would therefore be wise to strive for depositions that are in the low energy regime. However, this is not always possible. It has been known for a long time that the quality of a sputter deposited film is closely related to the processing pressure and substrate temperature of the system. Usually, this is illustrated by the Thornton diagram (Fig. 5.4.1)[87] which distinguishes between several zones of film morphology. The diagram illustrates different types of film growth depending on the substrate temperature relative to the melting point of the deposited material, as well as the pressure of the system. Many of the desired metals have melting points higher than 1000 ^{o}C, e.g. Au (1064 ^{o}C), Cu (1084 ^{o}C) and Ti (1668 ^{o}C). However, we found in **paper V** that an elevated substrate temperature promoted surface diffusion. The deposited metals agglomerated at the defect sites leaving the unharmed graphene exposed to further impact from sputter deposited material and energetic species.[88, 89] Such impact, possibly in combination with the added energy from the elevated temperature, resulted in damaged graphene. This shows that the graphene can become what limits the deposition temperature. Then in the Thornton diagram only zone 1 and T might be available, where the growth results in fibrous grains parallel to the inflow. In zone 1 the grains are linear whereas they are V-shaped in the T zone.[90]

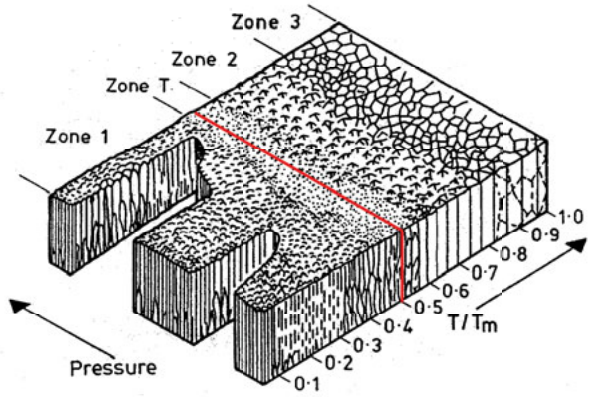

Figure 5.4.1 Thornton diagram with T/Tm = 0.5 marked with a red line. Reprinted with permission from [87]

It was this need to identify the boundaries of sputter deposition and the lack of an empirical confirmation on the level of allowed kinetic energy that prompted **paper IV.** By studying the influence of Ar bombardment at different kinetic impact energies and evaluating with Raman, the break down point for graphene could be estimated. In Fig. 5.4.2 b), the effect of ion bombardment dose on the defect-to-defect distance is visualized, showing a breaking point at ~26 eV.[91] In Fig. 5.4.2 the damage per dose at different nominal kinetic energies is displayed

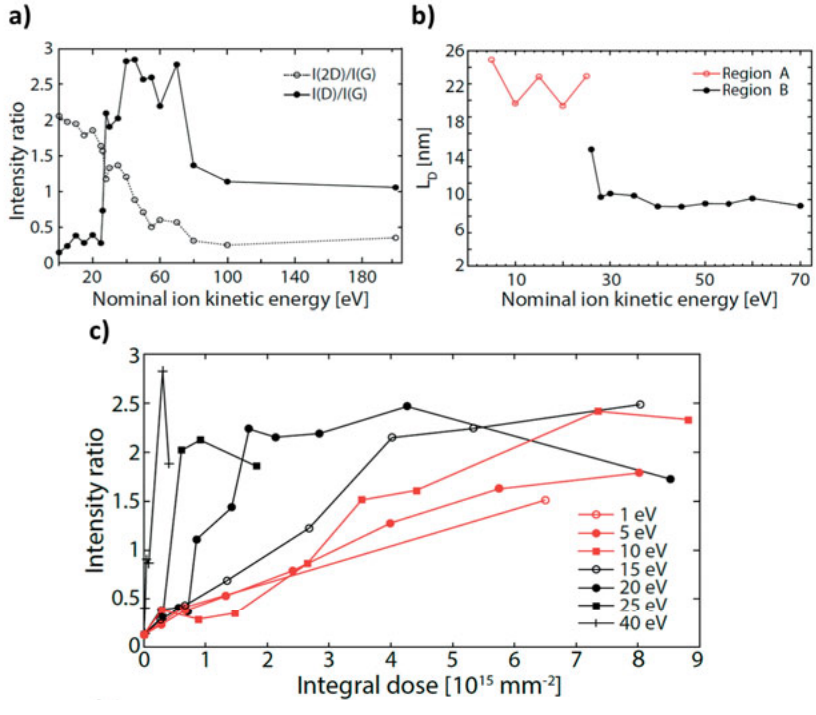

Figure 5.4.2 a) I(2D)/I(G) and I(D)/I(G) vs. nominal kinetic energy (eV) of exposure to ion bombardment b) corresponding defect-to-defect distance calculated in accordance to Eq. 4.1.1 c) I(D)/I(G) vs. the integral dose bombardment for different nominal kinetic energies.

A further challenge when employing sputter deposition on graphene arises when the desired film is an oxide. The reactive nature between C and O is the origin of this challenging problem. A direct solution is of course to sputter first and then do the transfer, an approach that has been previously adopted.[92] However, it might not always be feasible to complete all the sputter depositions needed before graphene is transferred. In **paper V,** the chemical effects of O present in a sputtering chamber was investigated. It was already known from literature that atomic O would be reactive with respect to graphene.[93] The situation was evaluated in our work by sputtering from both

an oxide target (Fig. 5.4.3, a) and from a metal target in a reactive atmosphere (Fig. 5.4.3, b) as opposed to just an alloy sputter deposition (Fig.5.4.3 c). As is apparent from the increased D peak, vanished 2D peak and broadening of the D and G peaks the lattice in graphene has been disrupted. Likely due to oxidization, to an unacceptable level when O is present in the sputtering process.

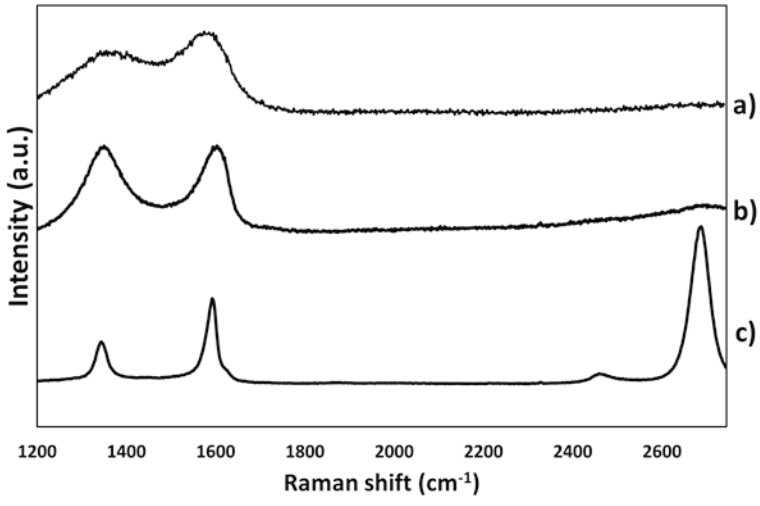

Figure 5.4.3 The effect of sputtering onto graphene from: a) an IGZO target b) a ZnSn target with 10 sccm O_2 flowing through the chamber (c) a ZnSn target in Ar atmosphere.

5.5 Macro deposition

With macro deposition, it is intended to cover deposition methods where the thin film is not introduced atom by atom or molecule by molecule. Examples of these are spraying, inkjet printing, screen printing and blade coating. In this work, studies have been concentrated around the subject of Galinstan, a liquid alloy consisting of Ga, In and Sn. It is a liquid down to -19 ^{o}C while having an electrical resistivity of 0.43μΩm.[94] Due to this, Galinstan has been considered a promising material for interconnects in future flexible electronics. However, it has the drawback of being extremely reactive to almost all metals normally used in the industry thereby making it challenging to incorporate in most established systems. This prompted the research in **paper VI** of studying the protective effects of graphene when combined with Galinstan. Al is one of the most sensitive materials when interacting with Galinstan and is easily oxidized by the process. Therefore, the electrical resistance (Fig. 5.5.1 c) and the appearance of a thin film of sputter deposited Al were used to evaluate the effectiveness of different layers of graphene. It was found that for graphene to be an effective barrier against Galinstan

when it was drop-deposited, a minimum of 3 layers was needed (Fig. 5.5.1 a and b). When Galinstan was sprayed on the requirement was 4 layers or above. This probably comes from a combination of the spray deposition inducing defects in the top layers of graphene while several layers are needed for the micro-tears to be fully covered.

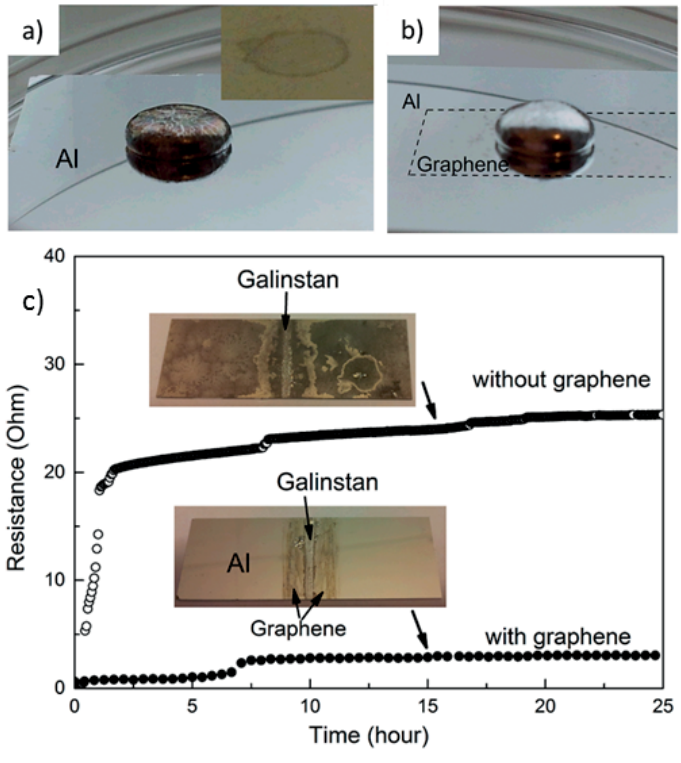

Figure 5.5.1 The effect of Galinstan on a) unprotected Al b) 3 layer graphene covered Al. c) The protective effect of graphene on Al from sprayed Galinstan, evaluated by the resistance.

The spray technique could be utilized in a lift-off process together with Galinstan in order to create micro sized interconnects. Acetone used during the PR removal step, will oxidize Galinstan edges thus resulting in well-defined structures. This technique holds promise for a future of unbreakable Galinstan interconnects supported by a graphene barrier (Fig. 5.5.2).

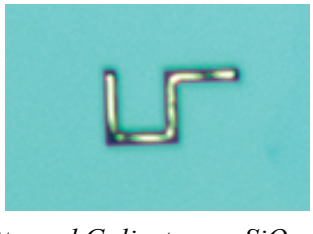

Figure 5.5.2 Lift-off patterned Galinstan on SiO_2. Structure is 85 µm wide.

6. Summary and outlook

I have in this work studied the impact from different thin film deposition methods on graphene. In order to do this a CVD method has been established and a novel way of graphene transfer has been developed. The deposition methods differ in many ways but can be divided by the kinetic impact energies they are associated with. It has been noted that these methods under a range of circumstances can affect the graphenes chemistry, physical state and electrical performance. The major findings from each paper in this thesis are summarized below:

Paper I. I developed a new clean, low temperature method for the transfer of CVD graphene from Cu-foil to the desired substrate. In this work we studied what impact different spacing's between Au-nanoparticles and graphene have on the SERS effect. Using the new clean method of transfer and comparing it to the old heat based technique the impact of residual PMMA on the graphene could be modelled with the SERS effect.

Paper II. I together with the group developed a method for G-FET production. The resulting electrical behavior is that of intrinsic graphene. I show that graphene processing can greatly benefit from the effect of an Al_2O_3 ALD step. The ALD process has a two-in-one effect where a topgate dielectric can be added while the channel is chemically cleaned by a gaseous Al-complex. This ALD cleaning is more efficient than to remove I_2 from the graphene in a separate process as most of the proposed approaches are time consuming.

Paper III. I investigate how the Al_2O_3 ALD can be steered through substrate manipulation to achieve different electrical behavior of the graphene. By altering the hydrophilicity of the SiO_2 surface it is here shown to introduce unipolar transfer conductivity in a G-FET. I find through thorough evaluations of the electrical characteristics that the suppressing behavior is most likely explained by bipolar ligands in the channel interface.

Paper IV. I show that it is very challenging to design a sputter process that does no damage to the graphene at all. By exposing graphene to different doses and energies of Ar ions, we have empirically investigated how graphene is affected by kinetic impact energies normally associated with sputter deposition. It is concluded that even at very low energy levels, at a sufficiently large dose of Ar ions, a sputter deposition can still result in amorphous graphene.

Paper V. It was concluded that it is not viable to deposit an oxide film on graphene through sputtering without causing damage to the graphene. O in atomic form is reactive enough to oxidize the graphene during the process. It is however possible to deposit metal thin films and perform thermal post-oxidation in order to achieve the desired oxide. This was proven for relatively thick films, i.e. 80 nm. When using sputter deposition it is most preferable to keep the substrate temperature as low as is feasible. This is to avoid surface diffusions that otherwise could increase the induced defect density.

Paper VI. I investigated the viability of using graphene as a diffusion barrier for a Ga-In-Sn alloy. I evaluated this barrier property by monitoring the resistivity of Al-films, either protected with graphene or not, exposed to the Ga-In-Sn. I concluded that when the purpose of utilizing a transferred graphene film as a chemical barrier it is important that at least 3 layers are stacked on top of each other. When using a spray deposition technique on the graphene film at least one more layer should be added.

It has not been published at the moment of print, but we have found that the substrate can be used to direct the deposition organic molecules through electrostatic interactions. A charged surface next to a neutral one can be used to differentiate between differently charged organic molecules.

It might sound as the sputter technique is not feasible in graphene processing. That is however not true, it just has a smaller window of operation parameters than it usually has. After the initial layer is fully covering the graphene the pressure can be decreased and higher quality of films can be deposited. The sputtering system can also be used even at the more degenerative settings. What we can see from the experiments concerning spray deposition is that at high impact energies 4xSLG can be sufficient to handle the impact of the deposited thin films, while retaining its chemical barrier properties. This will be of interest for fields such as the corrosion protection industry where large areas need to be covered with preferably hydrophobic surfaces. A multi stack of graphene could here be combined with low tear polymers that are sprayed on the graphene. Replacing the spraying with atomic deposition, e.g. sputtering would most likely lower the amount of layers needed to reach this effectiveness. However, a minimum of two layers will be needed until a breakthrough allowing for tear free transfer is introduced. With a MLG stack transferred onto a substrate it could be combined with doped ZnO or ITO to create highly conductive and transparent films with an effective humidity barrier. This could be the key to improve the use of organic semiconductors in several fields, e.g. screens and solar cells.

It is expected that the quality of transfer methods will continue to improve, especially if it is implemented into macro devices, e.g. packaging and screens. However it is questionable if the quality of the transfer can be good enough to be acceptable in the industrial application of nano devices. Recent developments suggest that graphene, despite its remarkable mobility, will not continue Moore's law due to the lack of a bandgap. My findings support

the already established roadmap that foresees the most likely implementation of graphene in the near future is in products that require micrometer sized structures and larger (Fig. 6.1). If transfer based production is to be realized, a workaround for the issue of micro tears needs to be proposed.

The effects in this work have been evaluated mostly on graphene supported by SiO_2. This has allowed a fair comparison between our work and others but it also mean that the findings here are not necessarily translated to other substrates. The implementation of flexible substrate in production could be financially beneficial and if done correctly environmentally friendly.

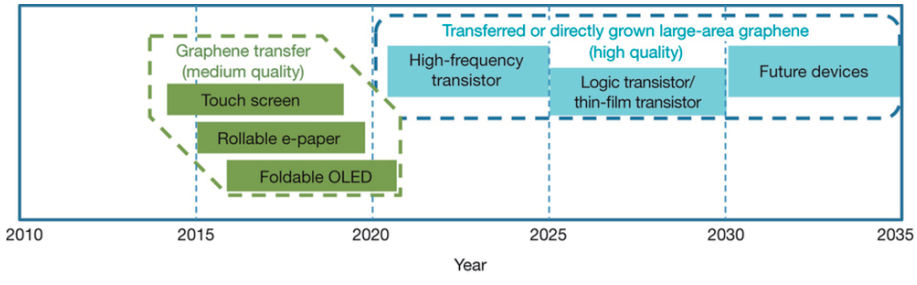

Figure 6.1 The CVD graphene evolution according to the roadmap, reprinted with permission from [18]

7. Svensk sammanfattning

I och med att A Geim och K Novoselov 2014 publicerade deras upptäckt av att grafen, ett atomärt mono-lager av grafit, kan tillverkas från grafit initierades ett helt nytt fält inom C-elektroniken. Detta kom passande nog i samband med att flera aktörer söker efter alternativa användningsområden för de process tekniker som utvecklats för processorindustrin. Idag eftersöks det sätt att implementera dessa tekniker på ett sätt som kan leverera billiga lösningar inom allt från paketering till solceller. Det är i den här övergången som grafenet har potential att spela en nyckelroll. Det är denna efterfrågan på att anpassa redan etablerade processtekniker till grafen som motiverade denna avhandling. Fokus ligger på vilken effekt olika beläggningsmetoder har på ytskiktet och i förlängningen grafenets egna prestanda. Metoderna har utvärderats optiskt med Raman såväl som elektriskt genom att studera grafenets halvledande egenskaper. Grafenet har tillverkats lokalt med kemisk ångdeponering (chemical vapor deposition, CVD). CVD metoden har i dagsläget blivit den populäraste metoden för att kunna arbeta med större ytor av grafen, i storleksordningen cm^2 och uppåt.

Som ett led i utvecklingen etablerades en ny metod för att transportera grafen från den Cu-folien som den syntetiserats på till ett valfritt substrat. Den rena vakuummetoden som beskrivs i **artikel I** ligger till grunden för de efterföljande artiklarna, undantaget **artikel II och VI**, och säkerställer att de utvärderingar som utförts här är representativa för grafen.

Beläggningsmetoderna spänner över ett stort spann av olika energi nivåer för kollisioner med grafenet, allt från 10^{-2} eV till över 10^3 eV. De lägre energierna är förknippade med rena diffusions mekanismer från atomer och molekyler som adsorberar på grafenets yta genom gaser och vätskor. De högre energierna är förknippade med sputtring och spraydeponering.

Molekylär gasdeponering, mera känt som “atomic layer deposition” (ALD) är inte bara en av de minst destruktiva metoderna för tunnfilms beläggning, i **artikel II** identifieras också en synergistisk effekt. Tack vare den höga reaktiviteten hos Al kunde ALD processen, när den var designad för Al_2O_3, användas för att rena grafenet från halogener.

De initiala problemen med sputtertekniken utvärderas i **artikel IV** där kollisionseffekten från Ar joner korrelerades med deras accelerationsspänning. Denna empiriska undersökning bekräftar den teoretiska bindningsbrytande energinivån som krävs för förstöra grafenets kristallinitet. Utöver detta blev slutsatsen att alla kinetiska kollisioner med grafen, givet tillräckligt hög

dos, kommer att resultera i mätbart skadat grafen oavsett med vilken energi jonen träffar ytan. Vidare visas i **artikel V** att närvaron av O i ett sputtersystem, oavsett dess form, resulterar i att grafenet blir oacceptabelt skadat. Anledningen är närvaron av atomärt O vilket är signifikant mer reaktivt och resulterar i ett fullständigt oxiderat grafen. I **artikel IV** utformas istället en postoxideringsmetod där grafenet beläggs med sputtering och sedan oxideras under kontrollerade former.

I **artikel VI** studeras hur uthålligt grafenet är när det utsätts för spraybeläggning av en flytande legering. Den studerade legeringen var en Ga-In-Sn blandning som är känt under märket Galinstan. Legeringen är flytande ner till -19 ^{o}C och har en ledningsförmåga som är jämförbar med Cu. Den har däremot det stora problemet av att diffundera in i fasta metaller och oxidera de till ett isolerande tillstånd. Dess låga smältpunkt gör materialet intressant att kombinera med grafenet som kan sträckas upp till 6% utan att brytas samtidigt som grafen är en välkänd kemisk barriär. Studien kom till slutsatsen att det krävs ett minimum av 4 lager av grafen för att effektivt hindra legeringen från att reagera med underliggande Al om det är deponerat genom sprejning. 3 lager är tillräckligt om deponeringen är droppvis.

Som slutsats kan det fastställas att grafenet har potentialen för ett antal användningsområden. Huvudsakligen ser man att de potentiella områdena är begränsade till större enheter. Detta överensstämmer med vad den officiella kartan för grafenets utveckling har stakat ut.

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