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Kilowatt-level power amplifier in a single-ended architecture at 352 MHz

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This paper demonstrates the feasibility and very good performance of a kilowatt-level power amplifier in a single-ended architecture, intended for energy systems. The prototype is designed at 352 MHz for the ESS LINAC and delivers up to 1250 W with 71% efficiency in pulsed operation with a duty cycle of 5%, 3.5 ms pulse at 14 Hz repetition.

Introduction: Solid-state r.f. high power amplifiers (PA) are increasingly used as energy systems in particle accelerators, such as cyclotrons and LINACs, in a large variety of applications, including radionuclide production, particle therapy for cancer treatment, and synchrotron light sources for scientific studies [1-2]. The design of solid-state PA for energy systems calls for a different approach than the design of PA for data transmission, where linearization is paramount. PA as energy systems could be operated in saturation and therefore be more efficient, while delivering more output power [3]. A direct implication is the reduction of the number of amplifier modules, as relatively more power, more efficiently could be delivered per module.

It remains unclear whether a simple architecture could be adopted at the kilowatt-level. In order to improve the competitiveness of solid state based energy systems, a simple architecture could drastically reduce the manufacturing costs, as a high number of modules need to be combined.

The purpose of this letter is to demonstrate by simulations and experimentation, the feasibility and performance of a single-ended power amplifier at kilowatt-level, realized in a planar printed circuit board technology and avoiding using complex circuits, such as baluns, as is presently customary at these high power levels [4].

Design considerations: At the FREIA laboratory, Uppsala University, Sweden we develop and test pulsed power amplifiers at 352 MHz. The frequency and pulsed operation (3.5 ms pulse at 14 Hz repetition) correspond to the specifications of the European Spallation Source (ESS), which we assist in its development and testing [5]. For the amplifier design, the source and load impedances were obtained using load-pull and source-pull simulations with the transistor's large signal model. The BLF188XR LDMOS was used, as it delivers high power with high efficiency and has excellent ruggedness capabilities [6]. For the optimal power added efficiency (PAE) with drain voltage, VDD = 50 V, gate voltage, V bias = 1.6 V and output power, P load = 1.3 kW, the simulated input impedance and load impedance are typically $Z_I = 0.36 - j0.72\Omega$ and $Z_L = 0.35 + j0.37\Omega$. Note that these impedances are roughly four times smaller than for the push-pull amplifier. The r.f. design implements matching networks in a single-ended architecture and avoids the use of baluns. The 50 Ohm input and output impedances are transformed to match the transistor's impedances using wide stepped striplines and are fine-tuned using SMD capacitors. DC feed at the drain is realised by connecting the supply voltage via a thick wire air coil and it is using a 100 Ohm SMD resistor (R_I) for biasing at the gate, to avoid mutual coupling if using a second RF choke at the gate. Capacitors C_1, C_2, C_3 and C_{13}, C_{14}, C_{15} are 560 pF and are used as DC blocks, and similarly C_7 and C_8, of the same value, are used to ground for r.f. the DC biasing, see Fig. 1. The input and output circuits use a two steps microstrip line transformer. The matching capacitor close to the drain, of optimal value 27 pF was split in three parallel capacitors C_{10}, C_{11} and C_{12} to lower the heat dissipation per capacitor. The circuit can be slightly tuned for different output power and efficiency, by decreasing the value and position of the capacitors at the output circuit, a higher output power and a lower efficiency is obtained. A similar tuning, i.e. increasing the value of C_4 and C_5 at the input side is reducing the return loss. The detailed dimensions are as follows: $G_I = 2$ mm, $W_I = W_6 = 3$ mm, $W_2 = 15$ mm, $W_3 = W_4 = 26$ mm, $W_5 = 34$ mm and $L_I = L_7 = 5$ mm, $L_2 = 42$ mm, $L_3 = 8.5$ mm, $L_4 = 12$ mm, $L_5 = 66$ mm, $L_6 = 36.5$ mm.
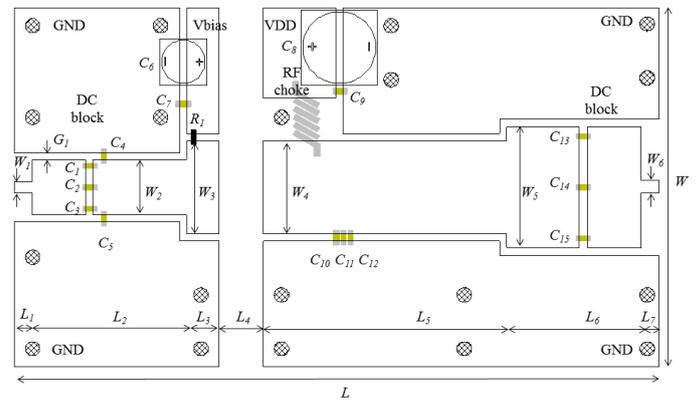

Fig. 1 *Circuit layout.*

The validation of the r.f. design is realized using the ADS software, Harmonic Balance (HB) simulations combined with simulations of the final layout of the matching networks using the method of moments, in combination with NXP's transistor model. In addition, a number of ports are implemented and used to connect the decoupling capacitors, BLF188XR transistor and DC biasing networks. The simulated output power is about 1.3 kW at around 1 dB in compression from a maximum gain of 20.5 dB, with 70% PAE, see Fig. 2.
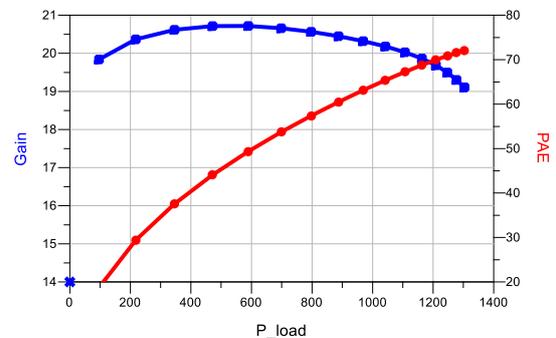

Fig. 2: *Harmonic Balance simulations of Gain and Efficency.*

Prototype and measurements: The matching networks are realised on a Rogers RO3003 substrate with $\varepsilon_r = 3$, $tan\delta = 0.001$, copper thickness is 35 μm and substrate thickness is 0.76 mm. All r.f. capacitors from American Technical Ceramics type 800B are best suited for high power use. In order to provide a stable bias condition, two electrolytic capacitors $C_6 = 47$ μF and $C_8 = 470$ μF bypass the DC circuit. Drain bias is supplied via a 6 turns enamelled copper choke inductor (1 mm diameter, 10 mm external diameter and 10 mm long), connected to the drain. The aluminium baseplate is provided with a cooling tube of 10 mm in diameter, located 10 mm under the flange of the transistor. The overall dimensions are: $W = 100$ mm and $L = 175$ mm, see Fig. 3.
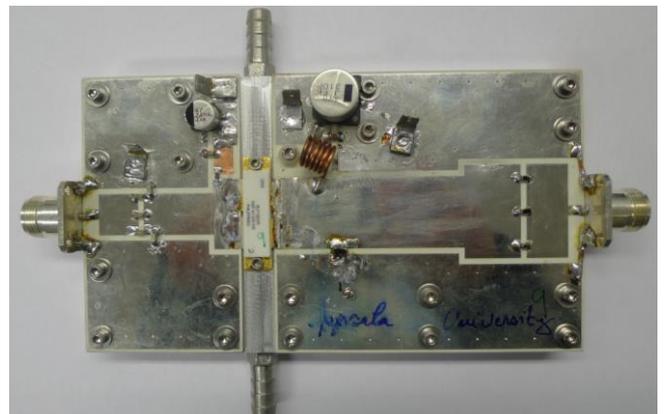

Fig. 3: *Realised single-ended power amplifier prototype at 352 MHz.*

A dedicated measurement set-up is implemented, see Fig. 4. The set-up is composed of two high power bi-directional couplers with 50 dB coupling level, allowing measuring input and output power as well as the return loss. Power measurements are performed with a N1912A pulsed power meter. A signal generator supplies a nominal – 10 dBm input power. A 50 W pre-amplifier, (50 dB gain) feeds the DUT i.e. the prototype amplifier. The harmonic signals are monitored with a spectrum analyser, harmonics are all below − 25 dBc.
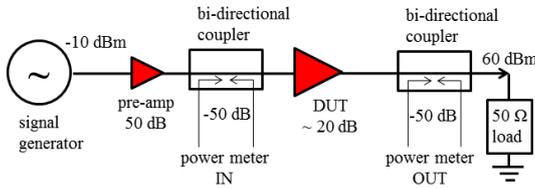

Fig. 4: *Measurement setup.*

Results and discussion: Measurements in pulsed mode, performed using ESS' conditions with a duty cycle of 5%, a pulse duration of 3.5 ms at 14 Hz demonstrate that the amplifier is capable of producing 1250 W output power at 1 dB gain compression, from a maximum gain of 20 dB with a measured efficiency of 71%, as shown in Fig. 5.
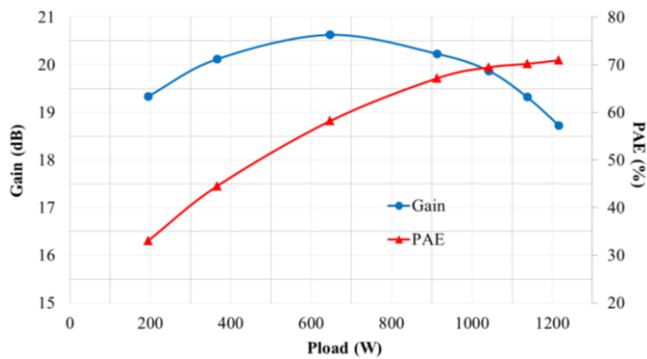

Fig. 5: *Measurements of Gain and Efficiency in pulsed mode (duty cycle = 5%, 3.5 ms pulse at 14 Hz repetition).*

In this mode, the thermal effects are attenuated due to the larger time between pulses, allowing the amplifier to cool down. The temperature rises for only few degrees, to about 30^0C (20^0C room temperature), while it is close to 150^0C in CW, see the thermal images in Fig. 6. During the r.f. measurements, a water debit of about 8 l/min is maintained in a water cooling pipe, with a diameter of 10 mm, across the heat-sink, located at 10 mm under the flange of the transistor.
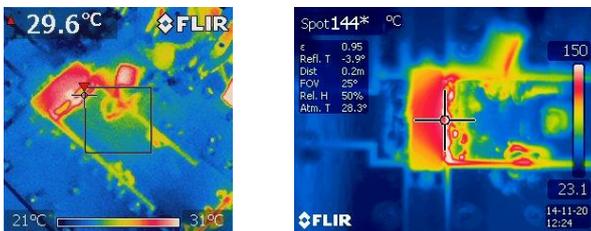

Fig. 6: *Thermal images during the r.f. measurements using water cooling with a debit about 8 l/min: left, in pulsed mode (duty cycle = 5%), at 1.25 kW and right, in CW, at 1 kW.*

During CW measurements, in order to obtain around 1 kW output power, the gain is compresses by 2.5 dB and the efficiency drops to about 61%, see Fig. 7. The high decrease in gain and efficiency is essentially due to thermal effects with a hot spot of 144ºC measured on the leads of transistor, see Fig. 6. Actually, both an excellent thermal contact to the cooling plate and a heat conducting compound between the transistor and the cooling plate are necessary. The cavity in the cooling plate should exactly fit the size of the transistor flange and in

the prototype amplifier it is presently 12 mm, while it should be 10 mm [7]. It results in a lack of cooling at the transistor leads, which are in air for a length of about 1 mm on both sides, strongly affecting the r.f. performance.
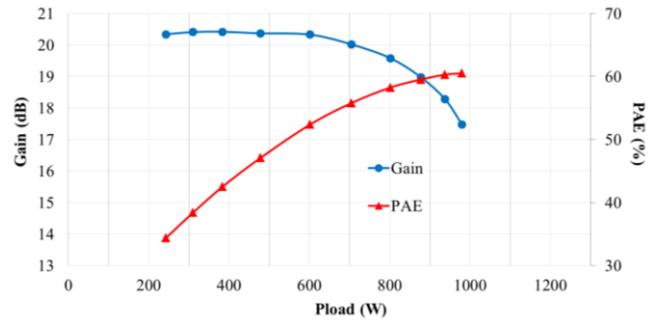

Fig. 7: *Measurements of Gain and Efficiency in CW mode.*

Conclusion: The single-ended architecture adopted for the high power r.f. amplifier allows achieving kilowatt-level output power with a very good efficiency, similar to the push-pull design [8]. The prototype at 352 MHz produces 1250 W with an efficiency of 71%, in pulsed operation while in CW, the efficiency drops to 61%, which is due to thermal effects. This single-ended architecture opens-up new perspectives towards kilowatt-level power amplifiers with a similar efficiency and output power, without requiring more complex circuits structures, such as baluns.

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