UPPSALA
UNIVERSITET

Digital Comprehensive Summaries of Uppsala Dissertations from the Faculty of Science and Technology 1794

Silicon Nanowire Field-Effect Devices as Low-Noise Sensors

XI CHEN

ACTA
UNIVERSITATIS
UPSALIENSIS
UPPSALA
2019

ISSN 1651-6214
ISBN 978-91-513-0625-4
urn:nbn:se:uu:diva-381049

Dissertation presented at Uppsala University to be publicly examined in Polhemsalen, Ångströmlaboratoriet, Lägerhyddsvägen 1, Uppsala, Monday, 27 May 2019 at 09:00 for the degree of Doctor of Philosophy. The examination will be conducted in English. Faculty examiner: Associate professor Fengnian Xia (Yale University).

Abstract

Chen, X. 2019. Silicon Nanowire Field-Effect Devices as Low-Noise Sensors. *Digital Comprehensive Summaries of Uppsala Dissertations from the Faculty of Science and Technology* 1794. 69 pp. Uppsala: Acta Universitatis Upsaliensis. ISBN 978-91-513-0625-4.

In the past decades, silicon nanowire field-effect transistors (SiNWFETs) have been explored for label-free, highly sensitive, and real-time detections of chemical and biological species. The SiNWFETs are anticipated for sensing analyte at ultralow concentrations, even at single-molecule level, owing to their significantly improved charge sensitivity over large-area FETs. In a SiNWFET sensor, a change in electrical potential associated with biomolecular interactions in close proximity to the SiNW gate terminal can effectively control the underlying channel and modulate the drain-to-source current (I_{DS}) of the SiNWFET. A readout signal is therefore generated. This signal is primarily determined by the surface properties of the sensing layer on the gate terminal, with sensitivity close up to the Nernstian limit widely demonstrated. To achieve a high signal-to-noise ratio (SNR), it is essential for the SiNWFETs to possess low noise of which intrinsic device noise is one of the major components. In metal-oxide-semiconductor (MOS)-type FETs, the intrinsic noise mainly results from carrier trapping/detrapping at the gate oxide/semiconductor interface and it is inversely proportional to the device area.

This thesis presents a comprehensive study on design, fabrication, and noise reduction of SiNWFET-based sensors on silicon-on-oxide (SOI) substrate. A novel Schottky junction gated SiNWFET (SJGFET) is designed and experimentally demonstrated for low noise applications. Firstly, a robust process employing photo- and electron-beam mixed-lithography was developed to reliably produce sub-10 nm SiNW structures for SiNWFET fabrication. For a proof-of-concept demonstration, MOS-type SiNWFET sensors were fabricated and applied for multiplexed ion detection using ionophore-doped mixed-matrix membranes as sensing layers. To address the fundamental noise issue of the MOS-type SiNWFETs, SJGFETs were fabricated with a Schottky (PtSi/silicon) junction gate on the top surface of the SiNW channel, replacing the noisy gate oxide/silicon interface in the MOS-type SiNWFETs. The resultant SJGFETs exhibited a close-to-ideal gate coupling efficiency (60 mV/dec) and significantly reduced device noise compared to reference MOS-type SiNWFETs. Further optimization was performed by implementing a three-dimensional Schottky junction gate wrapping both top surface and two sidewalls of the SiNW channel. The tri-gate SJGFETs with optimized geometry exhibited significantly enhanced electrostatic control over the channel, thereby confined I_{DS} in the SiNW bulk, which greatly improved the device noise immunity to the traps at bottom buried oxide/silicon interface. Finally, a lateral bipolar junction transistor (LBJT) was also designed and fabricated on a SOI substrate aiming for immediate sensor current amplification. Integrating SJGFETs with LBJTs is expected to significantly suppress environmental interference and improve the overall SNR especially under low sensor current situations.

Keywords: Silicon nanowire, field-effect transistor, Schottky junction gate, low frequency noise, ion sensor

Xi Chen, Department of Engineering Sciences, Solid State Electronics, Box 534, Uppsala University, SE-75121 Uppsala, Sweden.

ISSN 1651-6214
ISBN 978-91-513-0625-4
urn:nbn:se:uu:diva-381049 (http://urn.kb.se/resolve?urn=urn:nbn:se:uu:diva-381049)

List of Papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I. **Chen X.**, Zhang T., Constantoudis V., Zhang S.-L., Zhang Z., Aged Hydrogen Silsesquioxane for Sub-10 nm Line Patterns, *Microelectronic Engineering*, 163 (2016) 105-109

II. **Chen X.***, Hu Q.*, Chen S., Netzer N. L., Wang Z., Zhang S.-L., Zhang Z., Multiplexed Analysis of Molecular and Elemental Ions Using Nanowire Transistor Sensors, *Sensor and Actuator B*, 270 (2018) 89-96

III. **Chen X.**, Chen S., Hu Q., Zhang S.-L., Solomon P. M., Zhang Z., Device Noise Reduction for Silicon Nanowire Field-Effect-Transistor Based Sensors by Using a Schottky Junction Gate, *ACS sensors*, 2019, 4 (2), pp 427–433

IV. **Chen X.**, Chen S., Zhang S.-L., Solomon P. M., Zhang Z., Low Noise Schottky Junction Tri-gate Silicon Nanowire Field-Effect Transistor for Charge Sensing, submitted to *IEEE Transactions on Electron Devices*

V. **Chen X.**, Chen S., Solomon P. M., Zhang Z., Top-Bottom Gate Coupling Effect on Low Frequency Noise in A Schottky Junction Gated Silicon Nanowire Field-Effect Transistor, submitted to *IEEE Electron Device Letters*

VI. Hu Q.*, **Chen X.***, Norström H., Zeng S., Liu Y., Gustavsson F., Zhang S.-L., Chen S., Zhang Z., Current Gain and Low-Frequency Noise of Symmetric Lateral Bipolar Junction Transistors on SOI, *ESSDERC 2018*

*The authors contributed equally to the work. Reprints were made with permission from the respective publishers.

Author's Contributions

I. Planned and performed all the experimental work, took part in discussions and wrote the manuscript.

II. Planned and performed part of the experimental work, took part in all discussions and wrote the manuscript.

III. Planned and performed most of the experimental work except the TEM measurement, took part in discussions and wrote the manuscript.

IV. Planned and performed most of the experimental work except the TEM measurement, took part in discussions and wrote the manuscript.

V. Planned and performed all the experimental work, performed part of the simulations, took part in discussions and wrote the manuscript.

VI. Planned and performed part of the experimental work for fabrications, performed the LFN measurements, took part in discussions and wrote part of the manuscript.

Related work not included in the thesis:

I. Zeng S., Wen C., Li S., **Chen X.**, Chen S., Zhang S.-L., Zhang Z., Controlled Size Reduction and Its Underlying Mechanism to Form Solid-State Nanopores via Electron Beam Induced Carbon Deposition, submitted to *Journal of Membrane Science*

II. Tseng C-W., Wen C., Huang D-C., Lai C-H., Chen S., Hu Q., **Chen X.**, Xu X., Tao Y-T, Zhang S.-L., and Zhang Z., Synergy of Ionic and Dipolar Effects by Molecular Design for pH Sensing Beyond The Nernstian Limit, submitted to *Advanced Materials*

Contents

Abbreviations

A	Gate area	μm^2
A^*	The effective Richardson constant	$A/cm^2\text{-}K^2$
C_d	Differential capacitance	F/cm^2
C_{cable}	Cable parasitic capacitance	F/cm^2
C_D	Depletion layer capacitance	F/cm^2
C_{in}	Input parasitic capacitance	F/cm^2
C_{it}	Interface trap capacitance	F/cm^2
C_{out}	Output parasitic capacitance	F/cm^2
C_{ox}	Oxide capacitance	F/cm^2
C_{sub}	Substrate capacitance	F/cm^2
E_C	Bottom edge of conduction band	eV
E_F	Femi level	eV
f	Frequency	Hz
$f_{roll\text{-}off}$	Roll-off frequency	Hz
g_m	Transconductance	S
G_{VAMP}	Gain of the voltage amplifier	
$\overline{i_{TB}^2}$	Total base noise current	A^2
I_B	Base current	A
I_{DS}	Drain-to-source current	A
I_{GS}	Gate current	A
$I_{on(off)}$	On(off) current	A
k	Boltzmann's constant	J/K
L_G	Gate length	m
n^+	Heavily *n*-doped	cm^{-3}
N_A	Acceptor-impurity concentration	cm^{-3}
N_D	Donor-impurity concentration	cm^{-3}
N_s	Density of surface site	cm^{-2}
N_t	Volume trap density	cm^{-3}
$N_{V\ meas}$	Voltage fluctuations after amplification	$V/Hz^{1/2}$
q	Electronic charge	1.6×10^{-19} C
r_{in}	Input resistance	Ω
r_{out}	Output resistance	Ω
R_{in}	Input resistance	Ω
R_{load}	Load resistance	Ω
S_{ib}	Current noise PSD, bottom interface	A^2/Hz

S_{ibase}	Current noise PSD, base	A^2/Hz
S_{ibulk}	Current noise PSD, SiNW bulk	A^2/Hz
S_{id}	Drain current noise PSD	A^2/Hz
S_{it}	Current noise PSD, top interface	A^2/Hz
SS	Subthreshold slope	mV/decade
S_{vfb}	S_{vg} at flat-band condition	V^2/Hz
S_{vg}	Gate referred input voltage noise	V^2/Hz
t	Time	s
T	Kelvin temperature	K
t_{si}	Channel thickness	m
V_{bi}	Built-in potential	V
V_{CE}	Collector-to-emitter voltage	V
V_{DS}	Drain-to-source voltage	V
V_G	Gate voltage	V
V_{RE}	Reference gate voltage	V
V_{sub}	Substrate voltage	V
$\overline{v_T^2}$	Total noise voltage	V^2
V_{TH}	Threshold voltage	V
W_B	Base width	m
α	Activity	mol/L
α_{sc}	Coulumb scattering coefficient	V-s/C
α_t	Tunneling coefficient of electron	cm^{-1}
β	Current gain	
β_{int}	Intrinsic buffer capacity	cm^{-2}
ε_{Si}	Relative permittivity of silicon	F/cm
Φ_B	Schottky junction barrier height	eV
σ_s	Surface charge density	C/cm^3
μ_{eff}	Effective mobility	$cm^2/V\text{-}s$
φ_s	Surface potential	V
γ	Frequency exponent	
3D	Three-dimensional	
ALD	Atomic layer deposition	
As	Arsenic	
B	Base	
BOX	Buried oxide	
CMOS	Complementary metal-oxide-semiconductor	
DC	Direct current	
DeMOSFET	Depletion-mode MOSFET	
DI	Deionized water	
EBL	Electron beam lithography	
E/C	Emitter/collector	
EDL	Electrical double layer	
EDX	Energy dispersive spectroscopy	

FGA	Forming gas annealing
GC-MS	Gas chromatography-mass spectrometry
HF	Hydrofluoric acid
HPLC	High-performance liquid chromatography
HSQ	Hydrogen silsesquioxane
InMOSFET	Inversion-mode MOSFET
IPA	Isopropyl alcohol
ISE	Ion-selective electrode
ISFET	Ion selective field-effect transistor
JFET	Junction field-effect transistor
LBJT	Lateral bipolar junction transistor
LER	Line edge roughness
LFN	Low frequency noise
MB	Methylene blue
MMM	Mixed-matrix membrane
MOSC	Metal-organic supercontainer
MOSFET	Metal-oxide-semiconductor field-effect transistor
NaCl	Sodium chloride
PDMS	Polydimethylsiloxane
PEG	polyethylene glycol
PMMA	Poly(methyl methacrylate)
PSD	Power spectral density
PtSi	Platinum silicide
PVC	Poly(vinylchloride)
rpm	Revolutions per minute
RE	Reference electrode
RIE	Reactive ion etching
RTP	Rapid thermal processing
S/D	Source and drain terminals
SAM	Self-assembled monolayer
SEM	Scanning electron microscope
SiNWFET	Silicon nanowire field-effect transistor
SNR	Signal-to-noise ratio
SOI	Silicon-on-insulator
THF	Tetrahydrofuran
TVSEM	Top-view scanning electron microscopy
VAMP	Voltage amplifier
VBJT	Vertical bipolar junction transistor
XTEM	Cross-sectional transmission electron microscopy

1. Introduction and Theoretical Background

This thesis presents a study of the field-effect transistor as a compact biosensor operating in liquid. As such, the research goes across several scientific disciplines and touches upon potential applications much beyond the traditional microelectronics domain. Therefore, this chapter attempts to provide background information regarding the societal needs and prospects of this interdisciplinary topic, along with the scientific and technological requirements for a nanoscale electronic biosensor to deliver the desired functions.

1.1. Emergence of electronic biosensors

Early disease diagnosis is of paramount importance along with the development of therapeutic strategies [1], [2]. Many diseases, such as Alzheimer's and breast cancer, could be palliated greatly or even be cured by early intervention if they can be diagnosed at an early stage. Therefore, demands on more frequent and accurate diagnoses have been increasing dramatically. Nowadays, medical infrastructures are highly centralized. Diagnostic testing is mainly conducted in laboratories equipped with large and complex instruments which typically require highly skilled personnel to operate. Consequently, patients will expect great financial burden, long waiting time for their hospital visits and increasing possibility of missing the optimum window for their medical treatments. To meet such challenges, it is essential to develop portable and low-cost sensors which can rapidly detect important biomarkers at low concentrations [3]. Such sensors can be used in diversified places such as community hospitals, doctor’s office, or even at home. They may also be very useful in developing countries or remote fields where access to medical personnel and instruments are restricted [4]–[6].

Common analytical targets for medical assays can be ions, nucleic acids, proteins, metabolites, and pathogens. Figure 1.1 shows a brief summary of techniques for detecting proteins, including the ones that are still under development and not in clinical use [7]. Among them, electronic sensors have attracted great attention for their potential advantages such as small size and weight, fast response, high reliability, and possibility of on-chip integration together with a signal processing scheme with prospect of low-cost mass production [8]. As an example, a flexible and fully integrated sensor array capable of multiplexed *in situ* perspiration analysis is shown in Figure 1.2.

The sensor array can simultaneously and selectively measure sweat metabolites (such as glucose and lactate) and electrolytes (such as sodium and potassium ions), as well as the skin temperature [9]. In the array, each sensor is based on an ion-selective electrode (ISE) where the electrode surface is functionalized with receptors that can interact with different targets selectively.

Table 1 | Detection of protein biomolecules

Tool or technique	Read-out	Illustration	Detection limit*	Molecules per drop (60 µl)	In clinical use
Colorimetry	Visual		150 pM	10^9	Yes
Carbon nanotubes	Electrical		100 pM	10^9	No
Chemi-luminescence	Luminescence		30 pM	10^9	Yes
ELISA	Luminescence		1–10 pM	10^7	Yes
Quantum dots	Fluorescence		500 fM	10^7	No
Silicon nanowires	Electrical		1 fM	10^4	No
Metal nano-particles (bio-barcode)	Scanometric and/or light scattering		30 aM	900	Yes
Immuno-PCR	Fluorescence		20 aM	700	Yes

*Detection limits are best-case examples from the literature and can vary substantially depending on the target and the assay conditions.

Figure 1.1. Assays for detection of protein biomolecules. Reprinted with permission from [7]. *Copyright (2009) Springer Nature.*

Detection of low-concentration targets requires highly sensitive sensors while the lower detection limit of traditional ISEs is normally at µM level [10]. Here, another type of electronic sensor, *i.e.*, ion-sensitive field-effect transistor (ISFET), comes to light. First demonstrated about 50 years ago and lately developed into nanoscale, the ISFET represents a very competitive group of label-free electronic sensors [11]–[13]. Benefiting from comple-

mentary metal-oxide-semiconductor (CMOS)-compatible fabrication process, ISFET-based H^+ sensors have been successfully implemented in a novel full electronic based genome sequencing platform developed by Ion Torrent [14]. As shown in Figure 1.3, each sequencing chip contains 13 M individually addressable ISFETs and integrated signal readout circuitry, together with microfluidics for small volume handling of sequencing reagents.

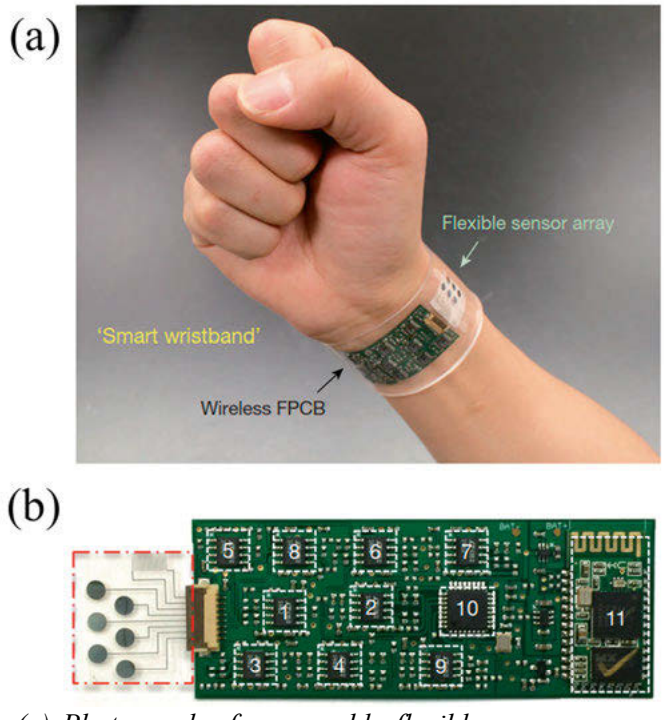

Figure 1.2. (a) Photograph of a wearable flexible sensor array on a subject's wrist, (b) photograph of a flattened flexible sensor array. The red dashed box indicates the sensor array and the white dashed boxes indicate the circuit components. Reprinted with permission from [9]. *Copyright (2016) Springer Nature.*

The charge sensitivity of ISFET can be greatly improved by downsizing its channel dimensions [15], [16] and detections of single molecular interactions have been demonstrated on ISFETs with silicon nanowire (SiNW) channel [17], [18]. In addition, based on the reaction-diffusion model [19], SiNW-sensors can also respond much faster than those with planar ISFETs due to simple geometrical effects with which 2D vs. 1D diffusion dictates in the respective case.

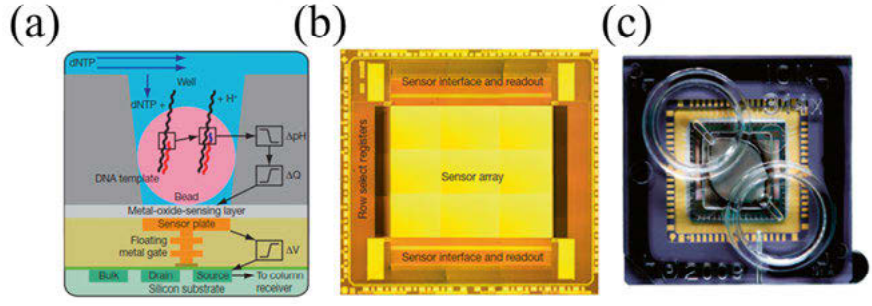

Figure 1.3. (a) Schematic showing the working principle for DNA sequencing using ISFET-based pH sensor, (b) unpackaged chip with functional regions indicated, and (c) wire-bonded chip in ceramic package, shown with fluidic lid to allow addition of sequencing reagents. Adapted with permission from [14].

1.2. Working principle of ISFETs

An ISFET is similar to a metal-oxide-semiconductor field-effect transistor (MOSFET), cf. Figure 1.4(a), with the gate metal replaced by an electrolyte, cf. Figure 1.4(b). The electrical potential of the electrolyte is defined by a reference electrode (normally a glass tube Ag/AgCl reference electrode). A sensing layer with analyte receptor is normally functionalized on the gate surface, which can selectively interact with targets of interest in the electrolyte. Such interaction can generate charge variations in close proximity to the channel, leading to a change in surface potential $\Delta\varphi_s$ and consequently a shift of the threshold voltage (ΔV_{TH}) of the ISFET. Provided the liquid gate potential is fixed by the reference electrode, the ΔV_{TH} is then transduced to a channel current change by the ISFET.

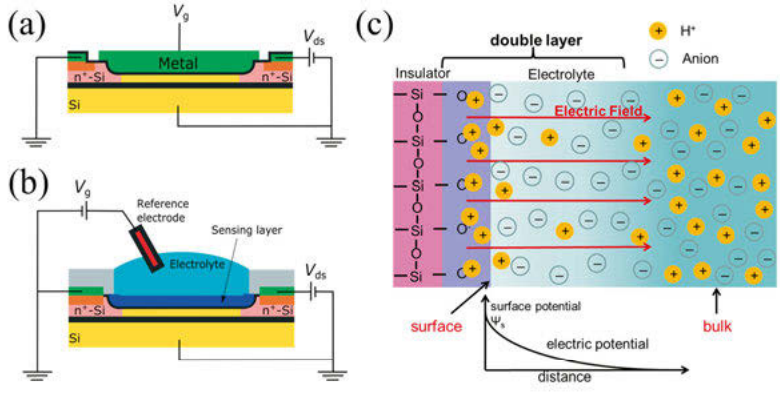

Figure 1.4. Schematic representations of (a) a MOSFET and (b) an ISFET. (c) Model for the EDL during the detection of H^+ with the potential distribution at the oxide/electrolyte interface.

In the case of ISFET *p*H sensor, the dependence of surface potential φ_s on the *p*H in the bulk electrolyte, *i.e.*, pH_B, can be well described by a site-binding model. As shown in Figure 1.4c, hydroxyl groups on the SiO_2 (gate insulator) surface will protonate or deprotonate when the SiO_2 is in contact with the electrolyte. The charge density (σ_s) and φ_s on the SiO_2 surface is determined by the density of surface site (N_s), the equilibrium constants of the hydroxyl group-H^+ interaction, pH_B, and the differential capacitance (C_d) of the electrical double layer (EDL). The dependence of φ_s on pH_B, *i.e.*, *p*H sensitivity of the ISFET, can be described by [20]:

$$\frac{\partial \varphi_s}{\partial pH_B} = -2.3\frac{kT}{q}\alpha, \text{ with } \alpha = \frac{1}{\left(\frac{2.3kTC_d}{q^2\beta_{int}}\right)+1} \tag{1.1}$$

where β_{int} is the intrinsic buffer capacity of the SiO_2 surface. It is evident from Eq (1.1) that the sensitivity upper limit, so called Nernstian limit, for ISFET is 59.2 mV/pH_B at room temperature and it can be reached for sensing oxide with high β_{int}. The Nernstian *p*H sensitivity of the ISFET can also be interpreted in a way similar to the ISE. The φ_s can be described by the Nernstian equation [10]

$$\varphi_s = \varphi_0 + 2.3\frac{kT}{q}\log_{10}^{[H^+]_B/[H^+]_S}, \tag{1.2}$$

where φ_0 is a constant, $[H^+]_B$ and $[H^+]_S$ are the H^+ concentrations in the bulk electrolyte and on the oxide surface, respectively. If the sensing oxide has large buffer capacity for H^+ so $[H^+]_S$ does not change when $[H^+]_B$ is varied, an ideal Nernstian sensitivity can be achieved. This model can also be applied to selective detections of other ions as long as the gate surface of the ISFET is functionalized with a sensing layer which can selectively bind to the ions of interest [21]–[23]. For example, in order to detect F^+ and Na^+ simultaneously, an array of ISFETs are coated with gold on the gate oxide, on which a self-assembled monolayer (SAM) of F^+-sensitive transition metal complex and Na^+-sensitive crown ether are immobilized as shown in Figure 1.5 [24]. Another approach to enable ion-selective detection could be to coat the gate surface of the ISFET with a polymer membrane doped with ionophores which have high binding affinity towards the target ions [25]. The ionophores can stabilize the concentration of the target ions in the membrane phase, similar to the function of the oxide surface of an ISFET *p*H sensor with large H^+ buffer capacity, leading to an ideal Nernstian sensitivity [10], [26]–[29].

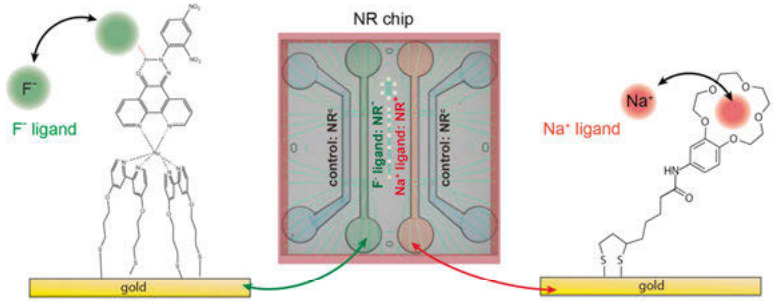

Figure 1.5. Schematics showing the molecular structures for the F^- ligand (Left) and the Na^+ ligand (Right) immobilized on the gold surface. Reprinted with permission from [24].

Extensive efforts have been devoted to optimizing the sensing surface and improving the sensitivity [30], with close to the Nernstian limit [31], 60 mV/dec (analyte concentration change) at room temperature widely reported in the literature [32]–[36]. In addition, higher charge sensitivity can be achieved by downscaling the planar ISFET to nano-ISFET, *e.g.* SiNW-ISFET [15], [30]. SiNWFETs with nanoscale channel have demonstrated excellent sensitivity for detecting large biomolecules due to its large surface-to-volume ratio and small capacitance and is a very promising platform for detecting low concentration, or even a single molecule event. However, the minimum signal which the ISFET can resolve depends on the fluctuations, *i.e.*, noise, of the ISFET itself. Sensors with lower noise can resolve smaller signal, thus enable detection of smaller changes in analyte concentration. Therefore the burden on sample preparation process, *e.g.*, sample enrichment, could be greatly reduced. Meanwhile, for detection of large biomolecules, the signal of the ISFET relies on the overlapping between the EDL and the biomolecules and can be very weak [37] due to the small thickness of the EDL, *i.e.*, less than 1 nm in typical physiological solutions, as illustrated in Figure 1.4(c).

1.3. Signal-to-noise ratio for ISFET-based sensors

For an ISFET sensor operating in electrolyte, the noise has mainly three components, *i.e.*, the bulk electrolyte noise, the solid-liquid interface noise, and the intrinsic noise of the ISFET. Previous studies have shown that the noise originating from the bulk electrolyte is negligible in comparison with that generated from the solid-liquid interface. Although direct assessment of the solid-liquid interface shows that its noise could be comparable or even higher than the noise of the state-of-the-art MOSFETs [38], the intrinsic

noise of the ISFETs in most reported work remains dominant when the ISFETs are operating in electrolyte.

The signal-to-noise ratio (SNR) of an ISFET-based sensor can be defined through

$$\mathrm{SNR} = \frac{\Delta\varphi_s}{\sqrt{\int_{f_L}^{f_H} S_{vg}\mathrm{d}f}}, \tag{1.3}$$

where S_{vg} is the power spectrum density (PSD) of the input-referred gate voltage noise of the ISFET. Integration of S_{vg} in the bandwidth (from a low frequency, f_L, to a high frequency, f_H) of the measurement gives the voltage fluctuation of the ISFET itself. $\Delta\varphi_s$ in Eq. 1.3 denotes the original signal of the ISFET, generated by changes in ion concentration with an upper limit of 59.2 mV/decade (change in concentration). $\Delta\varphi_s$ can also originate from the perturbation of the EDL by biomolecules in case of ISFET-based biosensors. It is evident from Eq. 1.3 that understanding and reducing S_{vg} of the ISFET-based sensors are of great importance.

1.4. Fundamentals of low frequency noise in MOSFETs

For ISFET-based sensors, low frequency noise (LFN) is most detrimental to the overall SNR as it can interfere with biomedical signals which span in the same frequency domain. LFN in MOSFETs has been an important research topic since the early days of semiconductor electronics. LFN minimization is a key issue in analogue applications as it determines the sensitivity or detection limit of the system. It has been well-established that the LFN in MOSFETs is dominated by flicker or 1/*f* noise [41], [42] which is characterized by a PSD (S_I for current noise or S_V for voltage noise) varying approximately according to $1/f^{\gamma}$, with the frequency exponent γ between 0.8 and 1.2 typically.

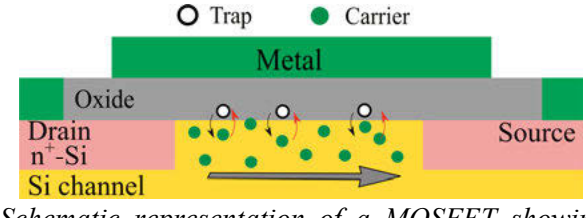

Figure 1.6. Schematic representation of a MOSFET showing the carrier trapping/detrapping process at the oxide/silicon interface.

There are mainly two theories to explain the physical origin of 1/*f* noise in MOSFETs. The number fluctuation model (Δn) ascribes the 1/*f* noise to fluctuations in the number of carriers due to random trapping and detrapping of

carriers to the traps in the vicinity of the interface between the gate oxide and the channel as illustrated in Figure 1.6, while the mobility fluctuation model ($\Delta\mu$) associates the 1/f noise to carrier mobility fluctuations due to Coulomb scattering near the interface. Although both Δn and $\Delta\mu$ theories predict a 1/f spectrum, S_{vg} of a MOSFET is independent of gate bias (V_G) according to the Δn theory while S_{vg} increases in strong inversion according to the $\Delta\mu$ theory. A unified model [43], [44] combining both Δn and $\Delta\mu$ theories have been developed, in which the S_{vg} of a MOSFET can be expressed as:

$$S_{vg} = S_{vfb}(1 + \alpha_{sc}\mu_{eff}C_{ox}\frac{I_{DS}}{g_m})^2, \tag{1.4}$$

where α_{sc} is the Coulumb scattering coefficient, μ_{eff} the effective mobility, C_{ox} the gate capacitance, and g_m the transconductance. S_{vfb} is S_{vg} at flat-band condition, given by:

$$S_{vfb} = \frac{q^2 kTN_t}{WLC_{ox}^2\alpha_t f}. \tag{1.5}$$

In Eq. (1.5), N_t is the volume trap density (cm^{-3}) in the gate oxide per eV, W and L are the device width and length, respectively, α_t is the tunneling coefficient of electrons in the gate oxide.

From Eqs. (1.4) and (1.5), it is evident that S_{vg}, which sets the minimum resolvable potential of an ISFET sensor, is strongly dependent on the trap density in the gate oxide particularly in the vicinity of the gate oxide/channel interface and is inversely proportional to the gate area of the device. Downscaling device dimensions aiming to increase the surface-to-volume ratio for achieving higher charge sensitivity will inevitably lead to a dramatic increase of intrinsic noise [41]. The noise issue is indeed becoming increasingly prominent as the detections have been pushed into extremely low concentration ranges, even targeting for single charge events [18].

Besides continuous improvement in the quality of gate oxide, efforts have been pursued to reduce LFN by, for example, using a depletion-mode MOSFET (DeMOSFET) [41], [45] where the conduction channel is pushed away from both top and bottom interfaces thereby distancing the conduction channel from both "noisy" interfaces. Minimum noise can be achieved on the DeMOSFET with a buried bulk conduction channel and/or with strong inversion at both interfaces in order to shield from the interfacial noise [41], [46]. However, it can be challenging to achieve such bias conditions without compromising transducing efficiency in practical sensor applications. Meanwhile, junction field-effect transistors (JFETs), employing a PN junction for channel current modulation, have been widely used in low noise amplifiers as the interface carrier trapping and detrapping have been elimi-

nated [47]. Due to the small dimensions of SiNW channel, implementing the JFET concept on SiNWFETs is challenging as it is difficult to achieve a precise control of a shallow PN gate junction on the channel.

1.5. Thesis organization

The main focus of this thesis is noise evaluation and reduction for SiNW-based ISFET sensors (SiNWFETs). The ultimate goal would be to develop low noise SiNWFETs capable of detecting electrical signals associated with discrete biomolecular binding events. The thesis is organized as follows. Chapter 2 describes the fabrication and characterization details of SiNWFETs. Chapter 3 introduces the work on sensing interface design towards multiplexed detection of molecular and elemental ions. Chapter 4 focuses on the development of low noise Schottky junction gated SiNWFETs. Chapter 5 proposes a possible mitigation solution for environmental noise by using lateral bipolar junction transistor (LBJT) as a local signal amplifier.

A brief summary of the papers included in this thesis is presented as follows. Firstly, a robust process employing photo- and electron-beam mixed-lithography was developed to reliably produce sub-10 nm SiNW structures for SiNWFET fabrication, which is summarized in **paper I**. **Paper II** presents a proof-of-concept sensing demonstration by using SiNWFET based sensors. It is applied for multiplexed ion detection using the ionophore-doped mixed-matrix membrane as the sensing layer. **Paper Ⅲ** addresses the fundamental noise issue of the SiNWFET sensor devices by designing a Schottky junction gated SiNWFETs (SJGFET), where the noisy gate oxide/silicon interface of the conventional SiNWFET is replaced by a Schottky junction gate (SJG) on the top surface of the SiNW channel. The resultant top-gate SJGFET exhibits close-to-ideal gate coupling efficiency and significantly reduced device noise compared to reference MOS-type SiNWFETs. This top-gate SJGFET also shows very strong noise dependence on substrate bias (V_{sub}). To enhance the SJG control over the SiNW channel, further SJGFET optimization is then performed by using a 3D SJG wrapping both top surface and sidewalls of the SiNW channel in **paper Ⅳ**. Such tri-gate SJGFETs with optimized geometry exhibit significantly enhanced electrostatic control over the channel, and can confine the I_{DS} in the SiNW bulk and maintain excellent noise performance in a large V_{sub} window. Thus, combining our low noise tri-gate SJGFET device with a close to Nernstian limit sensing surface can be a promising solution for future robust low noise nanoscale sensors. In addition, **paper Ⅴ** presents a systematic investigation of top-bottom gate coupling effect on the low frequency noise (LFN) in SJGFETs. Furthermore, **paper Ⅵ** proposes and demonstrates a LBJT fabricated on an SOI substrate to serve as an internal current amplifier for immediate sensor current amplification. This internal signal amplification is ex-

pected to significantly suppress the environmental interference and improve overall SNR especially for low sensor current situations.

2. SiNWFET Fabrication and Characterization

SiNWFETs in this work are fabricated on SOI wafers using standard silicon process technology. The most important and challenging part is the formation of SiNWs, which will be introduced in detail in section 2.1 and 2.2. In order to reduce processing time, a mixed lithography, combining photo-lithography for large structures and electron beam lithography for SiNWs, is developed in section 2.3. Finally, a description of the entire process flow for the SiNWFETs can be found in section 2.4.

2.1. Nanofabrication for SiNWs

There are two main categories of process schemes for fabrication of SiNWs: bottom-up and top-down [48]. The bottom-up approach is based on self-assembly growth mechanism. As-fabricated SiNWs are randomly distributed with their diameters determined by the sizes of the catalytic nanoparticles. Even though the cost of fabrication by bottom-up method is low, later SiNWFET process integration has proven to be challenging particularly in a large scale due to difficulty in the precise manipulation of the SiNWs. In this thesis, a top-down approach is applied to produce SiNWs, *i.e.*, the SiWNs are first defined using lithography and transferred to silicon substrate by reactive ion etching (RIE) afterwards.

As mentioned in the introduction, SiNWs with nanoscale dimensions are desired for sensor applications requiring high charge sensitivity. To achieve such small SiNWs with width down to several nanometers using top-down approach, there are two key factors need to be considered. First, the lithography tool should have a spot size small enough to be able to define nanostructures. Photo-lithography is commonly utilized while its resolution is mainly limited by the wavelength of the light source. With years of development, nowadays sub-100 nm structures can be mass produced by state-of-the-art photo-lithography [49]. However, considering production cost and flexibility, electron beam (e-beam) lithography (EBL) is a better candidate when it comes to extremely small structures, *i.e.*, sub-10 nm. The spot size of e-beam can be just a few nanometers. Meanwhile, throughput of modern EBL tools has been greatly improved [50]. Second, negative resist with high resolution is also required for SiNW pattern definition. Hydrogen silsesquioxane, HSQ, is a commonly used negative e-beam resist with a fine resolution of ~10 nm

[50]–[53]. In addition, unlike most polymeric resists, HSQ belongs to a class of inorganic compounds and turns to silicon dioxide after being exposed by e-beam [54]–[59]. Such unique property makes HSQ very flexible in integration with polymeric resist-based lithography processes to improve throughput, which will be elaborated in detail in later section [60].

Combining EBL and HSQ, a robust lithography process for defining 10 nm resist lines is developed. Top and cross-sectional SEM images of a 10 nm resist line are shown in Figure 2.1. During process optimization for the 10 nm resist line, effect of HSQ aging on line edge roughness (LER) is systematically investigated. It is found that fine 10 nm resist lines with an unchanged LER can be fabricated even with the use of 10 months expired HSQ by applying a reduced dose due to the aging effect of HSQ. And this aging process can be well described by the Avrami model [61]–[63] with the assumption of molecule clustering and cluster aggregating, which is published in **paper Ⅰ**.

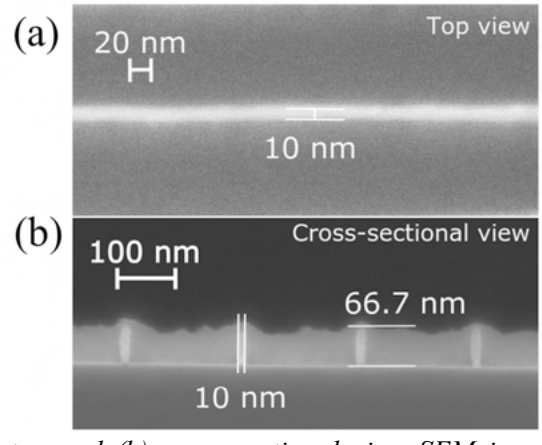

Figure 2.1. (a) top and (b) cross-sectional view SEM images of a 10-nm wide HSQ resist line after development. Adapted with permission from [64]. *Copyright (2016) Elsevier.*

2.2. Solutions for common EBL issues

This section provides solutions for some common issues during EBL exposures.

Ideally, the pattern area should receive uniform and adequate electron exposure to achieve an accurate delineation and size as designed. However, backscattered electrons can also introduce exposure to the area outside the pattern area. As illustrated in Figure 2.2, resist at point B can be exposed by the backscattered electrons coming from the point A of beam incidence. This phenomenon is called proximity effect [65].

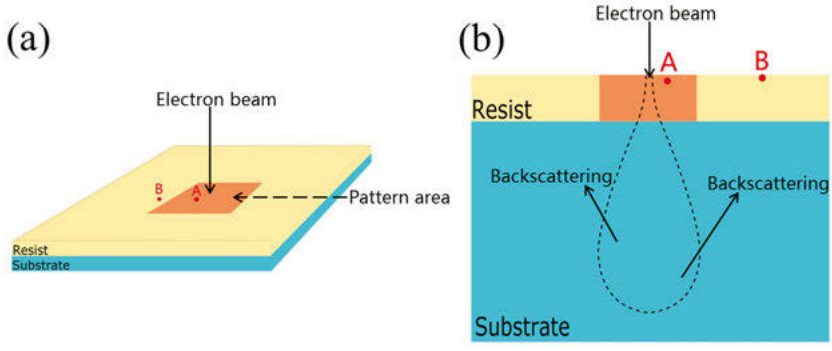

Figure 2.2. (a) 3D sketch of a substrate coated with resist, (b) cross-sectional view of the pattern area.

The proximity effect can cause dose variations between pattern elements or even inside a pattern element, for example, different geometries (*e.g.* square or round) of the pattern elements and the distributions (spacing and sizes) of the adjacent pattern elements. In general, a smaller pattern requires higher dose than a larger one, and an isolated pattern requires higher dose than the one in a densely packed area. Apart from the pattern itself, the proximity effect is also dependent on beam acceleration voltage, resist type, concentration and thickness, substrate material, and development process.

Because of the proximity effect, pattern definition is subjected to different degrees of deterioration. Therefore, in order to achieve accurate pattern delineation, it is necessary to apply some exposure adjustments to compensate for the proximity effect.

2.2.1. Dose optimization

As mentioned earlier, the proximity effect can cause a non-uniform distribution of actually received exposure dose in the pattern area, which can be observed clearly as cases of under/over dose as shown in Figure 2.3. When the dose is inadequate, the edges, especially the corners, of the pattern cannot be fully exposed. With too high dose, the resist outside the pattern area will instead also be exposed. Therefore, it is always recommended to first apply a dose matrix to the desired pattern on a dummy sample to identify an optimal dose range for achieving the best exposure result.

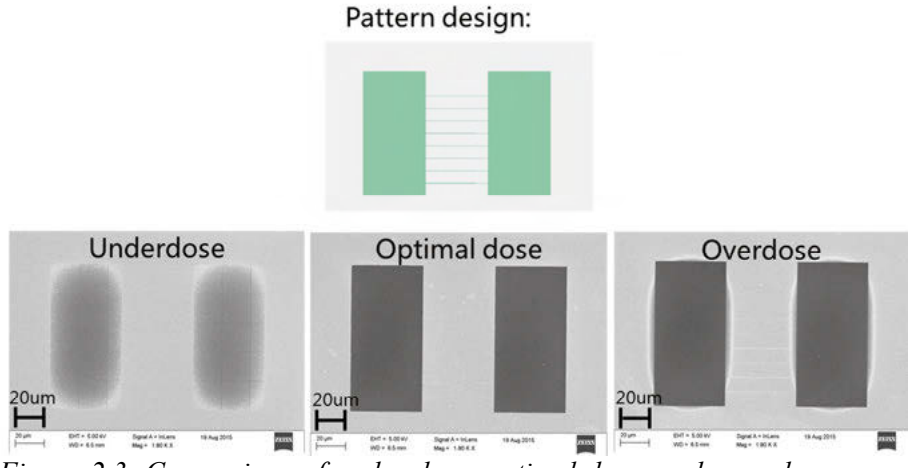

Figure 2.3. Comparison of under-dose, optimal-dose, and over-dose exposures.

2.2.2. Pattern optimization

In most cases, an optimal dose can be found after a dose test to achieve a satisfactory result. However, for some patterns, the proximity effect cannot be completely avoided even with the optimal dose because the exposure received in the center of a pattern is much higher than that on the edges. Therefore, pattern zoning is needed in such case.

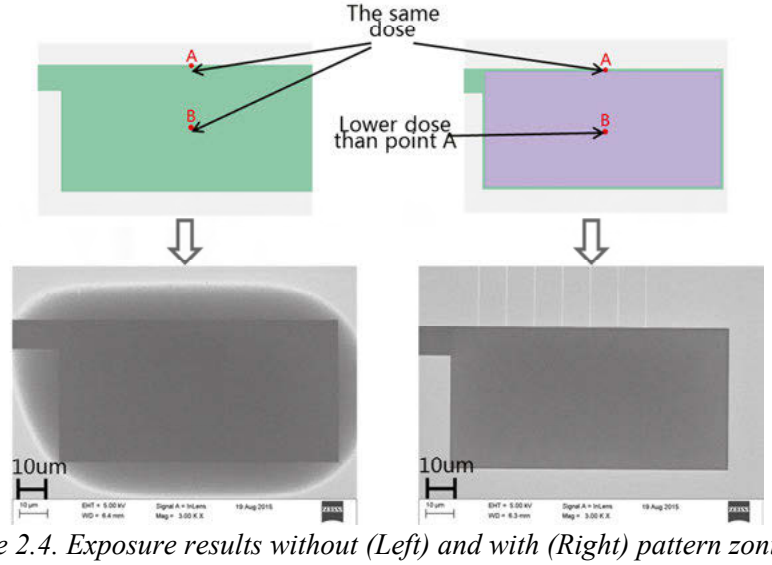

Figure 2.4. Exposure results without (Left) and with (Right) pattern zoning.

In the example provided in Figure 2.4 (Left), additional exposed resist is found around the edges of the pattern due to proximity effect when a single dose is applied to the whole pattern area. As shown in Figure 2.4 (Right), by pattern zoning, the original pattern is divided to two zones, one is the outer ring section (green) indicated by A, and another is the inner section (violet) marked by B. Then a higher dose is assigned to the outer ring A compared to the inner section B, which results in better exposure result as shown by the SEM image (Right).

2.2.3. Lithography step optimization

Apart from pattern zoning, using multiple lithography steps to expose different patterns contiguously and independently can also be an effective solution to reduce the proximity effect. However, this method can only be used when HSQ is involved because of its unique transition property so patterns defined by HSQ are not affected during the lithography process with other resists, as discussed in section 2.1.

Figure 2.5 shows an example of exposed nanowire with two adjacent large pads with the same resist. With one EBL step, the two ends of the nanowire are widened because they can also receive dose during the exposure of the two pads. With two EBL steps, the nanowire is exposed and developed first, then the pads. During the second exposure for the pads, the HSQ resist at the two ends of the nanowire can still receive backscattered electron from the pad area. However, this additional expose will not impact the resist pattern at the two ends of the nanowire since the HSQ nanowire is already developed. Therefore this second exposure will not widen the nanowire. As a result, uniform nanowire can be obtained as shown by the SEM images in Figure 2.5.

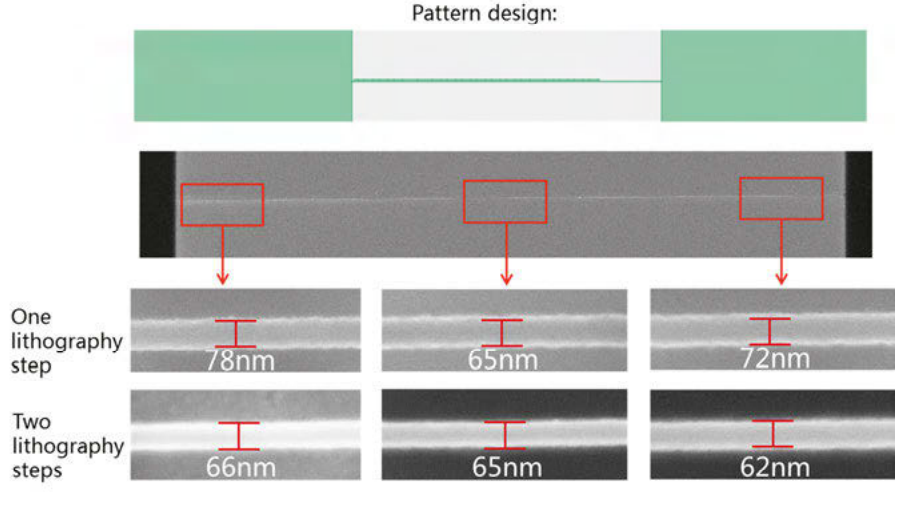

Figure 2.5. Exposure comparison between one-step and two-step lithography.

2.3. Mixed lithography

After definition of SiNW patterns, source and drain terminals (S/D) with diameters up to hundreds of micrometers are also defined by lithography. SiNW exposure requires low beam current and high exposure dose and it is extremely time-consuming to apply the same SiNW EBL process for S/D exposure. It is possible to save exposure time by applying higher beam current and lower dose, however no significant improvement can be made since the base dose required for HSQ is still high. In contrast, photo-lithography with significantly higher throughput would be a favorable choice for patterning such large structures. As explained in section 2.1, HSQ turns to SiO_2 after e-beam exposure and the resultant resist lines are stable when they are subjected to photo-lithography process. In order to increase overall process throughput, mixed lithography process was developed combining HSQ EBL and photo-lithography for SiNW and S/D patterning, respectively. Afterwards, pattern transfer to silicon substrate is achieved by silicon RIE. A SiNWFET with multiple channels patterned using the mixed lithography is shown in Figure 2.6.

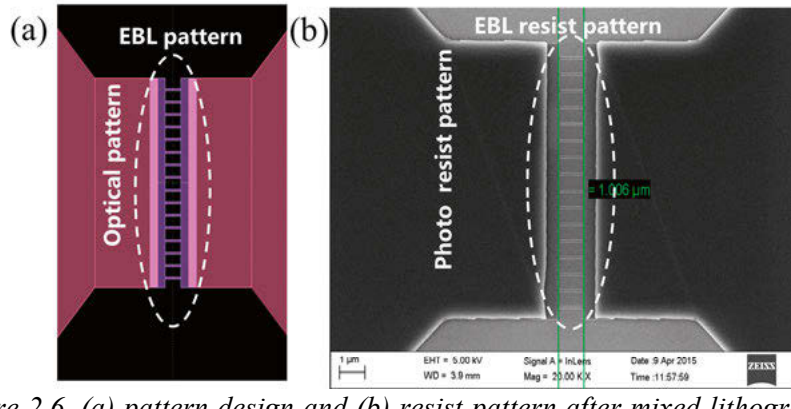

Figure 2.6. (a) pattern design and (b) resist pattern after mixed lithography exposure of a SiNWFET with multiple SiNWs and S/D.

2.4. Fabrication of SiNWFETs

Schematic representation of the fabrication process flow for SiNWFETs can be found in Figure 2.7. In detail, the SiNWFETs were fabricated on 100-mm SOI wafers using standard silicon process technology. The SOI wafers consist of a 200-nm thick lightly *p*-type doped silicon layer on top of a 375-nm thick buried oxide (BOX). The top silicon layer was thinned down from 200 to 120 nm via thermal oxidation. Arsenic (As) implantation was then performed to form the n^+-doped S/D with the channel region being protected by photoresist during the implantation. The SiNWFET structures with SiNWs

and S/D were defined by mixed lithography and RIE. The width of the SiNWs after RIE varied from 90 to 150 nm while the length was fixed at 2 µm. A SEM image showing SiNW and S/D after pattern transfer is shown in Figure 2.8(a). A 15 nm thick Pt layer was evaporated and patterned on the n^+-S/D regions via lift-off. Platinum silicide (PtSi) was subsequently formed by rapid thermal processing (RTP) at 500 °C for 30 s in N_2. Gate oxide of 5-nm HfO_2 was subsequently grown by atomic layer deposition (ALD) at 350 °C. Gate and S/D contact pads of 10 nm Ti and 100 nm Pt were evaporated and patterned via lift-off, followed by forming gas annealing (FGA) at 400 °C for 30 min. A completed SiNWFET with a metal top gate is shown in Figure 2.8(b).

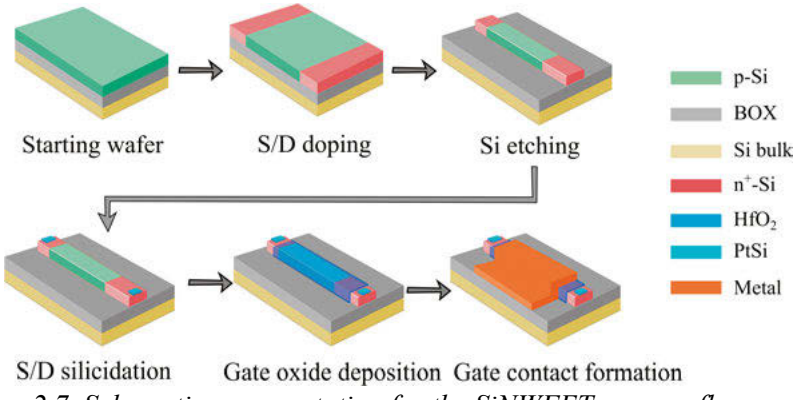

Figure 2.7. Schematic representation for the SiNWFET process flow.

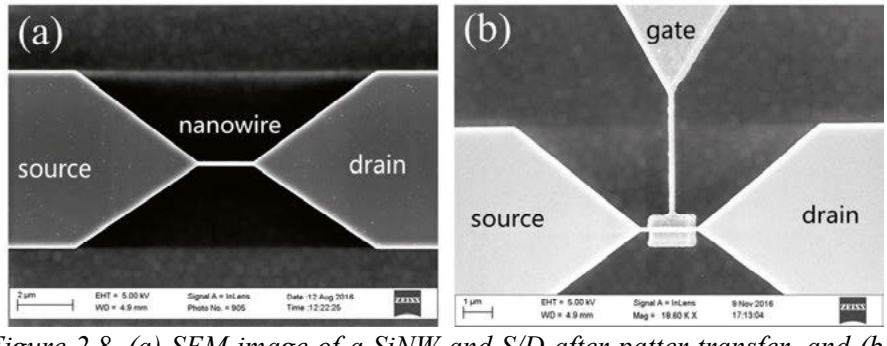

Figure 2.8. (a) SEM image of a SiNW and S/D after patter transfer, and (b) a completed SiNWFET with a metal top gate.

2.5. Electrical characterization

Four point measurements were applied to identify the resultant doping concentration after dopant implantation and activation. After the establishment

of the SiNWFETs, direct current (DC) and LFN characterizations were conducted for performance evaluation.

2.5.1. DC characterization

Transfer (I_{DS} vs. V_G (gate voltage)) characteristics of the SiNWFETs were measured at room temperature on a probe-station using a Keysight B1500A precision semiconductor parameter analyzer. Typical I_{DS} vs. V_G curves of the SiNWFETs are shown in Figure 2.9. These SiNWFETs have SiNW channel width ranging from 90 to 150 nm and the same channel height of 120 nm with 5 nm ALD HfO_2 as the gate oxide. The SiNWFETs exhibit I_{on}/I_{off} ratios over 10^6 and subthreshold slope (*SS*) between 110 and 160 mV/dec.

Device simulations were implemented to assist data interpretation by using commercially available simulation tools (Sentaurus Device from Synopsys) for all the devices studied in this thesis. Geometries and doping profiles of the devices were defined using Sentaurus Structure Editor.

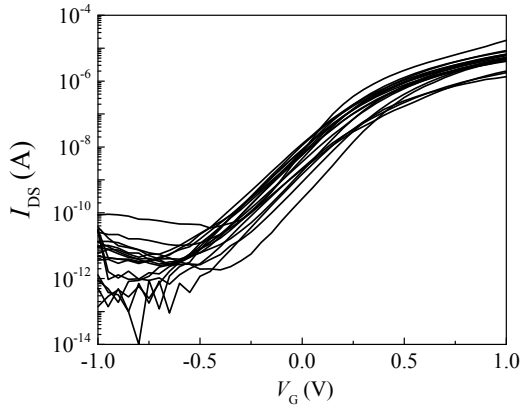

Figure 2.9. Transfer characteristics for multiple SiNWFETs.

2.5.2 LFN characterization

LFN of SiNWFETs is characterized using a commercial Keysight E4727A advanced low-frequency noise analyzer with a Keysight B1500 parameter analyzer supplying DC biases to the SiNWFET terminals. During the measurement, V_G bias was determined by the E4727A based on the transfer characteristic of the SiNWFET and I_{DS} set value.

To achieve a reliable LFN measurement, the first step is to ensure that the external interference (environmental noise) is low and its contribution to the measured device noise is negligible. When the device is measured on a probe station, extra noise generated by high power sources inside the laboratory, such as heaters and ovens, may be coupled to the noise measurement. An

example of severe external interference is shown in Figure 2.10, in which S_{id} of a reference FET measured on a probe station differs significantly to S_{id} measured on the same device but in a well-shield test fixture. Such difference is ascribed to the environmental noise which should be minimized through a debugging procedure before any measurement on sharp devices. Such calibration procedure is always performed throughout the noise studies in this thesis to ensure measurement integrity.

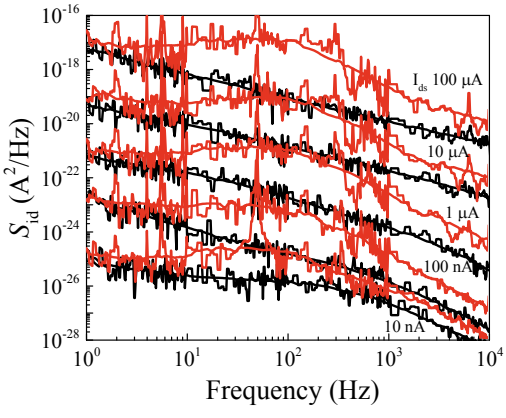

Figure 2.10. S_{id} of a reference FET under different I_{DS} measured in a well-shielded test fixture (black) and on probe station (red). The difference between the two measurements is due to external interference when the FET is measured on a probe station and should be minimized.

It is essential to understand how the instruments perform the measurement and process the noise data to avoid wrong interpretation due to any error or artifact in the noise data. Figure 2.11(a) shows a simplified block diagram for 4-terminal LFN measurement on a FET. The voltage fluctuations S_{vd} at the drain terminal of the FET can be calculated by

$$S_{vd}[V^2/\mathrm{Hz}] = (N_{V\_meas}[V/\sqrt{\mathrm{Hz}}]/G_{VAMP})^2, \tag{2.1}$$

where N_{V_meas} is the voltage fluctuations after amplification and G_{VAMP} is the gain of the voltage amplifier (VAMP). According to the equivalent circuit model shown in Figure 2.11(b), S_{vd} is contributed from three independent noise sources, *i.e.*, S_{id} of the FET and thermal noise from the load resistance (R_{load}) and the 1 MΩ input resistance (R_{in}) of the VAMP. S_{id} of the FET can be calculated by deducting the thermal noise contributed by R_{load} and R_{in} from S_{vd},

$$S_{id} = \frac{S_{vd} - 4kT\frac{1}{1/R_{load}+1/R_{in}}}{\left(\frac{1}{1/r_{ds}+1/R_{load}+1/R_{in}}\right)^2}, \tag{2.2}$$

where r_{ds} is the output resistance of the FET. From Eq. 2.2, the minimum S_{id} which the instrument can measure is determined by the thermal noise of the 1 MΩ R_{in} if R_{load} is significantly larger than 1 MΩ. Such noise floor estimated from the circuit model agrees well with the measured S_{id} floor of ~10^{-26} A^2/Hz shown in Figure 2.10(black curve, I_{DS}=10 nA). Finally, the input-referred S_{VG} of the FET is automatically calculated by the instrument via

$$S_{vg}[V^2/\mathrm{Hz}] = S_{id}[A^2/\mathrm{Hz}]/g_m^2. \tag{2.3}$$

Here g_m is the transconductance of the FET at the I_{DS} set point. Sometimes the actual I_{DS} which the instrument can achieve during S_{id} measurement can differ significantly from its set point, especially when the FET is biased in the subthreshold region, which results in large error in g_m and S_{VG}. In such case the g_m should be calibrated based on the actual measured I_{DS} (not its set value) and S_{VG} should be recalculated using the calibrated g_m.

LFN measurement at high frequencies may be limited by frequency roll-off of the system. As shown in Figure 2.10, a change in slope of the frequency response can be seen at f~500 Hz for S_{id} measured with I_{DS}=10 nA (black curve). It is important to understand if such change is intrinsic FET characteristics, or artifact due to high frequency limitation of the instrument. The roll-off frequency ($f_{roll\text{-}off}$) of the system can be determined through

$$f_{roll-off} = \min(f_{roll-off1}, f_{roll-off2}), \tag{2.4}$$

where

$$f_{roll-off1} = \frac{1}{2\pi C_{in}\frac{1}{1/r_{in}+1/R_{source}}}$$

$$f_{roll-off2} = \frac{1}{2\pi C_{out}\frac{1}{1/r_{out}+1/R_{load}+1/1M\Omega}}.$$

C_{in}=100 pF+C_{cable} and C_{out}=160 pF+C_{cable} are input and output parasitic capacitances, respectively. r_{in} and r_{out} are equivalent input and output resistances. It is essential to keep the measurement cable as short as possible since $f_{roll\text{-}off}$ is inversely proportional to C_{cable}. Using Eq 2.4 and all the parameters configured by the instrument, $f_{roll\text{-}off}$ calculated for S_{id} measurement at I_{DS}=10 nA is 578 Hz, which confirms that the slope change is due to the frequency roll-off of the system. In general, $f_{roll\text{-}off}$ should be calculated based on the actual length of the measurement cables for each S_{id} measurement.

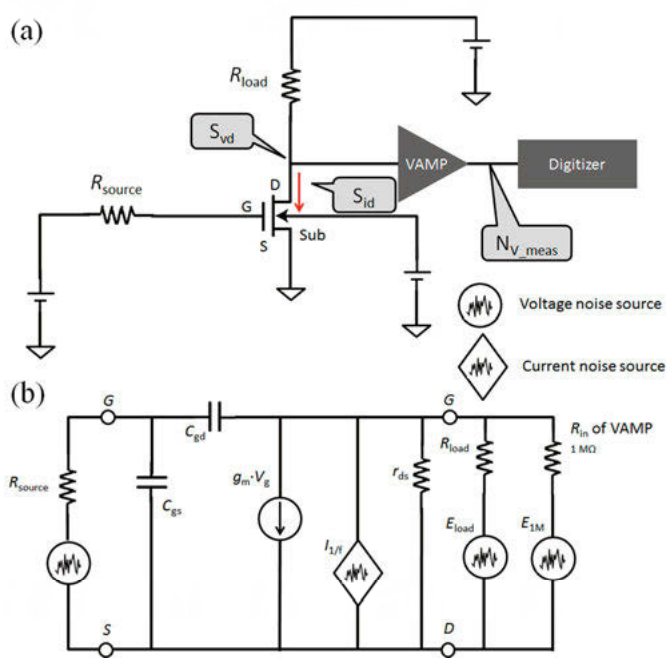

Figure 2.11. (a) Simplified diagram for 4-terminal LFN measurement on FET. The gate, drain, source, and substrate terminals are annotated with G, D, S, and Sub in the diagram, respectively. (b) Equivalent circuit model for calculating S_{id} and S_{vg} of the FET from measured noise.

3. Proof-of-Concept Ion Selective Sensor

With the established fabrication process for SiNWFETs, effort was then put on proof-of-concept selective ion detections. Multiplexed analyses of liquid samples, *e.g.*, water, sweat, blood, saliva, and urine, which consist of a complex matrix of small molecules, molecular ions, and elemental ions, have drawn great attentions in recent years [6], [9], [66]–[68]. Such analyses can reveal rich information of individual's physiological state or identify biomarkers which are essential for early disease diagnosis [69]–[76]. Ion-binding receptors, *i.e.*, ionophores, have been widely used on potentiometric sensors for selective ion detections [27], [77]. Commercially available ionophores are mainly for elemental and other small ions while limited options are available for large biologically relevant molecular ions [27]. Conventionally, these molecular ions are usually measured quantitatively by, for example, high-performance liquid chromatography (HPLC) [78] and gas chromatography-mass spectrometry (GC-MS) [79] which require highly-skilled operators, expensive and bulky apparatuses, and also are time consuming [80]. Recently, a new class of synthetic receptors, *i.e.*, metal-organic supercontainers (MOSCs), have been demonstrated to be an efficient ionophore for large molecular ions [81]–[84]. Conventional ion-selective electrodes (ISEs) with MOSC molecules incorporated into poly(vinylchloride) (PVC) mixed-matrix membranes (MMMs) exhibited a near-Nernstian response towards methylene blue (MB^+) that has a positive charge and a molecular size closely matching the MOSC's cavity size [85]. The tunability of the nanocavity structure in the MOSCs is anticipated to offer exciting new opportunities in the potentiometric sensing of a wide range of molecular ion targets.

In this thesis, ionophore-incorporated MMMs are chosen as the ion-selective layer on the gate insulator of SiNWFETs. MMMs have been shown to establish a more stable interface potential with the electrolyte [27], [77] than covalently functionalized ion receptors [21], [86], [87]. The success in potentiometric molecular ion sensing using a MOSC-incorporated MMM offers the opportunity to integrate both molecular and elemental ion sensors on a single chip. Besides the MB^+ specific sensor, a Na^+-specific sensor is fabricated using the same type of polymer matrix and commercially available Na^+-ionophore. Finally, multiplex detection of MB^+ and Na^+ ions in one electrolyte using SiNWFET sensor array is demonstrated.

3.1. Preparation of ion-selective mixed-matrix membrane

MMM solutions were prepared by dispersing ionic site and ion receptors into a solution of tetrahydrofuran (THF) and PVC. MOSC (1-Co) and Na^+-ionophore are used as ion- selective receptors for MB^+ and Na^+, respectively. Once the solution was mixed and there were no visible particles, the MMMs were drop cast on the chip device area by pipettes. As shown in Fig 3.1(a), the diameter of the MMM on the chip is ~2mm and multiple MMMs targeting different ions can be fabricated on the same chip, enabling analysis of multiple ions in one single solution. A zoom-in view of the MMM/electrolyte interface is schematically shown in Figure 3.1(b). The ionophore in the MMM can selectively interact with the target ions in the electrolyte. As a result, a potential shift is generated across the interface when the activity of the target ions is changed, which can be read out as a shift of V_{TH} of the SiNWFET sensor. More details regarding fabrication of ion-selective SiNWFET sensor and multiplexed analysis can be found in **paper II**.

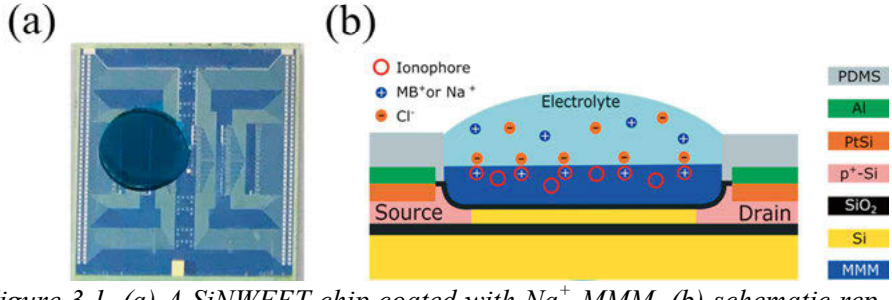

Figure 3.1. (a) A SiNWFET chip coated with Na^+-MMM, (b) schematic representation of MMM/electrolyte interface.

3.2. Molecular ion detection

To demonstrate the critical function of metal-organic supercontainer (MOSC) in selective detection of molecular ions, two mixed-matrix membranes (MMMs), i.e., methylene blue (MB^+)-MMM1 with MOSC and MB^+-MMM2 without MOSC, were fabricated and their responses to MB^+ activities are plotted in Figure 3.2(a). Each data point in the response curves represents an average of three independent measurements. SiNWFET coated with MB^+-MMM1 containing MOSC exhibits a near-Nernstian towards MB^+ activity (α_{MB^+}) and good reproducibility. A deviation from the ideal Nernstian response is found at high α_{MB^+}, which can be explained by the co-extraction of MB^+ and Cl^- from the sample into MMM, leading to the so-

called Donnan failure [88], [89]. SiNWFET coated with MB^+-MMM2 is sensitive to MB^+, with, however, large variations between each measurement. The increase of lower detection limit and poor reproducibility of the MB^+-MMM2 is likely due to the continues partitioning of MB^+ into the hydrophobic MMM during measurement as there is no MOSC to stabilize the MB^+ concentration in the MMM. The results here clearly demonstrate the critical role of the MOSC for achieving a Nernstian response with good stability. Finally, as shown in Figure 3.2(b), SiNWFET coated with MB^+-MMM1 shows good selectivity over Na^+, K^+, and H^+ which are common interfering ions present in practical samples such as sweat and serum.

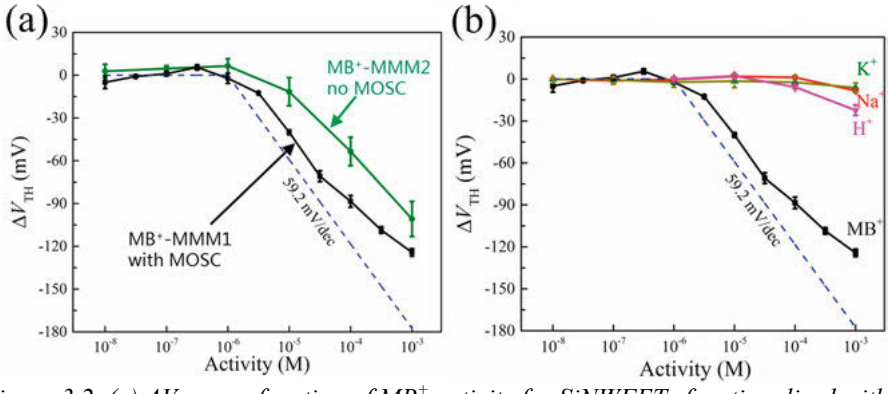

Figure 3.2. (a) ΔV_{TH} as a function of MB^+ activity for SiNWFETs functionalized with MB^+-MMM1 and MB^+-MMM2, and (b) response the MB^+-MMM1 functionalized SiNWFET to Na^+, K^+, and H^+. Adapted with permission from [33]. *Copyright (2018) Elsevier.*

3.3. Elemental ion detection

The Na^+-specific SiNWFET sensor exhibits a near-Nernstian response with a slope of 57.9 mV/dec in a wide Na^+ activity (α_{Na+}) range from 100 µM to 100 mM, with a lower detection limit of ~60 µM, as shown in Figure 3.3. However, the Na^+-specific sensor is susceptible to MB^+ interference as evident by its response to MB^+, which can be ascribed to the hydrophobic interactions between the polymer matrix and MB^+, similar case as the MB^+-MMM2. In order to achieve reliable detection of elemental ions in multiplexed analysis, it is important to control the activity of hydrophobic molecular ions below the threshold to avoid their rapid incorporation into MMM. Meanwhile, doping the MMM by polyethylene glycol (PEG) is also a promising approach to lower the hydrophobicity of the MMM so the Na^+-specific sensor becomes more stable in the presence of molecular ions.

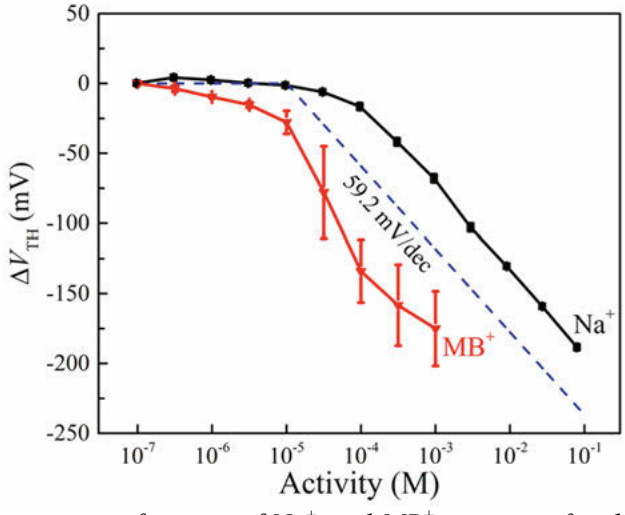

Figure 3.3. ΔV_{TH} as a function of Na^+ and MB^+ activities for the SiNWFET functionalized with Na^+-MMM. Adapted with permission from [33]. *Copyright (2018) Elsevier.*

3.4. Multiplexed ion detection

Finally, the MB^+-specific and Na^+-specific SiNWFET sensors were integrated on the same chip. Figure 3.4(a) is a photo showing an array of SiNWFETs with MB^+-MMM and Na^+-MMM formed by drop-casting. Multiplexed analysis of molecular and elemental ions is demonstrated with MB^+ and Na^+ concentration series prepared in both deionized water (DI) and river water. To avoid false response on the Na^+-specific sensor, the MB^+ activity in the solution is kept below the threshold, i.e., 10 μM, during the demonstration. As displayed in Figure 3.4(b), the experiment was first conducted with DI water (solid line), then with river water (dashed line). The sensors are operated simultaneously and are able to respond selectively to the targets in a complex sample. It is worth noting that cross interference is still the main issue limiting the operation range of multiplexed analysis. Further engineering of MMM to enable effective shielding of hydrophobic ions will be essential for practical applications of such a platform.

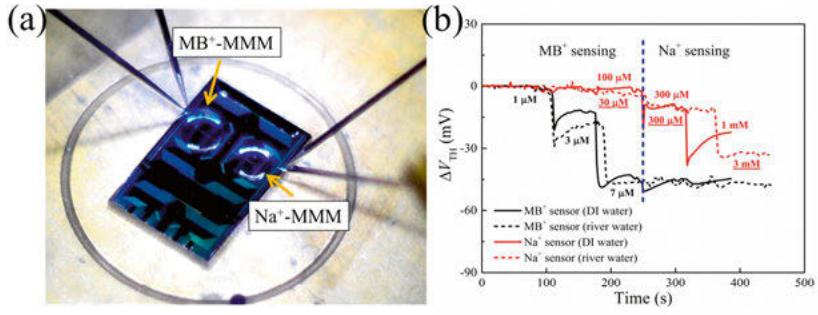

Figure 3.4. (a) Photo picture of a SiNWFET chip coated with MB^+-MMM (left) and Na^+-MMM (right), and (b) multiplexed measurement of MB^+ (black) and Na^+ (red) in one solution with the concentration series prepared with DI water (solid lines) and river water (dashed lines). Adapted with permission from [33]. *Copyright (2018) Elsevier.*

4. Schottky Junction Gated SiNWFET (SJGFET) for Noise Mitigation

In a SiNWFET sensor, the gate surface is functionalized with receptors that selectively bind to targets of interest, leading to a change in surface potential $\Delta\varphi_s$ and consequently a shift of V_{TH} of the SiNWFET. ΔV_{TH} represents the original sensing signal and is primarily determined by the surface properties of the sensing layer on gate terminal and the kinetics of interactions between the receptors and the targets. Extensive studies have been performed to optimize the sensing layer and high sensing signal close to the Nernstian limit [31], *i.e.*, 60 mV/dec (analyte concentration change) at room temperature, have been reported in literature [32]–[35].

When the SiNWFET sensor is operating in electrolytic environment, the sensor noise can still be dominantly contributed from the intrinsic device noise which ultimately sets the lower detection limit of the sensor. There have been constant efforts to further improve the sensitivity of the SiNWFET sensor towards detection of discrete charge events, even down to single molecular level. One of the most popular approaches is downsizing the SiNW channel which unfortunately lead to dramatic increase in device noise as the noise is known to be inversely proportional the device area. After successful demonstration of selective ion detection with close to the Nernstrian response using our SiNWFET sensors, we move forward to address the noise issue of the MOS-type SiNWFET sensor.

4.1. Schottky junction top-gate SiNWFET (Top-SJGFET)

To emulate the low noise JFETs, Schottky junction gated SiNWFET (SJGFET) is developed, using a silicide/silicon Schottky junction to replace the noisy oxide/silicon interface. The design of the SJGFET is similar to the JFET where the channel is pinched off by depletion layers originating from the gate Schottky junctions, as descripted in Figure 4.1. The Schottky junction is advantageous due to its atomically abruptness, which enables the ultra-shallow gate junction formation on the nano-dimension SiNW channel.

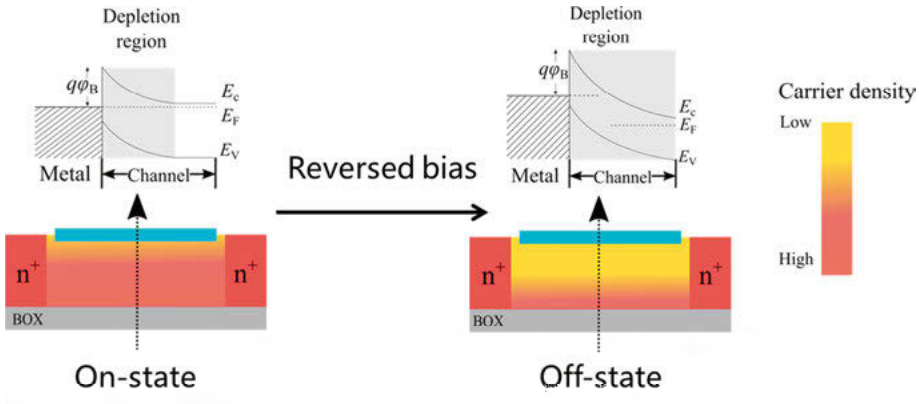

Figure 4.1. Cross-sectional sketches and band diagrams showing the working principle of a SJGFET.

A simulated transfer curve of an SJGFET with *n*-doped channel and n^+-doped S/D can be found in Figure 4.2(a). When a positive V_G is applied, the channel is partially depleted and the SJGFET is at on-state, as indicated by ① in Figure 4.1(a) with the corresponding channel electron density contour shown in Figure 4.2(b). As V_G reduces, the depletion layer expands and pinches off the channel at V_{TH} as shown by ③. When further reducing V_G, the SJGFET operates in subthreshold region where its I_{DS} decreases exponentially with V_G.

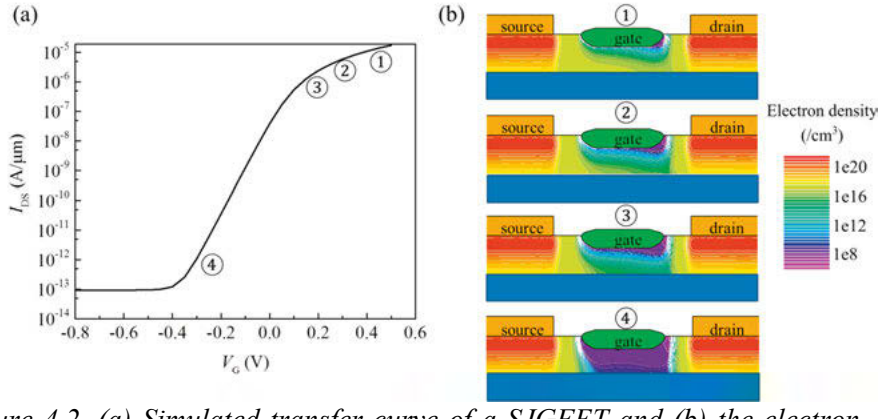

Figure 4.2. (a) Simulated transfer curve of a SJGFET and (b) the electron density in the SiNW channel corresponding to the different V_G as indicated by the numbers in (a). At V_{TH}, the source end of the SiNWFET is fully depleted, as indicated by ③. Reprinted with permission from [90]. *Copyright (2019) American Chemical Society.*

Assuming a flat-band condition at the bottom BOX/silicon interface, V_{TH} of an SJGFET can be calculated as [47]:

$$V_{TH} = \Phi_B - \frac{(E_C - E_F)}{q} - \frac{qN_D t_{Si}^2}{2\varepsilon_{Si}}, \quad (4.1)$$

where Φ_B is the Schottky junction barrier height, E_C the bottom edge of conduction band and E_F the Femi level, t_{Si} the SiNW channel thickness, and ε_{Si} the dielectric constant of silicon. The leakage current of the SJG, I_{GS}, can be described by the thermionic emission theory [47]:

$$I_{GS}/A = A^* T^2 \exp(-\frac{q\emptyset_B}{kT})[\exp\left(\frac{qV_G}{kT}\right) - 1], \quad (4.2)$$

where A is the junction area and A^* the effective Richardson constant. It is essential that the SJGFET operates without excessive forward biasing the junction gate to avoid large I_{GS}. Therefore, a high Φ_B of the junction is favorable according to Eq 4.2. PtSi is chosen as the gate metal because of its high Φ_B, 0.85 eV, to *n*-Si and good compatibility with the standard CMOS process flow [91], [92]. In present work, a design range of V_{TH} from -1 to 0.2 V is implemented for practical considerations of operation in electrolyte, which means N_D in the SiNW channel should be controlled between 1.0×10^{17} and 3.2×10^{17} cm^{-3} for t_{si} = 80 nm, for instance.

In a first attempt, SJGFETs were designed and fabricated with the Schottky junction gate (SJG) present only on the top of the SiNW channel. A cross-sectional sketch of a top-gate SJGFET (Top-SJGFET) including annotations of critical design parameters is shown in Figure 4.3. For comparison, control groups of inversion-mode and depletion-mode MOS-type SiNWFETs, *i.e.*, InMOSFET and DeMOSFET, were also designed, as depicted in Figure 4.3.

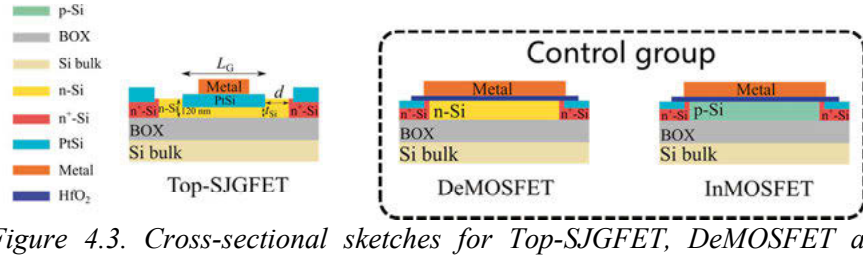

Figure 4.3. Cross-sectional sketches for Top-SJGFET, DeMOSFET and InMOSFET. Adapted with permission from [90]. *Copyright (2019) American Chemical Society.*

4.1.1. Fabrication of Top-SJGFETs

The Top-SJGFETs and MOSFETs are fabricated by means of standard silicon process technology. The Top-SJGFETs have a SiNW channel N_D of 1.2×10^{17} cm^{-3} according to sheet resistance measurements. A PtSi layer was formed on top of the SiNW channel as well as on the n^+-S/D pad regions. Optimizations on Pt thickness and silicidation process are critical since poor

coverage of gate silicide due to the aggregation of PtSi [93] may occur and cause substantial gate leakage current. The channel is *p*-type for the In-MOSFETs with the doping level (N_A) defined by the starting top silicon layer of the SOI wafer. For the DeMOSFETs, the channel was *n*-type with the same N_D as for the Top-SJGFET. The device patterning is performed using the mixed-lithography as discussed in Section 2.3, to improve overall throughput. More detailed information regarding the fabrication processes as well as characterizations of the SiNW and PtSi/silicon gate junction can be found in **paper III**. The top-view SEM image of a completed Top-SJGFET is shown in Figure 4.4 (a), and a completed MOSFET in Figure 4.4(b), with gate contact arm formed.

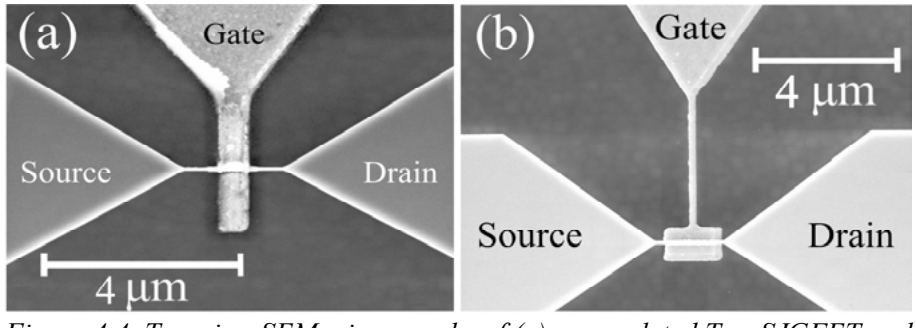

Figure 4.4. Top-view SEM micrographs of (a) a completed Top-SJGFET and (b) MOSFET. Reprinted with permission from [90]. *Copyright (2019) American Chemical Society.*

4.1.2. DC characterization of Top-SJGFETs

The Top-SJGFET exhibits significantly enhanced gate coupling, as represented by a near-ideal subthreshold slope, *SS*, of 60.5 mV/dec as seen in Figure 4.5, in comparison to 157.1 mV/dec and 228.0 mV/dec for the In-MOSFET and the DeMOSFET, respectively. *SS* of a MOSFET determines ΔV_G needed to change I_{DS} by one decade in the subthreshold region and can be calculated through [47]:

$$SS = 2.3\frac{kT}{q}\left(1+\frac{C_D+C_{it}}{C_{ox}}\right), \tag{4.3}$$

with C_{ox} and C_D the gate oxide capacitance and the silicon depletion-layer capacitance, respectively. C_{it} is the capacitance associated with the gate oxide/silicon interface traps. Without the presence of gate oxide, C_{ox} in Eq. 4.3 can be seen as infinitely large therefore V_G is fully coupled to the SiNW channel as the potential drop over the thick BOX is negligible in an SJGFET. Meanwhile, gate leakage, I_{GS}, of the Top-SJGFET is 4 orders of

magnitudes lower than I_{DS} in a large V_G range, which can be further improved by fine tuning t_{si} and N_D.

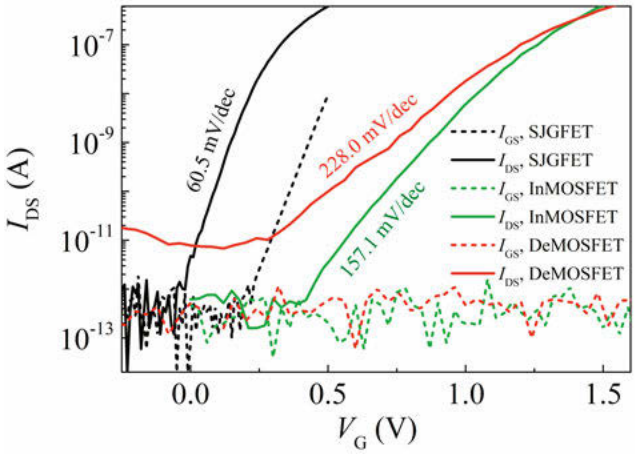

Figure 4.5. Measured I_{DS} (solid lines) and I_{GS} (dash lines) as a function of V_G for a Top-SJGFET (black), a DeMOSFET (red) and an InMOSFET (green). Adapted with permission from [90]. *Copyright (2019) American Chemical Society.*

4.1.3. LFN characterization of Top-SJGFETs

LFN performance of the Top-SJGFETs is systematically investigated at different I_{DS} set values and different bias conditions to elucidate the benefit of replacing the noisy gate oxide/silicon interface with Schottky junction PtSi/silicon interface. The PSD of I_{DS}, S_{id}, of an SiNWFET fabricated on SOI substrate is contributed from three uncorrelated noise sources [41], [46]:

$$S_{\mathrm{id}} = S_{\mathrm{it}} + S_{\mathrm{ib}} + S_{\mathrm{ibulk}}, \tag{4.4}$$

where S_{it} and S_{ib} stand for the noise generated by the top and bottom oxide/silicon interfaces, respectively. S_{ibulk} arises from the fluctuations in the SiNW bulk, which is a film-trap related generation-recombination noise and is significantly lower than S_{it} and S_{ib} [46]. As for the gate referred input noise, *i.e.*, S_{vg}, it can be calculated using S_{id} and g_m of the SJGFET as:

$$S_{\mathrm{vg}} = \frac{S_{\mathrm{id}}}{g_m^2}, \tag{4.5}$$

Here, to facilitate the comparison, "total noise voltage", $\overline{v_T^2}$, which is an integration of S_{vg} from 1 to 500 Hz, is used instead of S_{vg} at a single frequency (see **paper III** for details regarding LFN data analysis) [94]. As seen in Figure 4.6(a), the gate area normalized $\overline{v_T^2}$, *i.e.*, $A \times \overline{v_T^2}$, of the Top-SJGFET are

significantly lower than those of the InMOSFET and the DeMOSFET. Such significant improvement in LFN performance for the Top-SJGFET can be ascribed to the replacement of top noisy HfO_2/silicon interface by a quieter PtSi/silicon junction interface therefore complete suppression of S_{it}.

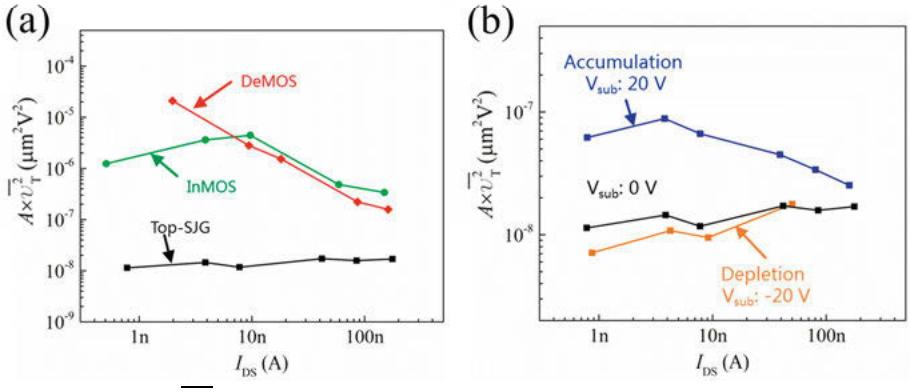

Figure 4.6. $A \times \overline{v_T^2}$ as a function of I_{DS} (a) for the Top-SJGFET, an In-MOSFET, and a DeMOSFET at V_{sub}=0 V, (b) for the Top-SJGFET with different V_{sub}.

LFN measurements were also conducted at different V_{sub} to further investigate the different noise components in the Top-SJGFET and the results are depicted in Figure 4.6(b). With a positive V_{sub}, electrons are accumulated at the BOX/silicon interface. Therefore, I_{DS} of the Top-SJGFET becomes more dominated by the conduction close to that interface and the contribution of S_{ib} to S_{id} increases. On the other hand, with a negative V_{sub}, the conduction is pushed away from the BOX/silicon interface, *i.e.*, deep into the SiNW bulk or close to the quiet PtSi/silicon interface. In such a case, S_{ib} contribution to S_{id} is greatly reduced and S_{id} is now more dominated by S_{ibulk}. As expected, S_{ib} generated at the BOX/silicon interface is a major contributor to S_{id} in the Top-SJGFET. As a result, V_{sub} tuning is normally required for the Top-SJGFET during operation to achieve the optimum LFN performance.

For benchmarking, our results were compared with other related work published from different university laboratories [90]. Although the noise of our SiNW-based Top-SJGFET is not superior to that of the state-of-the-art planar MOSFETs, [44], [95] it is better than reported university SiNW or Si nano-ribbon based FET devices [40], [96]–[98].

4.1.4. Sensing demonstration on Top-SJGFETs

During detections, if the Top-SJGFET, where no silicide is present on the sidewalls of the nanowire, is directly immersed in the electrolyte, the liquid solution will also gate the silicon channel from the two sides of the Si chan-

nel via an oxide/silicon interface. The top-SJGFET will then suffer from the same noise problem as an ordinary MOSFET. Therefore, to demonstrate the ion sensing application of the Top-SJGFET, *p*H and Na^+ sensing using an extended gate [88] is conducted.

The I_{DS}-V_G curves of an SJGFET measured with the top gate under dry condition and with the extended gate under liquid condition are depicted in Figure 4.7(a). The real-time potential shift at different *p*H is shown in Figure 4.7(b). Sensitivity of 56 mV/dec for *p*H and 57.4 mV/dec for Na^+ was achieved by the employed sensing layers as shown in Figure 4.7(c) and (d). The low noise properties of the SJGFET together with the close to ideal sensing signal generated by the sensing layers will hold promises for future high SNR sensor applications.

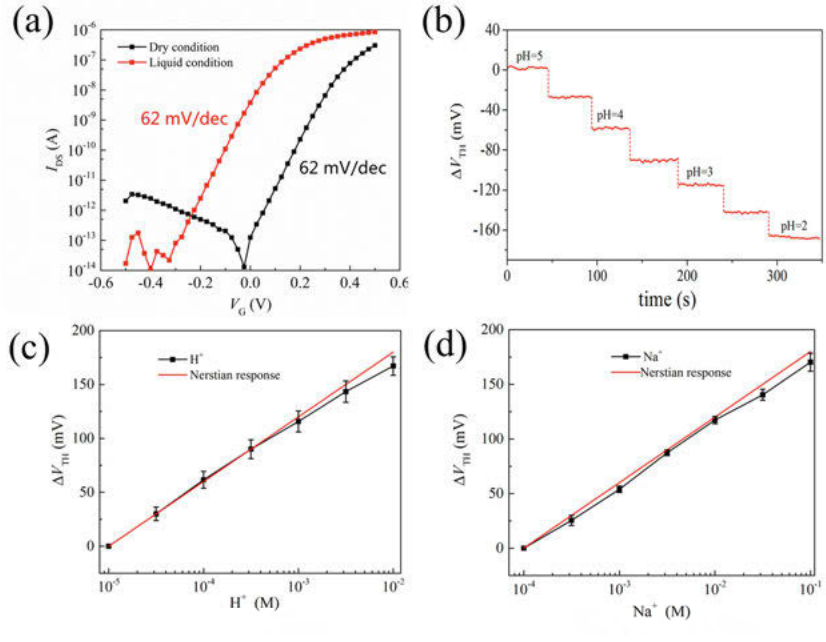

Figure 4.7. (a) Measured I_{DS} as a function of V_G for an SJGFET measured with top gate (dry condition) and extended gate (liquid condition), (b) Real-time ΔV_{th} measurement for an SJGFET with an extended gate. (c) ΔV_{TH} as a function of H^+ concentration. (d) ΔV_{TH} as a function of Na^+ concentration. Adapted with permission from [90]. *Copyright (2019) American Chemical Society.*

4.2. Schottky junction tri-gate SiNWFET (Tri-SJGFET)

LFN of SiNWFETs can be significantly reduced by replacing the noisy oxide/silicon interface with a PtSi junction gate on the top of the SiNW channel. As demonstrated in previous section, the bottom BOX/silicon interface can make significant contribution to the total LFN in a Top-SJGFET, therefore V_{sub} optimization is still required to mitigate such adverse influence. This V_{sub} dependent LFN performance may severely limit the practical application of the Top-SJGEFT based sensors especially in situations requiring high-density integration, as each sensor then needs to be individually tuned. Meanwhile, avoiding large V_{sub} also improves the reliability of the sensor encapsulation. To address these issues, we introduce a tri-gate SJGFET (Tri-SJGFET) in this section with the SJG formed on both the top surface and the two sidewalls of the SiNW channel. The Tri-SJGFET is demonstrated to exhibit enhanced gate control over the SiNW channel, which is investigated in detail in **paper IV**. 3D sketches of a Top-SJGFET and a Tri-SJGFET are shown in Figure 4.8 for comparison.

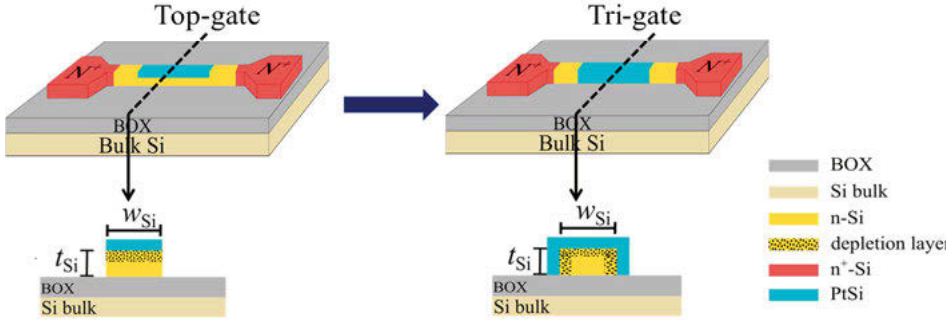

Figure 4.8. 3D sketch of a Top-SJGFET (left) and a Tri-SJGFET (right) along with the respective cross-section of the gated SiNW section with the depletion layer illustrated as the yellow dotted region.

4.2.1. Fabrication of Tri-SJGFETs

The Tri-SJGFETs were fabricated with a process flow similar to that for the Top-SJGFETs except for the step to form the Schottky gate junction. Meanwhile, N_D in the SiNW channel was increased from 1.2×10^{17} to 2.3×10^{17} cm^{-3} for Tri-SJGFETs in order to lower V_{TH} and enlarge the operation window, according to Eq. 4.1. As illustrated in Figure 4.9, a two-step evaporation process was employed to form the tri-gate structure on a SiNW channel. In detail, the substrate was tilted clockwise by 60 °C for the first Pt evaporation and then anti-clockwise for 60 °C for the second Pt evaporation to ensure a conformal Pt coverage on the sidewalls of the SiNW channel.

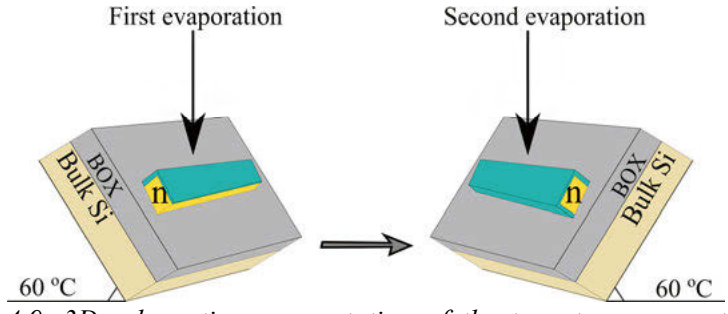

Figure 4.9. 3D schematic representation of the two-step evaporation employed with substrate tilting for tri-gate formation on the SiNW channel.

Tri-SJGFETs with three different channel widths, w_{Si}, *i.e.*, 120 nm, 180 nm, and 480 nm, are fabricated to cover the range from narrow to wide channel conditions, and hereafter are referred to as SJG120, SJG180, and SJG480, respectively.

4.2.2. DC characterization of Tri-SJGFETs

If the Tri-SJGFET has a wide channel with $w_{Si} \gg t_{si}$, for example SJG480, it can be treated as a Top-SJGFET since the full depletion of the SiNW channel can be only achieved from the top therefore V_{TH} can still be calculated by Eq 4.1. On the other hand, for a narrow and tall channel Tri-SJGFET ($w_{Si} \ll t_{si}$) whose channel depletion predominantly occurs from the two sides like SJG120, the following expression applies:

$$V_{TH} = \Phi_B - \frac{(E_C - E_F)}{q} - \frac{qN_D(w_{Si}/2)^2}{2\varepsilon_{Si}}. \quad (4.6)$$

Transfer curves of the three Tri-SJGFETs measured at different V_{sub} are depicted in Figure 4.10(a)-(c). Channel depletion from the two sides is evident since positive V_{TH} shift is observed with decreasing w_{si}. As seen in Figure 4.10, V_{sub} modulation of V_{TH} is greatly reduced for the Tri-SJGFETs with narrower channels, which confirms the enhanced electrostatic control over the SiNW channel by the 3D SJG configuration. Such enhanced gate coupling is further supported by the weakened dependence of *SS* on V_{sub} for the Tri-SJGFET with smaller w_{si}. More detailed analysis of the top-bottom gate coupling effect on LFN as well as the advantageous properties of such 3D SJG can be found in **Paper V**.

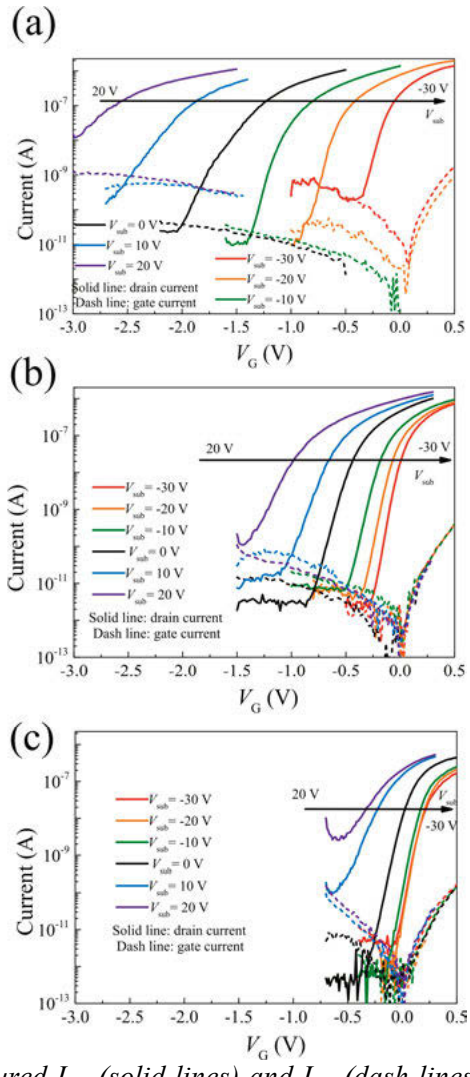

Figure 4.10. Measured I_{DS} (solid lines) and I_{GS} (dash lines) as a function of V_G for SJG480 (a), SJG180 (b) and SJG120 (c) with V_{sub}=-30 (red), -20 (orange), -10 (green), 0 (black), 10 (blue) and 20 V (violet). All plots have the same X and Y scales.

4.2.3. LFN characterization of Tri-SJGFETs

LFN of the three Tri-SJGFETs are comprehensively assessed to demonstrate the beneficial effects of enhanced electrostatic control by the 3D SJG. As shown in Figure 4.11(a), $A \times \overline{v_T^2}$ of SJG480 is strongly dependent on V_{sub} as its carrier concentration and current distribution in the SiNW channel is expected to be mainly controlled by the vertical electrical field from the top SJG in analogy to the Top-SJGFETs. As w_{Si} decreases, depletion from the

two side SJGs becomes increasingly predominant, therefore $A \times \overline{v_T^2}$ does not vary so much as that of SJG480 since the ability of V_{sub} to modulate the current distribution in the SiNW channel becomes weakened. In particular, as shown in Figure 4.11(c), SJG120 with w_{Si} of 120 nm exhibits a greatly reduced span of $A \times \overline{v_T^2}$. As further confirmed by device simulations in Figure 4.12, the low $A \times \overline{v_T^2}$ observed for SJG120 in a large V_{sub} window arises from its capability to confine the conduction in the SiNW bulk. This demonstrates the advantageous properties of Tri-SJGFETs over the Top-SJGFETs for future robust low-noise nanoscale sensor applications.

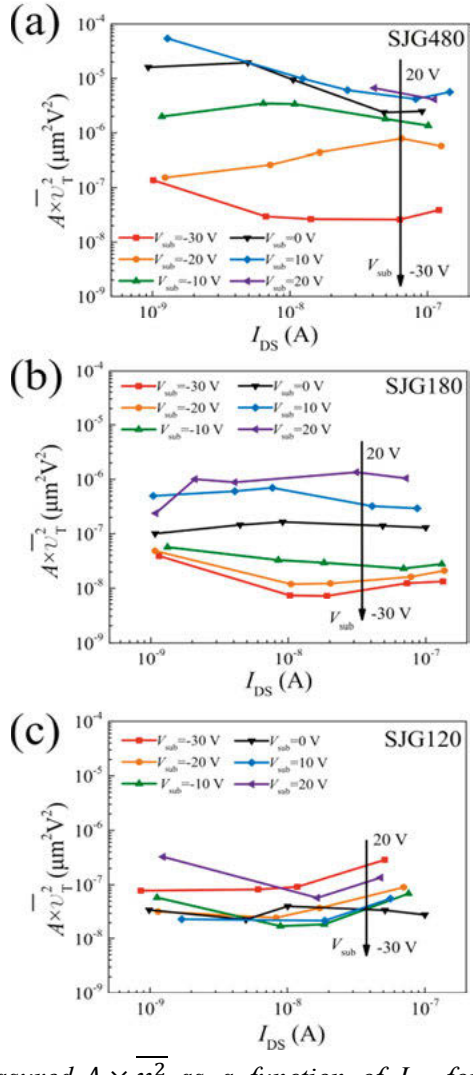

Figure 4.11. Measured $A \times \overline{v_T^2}$ as a function of I_{DS} for (a) SJG480, (b) SJG180, and (c) SJG120 at different V_{sub}. All plots have the same X and Y scales.

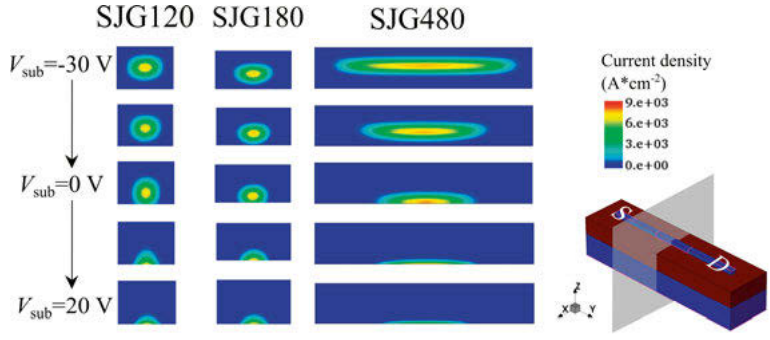

Figure 4.12. Cross-sectional view of simulated current density contours in the SiNW channel for SJG120, SJG180 and SJG480 at different V_{sub} but at the same I_{DS} of 100 nA. A 3D schematic of a Tri-SJGFET structure used in the simulation is shown to the left, where the current density data are taken from the gray X-Z panel.

A comparison between the minimum $A \times \overline{v_T^2}$ of Top-SJGFETs and Tri-SJGFETs can be found in Figure 4.13. The slight variation between the two types of SJGFETs can be ascribed to the different BOX/silicon interface qualities since they are fabricated on different SOI wafers.

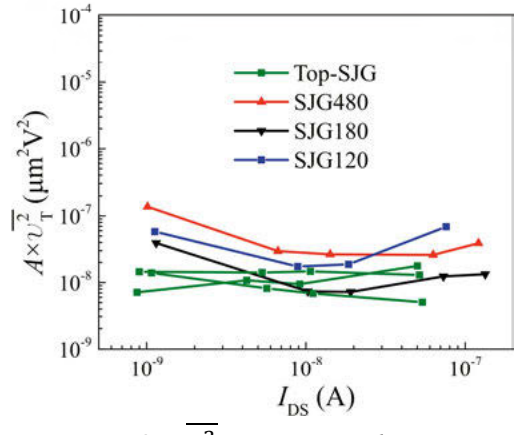

Figure 4.13. The minimum $A \times \overline{v_T^2}$ comparison between Top-SJGFETs and Tri-SJGFETs.

4.3. Operation of SJGFETs in electrolyte

For biosensor applications, the SJGFET should be able to operate in electrolyte with its metal gate replaced by the electrolyte containing targets of interest. First of all, the wire leads should be properly passivated to avoid leakage current through the electrolyte. To maintain the excellent SJG coupling,

it is essential to avoid the electrolyte being in contact with PtSi-free region of the SiNW where the electrolyte can also have gating effect, thus forming parasitic MOS channels. In this respect, Tri-SJGFETs are advantageous as the sidewalls of the SiNW channel are also wrapped by PtSi. Indeed, the Top-SJGFETs show *SS* up to 200 mV/dec when they are operating in electrolyte. Such degradation is likely due to the formation of parasitic MOS channels along the SiNW sidewalls which are covered by SiO_2.

After formation of PtSi SJG, firstly a 3-nm ALD HfO_2 was grown on the SiNW channel as well as the S/D terminals. Then a layer of UV5 (DUV positive tone photoresist) was spin-coated and subsequently patterned by EBL to form a trench of about 100 nm wide centered on the gated section of the SiNW. The trench in the UV5 resist allows the electrolyte to be in contact only with the PtSi-gated section, as shown by the TVSEM image in Figure 4.14(a). The quality of the passivation resist is critical as poor passivation will allow the electrolyte to penetrate through the resist and gate the PtSi-free region of the SiNW, forming parasitic MOS channels. For example, when poly(methyl methacrylate (PMMA) resist was used for passivation, the Tri-SJGFET exhibited a *SS*~200 mV/dec because the PMMA film is much thinner than UV5 film.

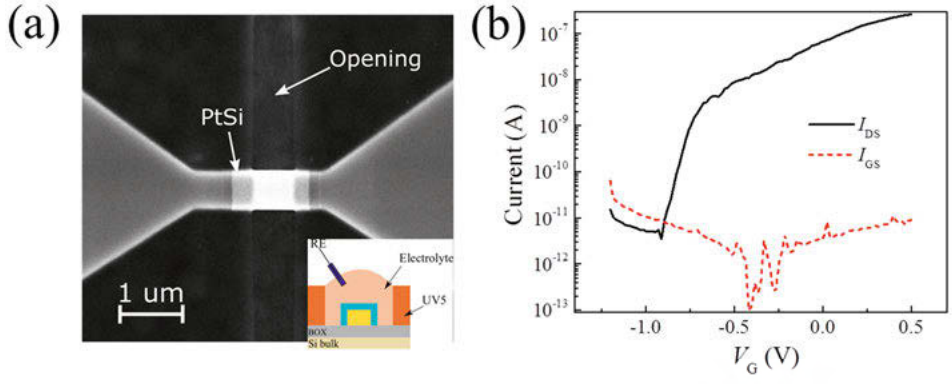

Figure 4.14. (a) TVSEM image of a Tri-SJGFET after passivation with resist, insert: cross-sectional sketch of the Tri-SJGFET in electrolyte. (b) Transfer characteristic of the Tri-SJGFET measured in a buffer solution with pH=7, V_{sub}=0 V.

Transfer characteristic of the Tri-SJGFET (w_{Si}=120 nm) measured in a buffer solution (*p*H=7) is depicted in Figure 4.14(b). During the measurement, V_G is supplied via an Ag/AgCl reference electrode inserted into the buffer solution. The Tri-SJGFET exhibits a near-ideal *SS* of 66.4 mV/dec and low leakage current, indicating high quality passivation as well as that the solution is in reliable contact with the SiNW channel through the trench.

LFN of the Tri-SJGFET is measured and $A \times \overline{v_T^2}$ is plotted in Figure 4.15, in comparison to different FETs measured under dry condition. For the Tri-SJGFET operating in the buffer solution, only the PtSi area which is exposed to the solution is counted for LFN normalization. The Tri-SJGFET exhibit significantly higher $A \times \overline{v_T^2}$ in the buffer solution compare to typical $A \times \overline{v_T^2}$ of Tri-SJGFETs measured under dry condition while it is at the same level as those measured on the MOS-type SiNWFETs. Such increase in noise is probably due to the interaction between HfO_2 and ions in the solution. Further investigation is required to fully understand the effect of such interaction on the sensor noise.

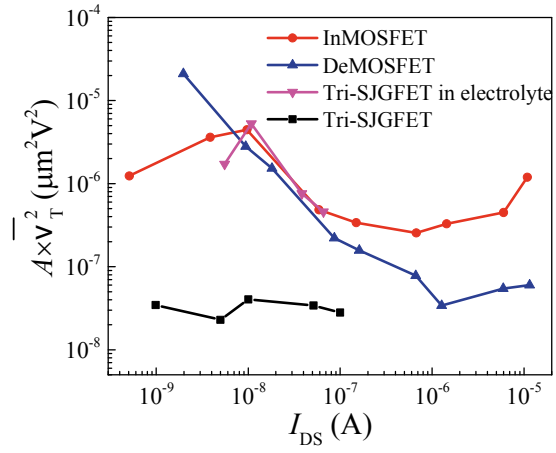

Figure 4.15. $A \times \overline{v_T^2}$ as a function of I_{DS} for the Tri-SJGFET measured in buffer solution, in comparison to SJG120 (V_{sub}=0 V), an InMOSFET, and a DeMOSFET measured under dry condition with a top metal gate.

5. Lateral Bipolar Junction Transistor as a Local Signal Amplifier

Apart from intrinsic device noise, SiNWFET sensors are also vulnerable to external interference, *i.e.*, environmental noise, which mostly spans in the same frequency domain as the biomedical signals [100]. Such noise can be easily picked up by the long metal wiring of the sensors and is detrimental to overall SNR. Figure 5.1 shows the drain current noise PSD, S_{id}, of a MOSFET measured in a well-shielded test fixture (black curves) and in open environment (red curves). The influence of environmental noise generated from large power sources, *e.g.*, heaters and oven, in the laboratory is evident as high noise peaks are observed around 50 Hz especially at low I_{DS}.

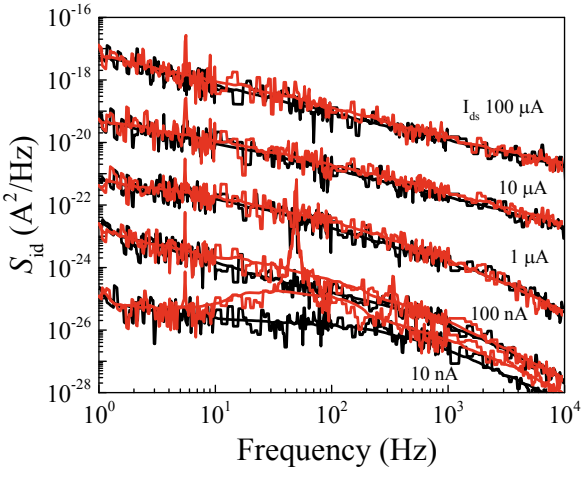

Figure 5.1 LFN of a MOSFET measured in a well-shielded test fixture (black) and in open environment (red).

SiNWFETs normally operate at lower I_{DS} comparing to planar devices due to their much narrower channel. Therefore they are more vulnerable to environmental noise. It has been demonstrated previously that integration of a vertical bipolar junction transistor (VBJT) for immediate sensor current amplification can significantly suppress the environmental noise, leading to greatly improved SNR [101]. However, it is challenging to integrate a VBJT with a SiNWFET because the SiNWFET is fabricated on a SOI substrate

while a VBJT can require Si of micrometers in thickness. Under such circumstances, a lateral version of BJT (LBJT) is proposed since it shares the same fabrication process as that for the SiNWFET sensors.

3D schematic of an LBJT is shown in Figure 5.1(a). The LBJT is NPN-type and symmetric, consisting of heavily *n*-doped emitter/collector (E/C) and moderately *p*-doped base (B). Precise control of base width (W_B) of the LBJT down to less than 50 nm during fabrication is critical for achieving large current gain (β). Meanwhile, alignment of poly-Si contact to the base region should achieve 20 nm in accuracy to avoid short-circuiting between the E/C and poly-Si base contact. Furthermore, two boron implantations are employed for base doping so that there are boron peaks near both top and bottom oxide/silicon interfaces to reduce the interface recombination current. XTEM image of a fully-processed LBJT and a zoom-in view of the base region are shown in Figure 5.2(b). More detailed process description can be found in **paper VI**.

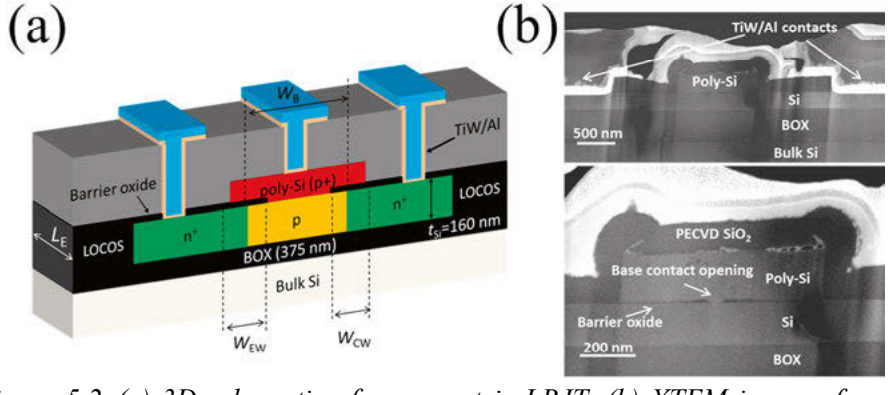

Figure 5.2. (a) 3D schematic of a symmetric LBJT, (b) XTEM image of an LBJT (top) and the zoom-in view of the base region (bottom). Adapted with permission from [102]. *Copyright (2018) IEEE.*

Typical Gummel characteristics and β for an LBJT is shown in Figure 5.3. A peak β over 50 is achieved. Figure 5.4(a) shows the possible integration scheme of an LBJT with a SiNWFET. In the design, source terminal of the SiNWFET will be connected to the base of the LBJT via short poly-Si line to minimize the coupling of environmental noise before amplification. Input referred base current (I_B) noise PSD *i.e.*, S_{ibase}, is further characterized to explore the potential of the LBJT as local signal amplifier for SiNWFETs, which requires S_{ibase} of the LBJT to be lower than S_{id} of the SiNWFETs originated from I_{DS} fluctuations, preferably with a large margin. Again, "total base noise current", *i.e.*, i_{TB}^2, is calculated by integrating S_{ibase} from 1 to 500 Hz, the same noise data process procedure applied on the previous SiNWFETs [103]. In Fig. 5.4(b), i_{TB}^2 of LBJTs are compared with the total noise

current $\overline{i_T^2}$ of different SiNWFETs, *i.e.*, InMOSFETs, DeMOSFETs, and SJGFETs. i_{TB}^2 of LBJTs is about two orders of magnitudes lower than i_T^2 of the SiNWFETs. Therefore, the additional noise introduced by LBJTs during amplification of SiNWFETs signal can be negligible.

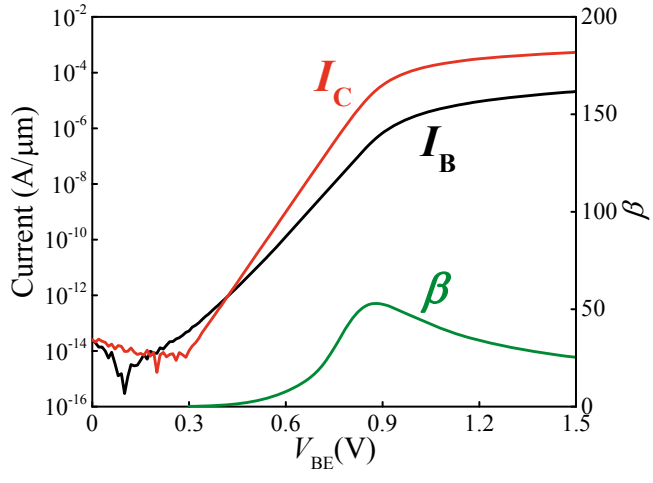

Figure 5.3. Gummel characteritics and β for an LBJT with W_B of ~100 nm, V_{CE}=1 V and V_{sub}=0V. Adapted with permission from [102]. *Copyright (2018) IEEE.*

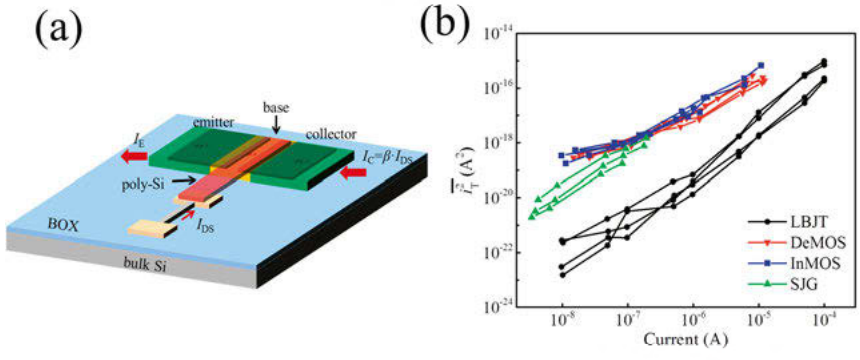

Figure 5.4. (a) Schematics showing the integration of an LBJT with a SiNWFET for local current amplification, (b) comparison of i_{TB}^2 for LBJTs and i_T^2 for InMOSFETs, DeMOSFETs, and SJGFETs. Adapted with permission from [102]. *Copyright (2018) IEEE.*

6. Conclusions and Future Perspectives

As elaborated in the Introduction, the ultimate goal of my work is to develop SiNWFET sensors with high SNR capable of resolving the tiny signal associated with discrete biomolecular interactions. This thesis mainly focuses on addressing the noise issue of MOS-type SiNWFET sensors by implementing a silicide/silicon Schottky junction gate to replace the noisy oxide/silicon interface. The major finds of this thesis are summarized below:

1. A robust CMOS-compatible process was developed to fabricate SiNWFETs with sub-10 nm SiNW channel. The process employed a mixed-lithography combining EBL and photo-lithography to define SiNW channel and large contact pads, respectively, to improve throughputs. During the development, it was found that fine 10 nm resist lines with an unchanged LER can be manufactured even with HSQ expired for 10 months. Such aging effect could increase the sensitivity of HSQ and therefore lead to decrease in exposure dose, which is beneficial in terms of exposure throughput particularly for ultrafine structures. The HSQ aging process can be well described by the Avrami model with the assumption of molecule clustering and cluster aggregating.

2. Proof-of-concept multiplexed ion detections were demonstrated with array of SiNWFET sensors. The sensor array could simultaneously detect both molecular and elemental ions in a single analyte solution. For this study, the SiNWFETs were functionalized with ionophore-doped membranes which greatly simplified the integration process. When operated separately, the sensors showed a near-Nerstian response in wide concentration ranges and the molecular ion sensor showed excellent selectivity against common interfering elemental ions. However, the elemental ion sensor was more susceptible to the presence of molecular ions due to the partitioning of hydrophobic molecular ions into the sensing membrane.

Further membrane optimization with PEG doping could potentially reduce the hydrophobicity of the membrane so that the elemental ion sensor could become more stable in the presence of molecular ions.

3. To reduce the intrinsic noise of MOS-type SiNWFETs and improve SNR, a silicide/silicon Schottky junction gate was proposed to replace the conventional oxide/silicon gating interface of the SiNWFET. The resultant SJGFETs showed a close-to-ideal gate coupling efficiency and significantly reduced LFN as compared to reference InMOSFETs and DeMOSFETs with HfO_2 as the gate oxide. In addition, the LFN of the SJGFETs could be fur-

ther improved by pushing the conduction channel away from the noisy BOX/silicon interface, *i.e.*, deep into the bulk of the SiNW channel. The SJGFETs are fabricated with standard silicon fabrication technology and can easily be adapted to FET fabrication with other semiconductors than silicon.

4. The SJGFETs were further optimized by implementing a 3D Schottky junction gate wrapping both top and sidewalls of the SiNW channel. The tri-gate SJGFETs with optimized geometry exhibited significantly enhanced electrostatic control over the channel, and could confine the I_{DS} in the SiNW bulk, making LFN performance less susceptible to traps in the remaining bottom BOX/silicon interface. Therefore, an optimal LFN can be achieved without the need of an additional V_{sub}, which is essential for high density sensor integration as individual tuning of LFN performance is no longer needed.

5. Symmetric LBJTs were fabricated on SOI wafers using the standard CMOS process, and were optimized for application as local current amplifier for SiNWFET sensors, with a β_{max} over 50 achieved with good reliability. Noise comparison between the LBJTs and SiNWFETs further demonstrated that applying LBJT as signal amplifier won't generate additional noise on top of the SiNWFET intrinsic noise.

To achieve the aforementioned goal, much more needs to be done with some of the efforts suggested as follows:

1. It is evident that the BOX/silicon interface is still a main noise contributor in the SJGFETs. Fabricating SJGFETs on a SOI wafer with high quality BOX/silicon interface, or even with an all-around Schottky junction gate completely eliminating all the oxide/silicon interfaces, could potentially further reduce the intrinsic device noise of SJGFETs.

2. The SJGFETs should be systematically evaluated towards their operation in electrolyte, including passivation quality, gate coupling, and possible formation of parasitic MOS channels.

3. LFN contributions from the solid/electrolyte interface should be investigated when the SJGFETs is operating in electrolyte. It would be interesting to study the magnitude and scaling behavior of such LFN, in comparison to the intrinsic LFN of the SJGFETs.

4. The low noise SJGFET can be further integrated with LBJT local signal amplifier to improve its immunity against external noise interference.

Sammanfattning på svenska

Under de senaste decennierna har fälteffekttransistorer baserade på kiselnanotrådar (SiNWFETs) visat sig vara en överlägsen plattform för etikettfria, mycket känsliga realtidsdetekteringar av kemiska och biologiska ämnen. Eftersom SiNWFETs har en avsevärt bättre laddningskänslighet jämfört med plana fälteffekttransistorer (FETs), så är de särskilt lämpade för applikationer som riktar sig mot analyt med ultralåga koncentrationer eller till och med aktiviteter på enmolekylnivå. I en SiNWFET-sensor kan elektriska potentialförändringar förknippade med laddning och molekylära rörelser i närheten av SiNW-kanalen effektivt påverka den underliggande kanalen och modulera drain-source strömmen (I_{DS}) hos SiNWFET, vilket alstrar en detekterande signal som kan avläsas. Denna detekterande signal bestäms primärt av ytegenskaperna hos det detekterande skiktet på gate-anslutningen. Höga känsligheter nära Nernst-gränsen, 60 mV/dec (förändring av analytkoncentration) vid rumstemperatur har redan visats med olika detekterande skikt. För att uppnå ett högt signal-till-brus förhållande (SNR) för detektering vid ovannämnda krävande situationer är det därför nödvändigt att SiNWFET komponenterna har lågt brus där instrinsiskt komponentbrus är en av huvudkomponenterna. Det är väl förstått att processen för infångande/frisläppande av laddningsbärare vid gränssnittet vid gateoxiden och halvledaren är orsaken till fluktuationerna hos I_{DS}, det vill säga det intrinsiska komponentbruset i fälteffekttransistorer baserade på metall-oxid-halvledare (MOSFETs). Detta komponentbrus är omvänt proportionellt mot komponentarean. Nedskalning av SiNWFET som syftar till förbättrad laddningskänslighet leder oundvikligen till en dramatisk ökning av brusets intensitet. Denna avhandling presenterar en omfattande studie av design, tillverkning och optimering av brusprestanda för SiNWFET-baserade sensorer, och en ny design för gaten vid Schottkyövergången är föreslagen och demonstrerad för applikationer med låg brusnivå.

Först utvecklades en robust process som är kompatibel med komplementär metall oxid halvledere (CMOS) för att framställa SiNWFETs med SiNW-kanaler under 10 nm. Processen nyttjade en blandad litografi som kombinerade elektronstrålelitografi och optisk litografi för att definiera SiNW-kanalen och stora kontaktpaddar, för att förbättra genomströmningar.

För att bevisa konceptet vid en demonstrationdetektering, tillverkades en uppsättning av SiNW-MOSFET-sensorer som applicerades för multiplex jondetektering med nyttjande av jonofordopad blandmatrismembran som det

detekterande skiktet, vilket väsentligt förenklade integrationsprocessen. Sensoruppsättningen kunde samtidigt detektera både molekylära och enstaka joner i en enda analytlösning. När de användes separat uppvisade sensorerna prestanda nära Nerstiangränsen inom stora koncentrationsområden och molekyljonjonssensorn uppvisade utmärkt selektivitet mot vanliga störande elementära joner. Elementärjonsensorn var emellertid mer mottaglig för närvaron av molekylära joner på grund av partitioneringen av hydrofoba molekyljoner i detekteringsmembranet.

För att ta itu med det grundläggande brusproblemet hos SiNW-MOSFET-sensorerna, konstruerades SiNWFETs (SJGFET) som kontrollerades av en Schottkyövergång, där det brusiga gränssnitten mellan gateoxid och kisel hos den konventionella SiNWFET-komponenten ersattes av en Schottky (PtSi/kisel) övergång på toppen av SiNW-kanalen. Den resulterande toppgate SJGFET-komponenten uppvisade nära ideal gatekopplingseffektivitet (60 mv/dec) och markant reducerat komponentbrus jämfört med referenskomponenterna som var SiNWFETs av MOS-typ. Och denna toppgate SJGFET-komponent uppvisade ett mycket starkt brusberoende på substratförspänningen (V_{sub}). Det lågfrekventa bruset (LFN) för SJGFET-komponenten kunde förbättras ytterligare genom att trycka ledningskanalen bort från det brusiga gränssnittet mellan den begravda oxiden (BOX) och kislet, dvs djupt in i bulken för SiNW-kanalen.

För att förbättra Schottkyövergångens kontroll över SiNW-kanalen utfördes ytterligare SJGFET-optimering genom att använda en 3-dimensionell Schottkyövergång-gate som bredde ut sig både både på topp- och sidoväggarna på SiNW-kanalen. Tri-gate SJGFET-komponenterna med optimerad geometri uppvisade signifikant förbättrad elektrostatisk kontroll över kanalen och kan hålla kvar I_{DS} inne i SiNW-bulken, vilket gör LFN-prestandan mindre mottaglig för fällor i det återstående bottengränsskiktet mellan BOX och kisel. Därför kan en optimal LFN uppnås utan att behöva en ytterligare V_{sub} vilket är nödvändigt för sensor-integration med hög densitet eftersom individuell avstämning av LFN-prestanda inte längre behövs. Således kan kombinationen av vår lågbrusiga tri-gate SJGFET-komponent med en yta med prestanda nära Nernst-gränsen vara en lovande lösning för framtida robusta lågbrusiga nanosensorer. Dessutom undersöktes systematiskt effekten av gränssnittet BOX/kisel på lutningen under tröskelvärdet (SS) och LFN för SJGFETs. För att bevisa konceptet vid en demonstrationdetektering, var denna tri-gate SJGFET passiverad och testad i lösningar för att undersöka dess brusegenskaper.

Vidare tillverkades symmetriska laterala bipolära transistorer (LBJT) på kisel-på-isolatorskivor med den standardmässiga CMOS processen och optimerades för att fungera som lokal strömförstärkare för SiNWFET-sensorerna med en strömförstärkning över 50 vilket erhölls med god tillförlitlighet. Denna interna signalförstärkningen förväntas väsentligt undertrycka miljöinterferensen och förbättra övergripande SNR speciellt vid låga sensor-

strömmar. Brusjämförelse mellan LBJT och SiNWFET visade vidare att nyttjandet av LBJT som signalförstärkare inte kommer att generera ytterligare brus ovanpå det intrinsiska bruset i SiNWFET.

Konceptet som demonstreras i denna avhandling är inte begränsat till nanotrådsgeometrin och kan lätt anpassas till FET-tillverkning med andra halvledare än kisel.

Acknowledgement

Foremost, I would like to express my sincere gratitude and appreciation to my supervisor Professor Zhen Zhang for offering me this opportunity to come to Sweden and start my PhD study and research in such interesting field, and also giving me so much guidance throughout my PhD life. Also, many thanks go to Professor Shi-Li Zhang, my co-supervisor, who infected me by his enthusiasm and inspired me by his immense knowledge.

I am particularly grateful for the assistance given by Dr. Si Chen, also my co-supervisor, for the continuous support. Thank you for always being patient with my questions and responding to me generously. Your intelligence and experience has guided me through all the time of research and writing of this thesis.

I'd like to thank Dr. Paul Solomon for your patience and insightful comments on my work. Discussing with you has been so much pleasure and full of flashes of wit.

I would also like to offer my special thanks to Dr. Tao Zhang for his generous assistance and continuous help with EBL all the time. Your knowledge has contributed greatly to my Ph.D work.

Many thanks are given to Dr. Örjan Vallin, Amit Patel, Rimantas Brucas, and Farhad Zamany and other MSL staffs who kindly offered me help when I got troubles in the cleanroom, and for your fruitful discussions. Thanks also go to Docent Per-Erik Hellström and Dr. Yongbin Wang for all the supports in Electrum laboratory.

A very deep gratitude goes out to all former and current group members. Thank Da Zhang for sharing so many experiences with me when I first joined the group. Thank Lukas Jablonka for your company and all the stimulating discussions. Thanks to Chenyu Wen, Xingxing Xu, Shuangshuang Zeng, Qitao Hu, Yifei Liu, Yingtao Yu, for your feedback, cooperation and all the fun we have had in past years.

I also want to thank Dr. Asta Makaravičiūtė and Dr. Nathan Netzer for every positive comment and warm encouragement. Thank Dr. Indrek Must, Dr.

Chiao-Wei Tseng, Dr. Umut Cindemir and Dr. Quentin Palomar for your inspiring discussions.

Thank Professor Charlotte Platzer Björkman for your precious time to screen the thesis and give me concrete and useful comments and suggestions for improvement. Thank Docent Tomas Nyberg for translating the summary for my thesis.

Thank Ramy Salameh for all your administrative help.

Thanks to Man Song, Malkolm Hinnemo, Patrik Ahlberg, Katharina Rudisch, Yi Ren for your company in the division and all the joy you brought.

I want to thank all my Chinese friends in Sweden with a special mention to Yuan Xie for taking me in like a family when I first came to Sweden. You kindness and warm-hearted spirit is remarkable. Also many thanks to my friends, Jie Zhao, Huan Wang, Shiyu Li, Jie Ren, Yihua Zha, Peng Zhang, Yan Guo, Xiaowen Li, Shuyi Li, Mingzhi Jiao, Jing Ma for spending such fun time with me.

Thanks to Knut Graw for being a language partner with me. So much time was spent on practicing English and it did work out well.

Many thanks to all the girls of Jennys Änglar! I enjoy your company as much as all the trainings. Your kindness and positive attitude has cheered me up so many times in the last period of my Ph.D life.

At last, I would like to thank my dear family for supporting me spiritually throughout my Ph.D. and my life in general. 感谢爸爸妈妈对我一直以来的支持。这一段人生之路不仅对我，对你们也是一段挑战，以后的路我们也会携手并进，分享痛苦，也分享快乐，谢谢你们。

Xi Chen
陈希
April. 2019

References

[1] "WHO | Early Diagnosis and Screening," *WHO*. [Online]. Available: http://www.who.int/cancer/prevention/diagnosis-screening/en/. [Accessed: 08-Mar-2019].

[2] J. Newquist, "Importance of an early diagnosis." [Online]. Available: https://www.alzwisc.org/Importance%20of%20an%20early%20diagnosis.htm. [Accessed: 08-Mar-2019].

[3] S. O. Kelley, "What Are Clinically Relevant Levels of Cellular and Biomolecular Analytes?," *ACS Sens.*, vol. 2, no. 2, pp. 193–197, Feb. 2017.

[4] P. Yager, G. J. Domingo, and J. Gerdes, "Point-of-Care Diagnostics for Global Health," *Annual Review of Biomedical Engineering*, vol. 10, no. 1, pp. 107–144, 2008.

[5] C. P. Price, "Point of care testing," *BMJ*, vol. 322, no. 7297, pp. 1285–1288, May 2001.

[6] V. Gubala, L. F. Harris, A. J. Ricco, M. X. Tan, and D. E. Williams, "Point of Care Diagnostics: Status and Future," *Analytical Chemistry*, vol. 84, no. 2, pp. 487–515, Jan. 2012.

[7] D. A. Giljohann and C. A. Mirkin, "Drivers of biodiagnostic development," *Nature*, vol. 462, pp. 461–464, Nov. 2009.

[8] J. Wang, "Electrochemical biosensors: Towards point-of-care cancer diagnostics," *Biosensors and Bioelectronics*, vol. 21, no. 10, pp. 1887–1892, Apr. 2006.

[9] W. Gao *et al.*, "Fully integrated wearable sensor arrays for multiplexed in situ perspiration analysis," *Nature*, vol. 529, no. 7587, pp. 509–514, Jan. 2016.

[10] P. Bühlmann and L. D. Chen, "Ion-Selective Electrodes With Ionophore-Doped Sensing Membranes," in *Supramolecular Chemistry*, John Wiley & Sons, Ltd, 2012.

[11] C. Toumazou and P. Georgiou, "Piet Bergveld - 40 years of ISFET technology: From neuronal sensing to DNA sequencing," *Electronics Letters*, vol. 47, no. 26, p. S7, 2011.

[12] P. Bergveld, "The operation of an ISFET as an electronic device," *Sensors and Actuators*, vol. 1, pp. 17–29, Jan. 1981.

[13] "ISFET, Theory and Practice." [Online]. Available: https://resourcecenter.ieee-sensors.org/education/tutorials/SCTUT00-20.html. [Accessed: 08-Mar-2019].

[14] J. M. Rothberg *et al.*, "An integrated semiconductor device enabling non-optical genome sequencing," *Nature*, vol. 475, no. 7356, pp. 348–352, Jul. 2011.

[15] L. Mu, Y. Chang, S. D. Sawtelle, M. Wipf, X. Duan, and M. A. Reed, "Silicon Nanowire Field-Effect Transistors;A Versatile Class of Potentiometric Nanobiosensors," *IEEE Access*, vol. 3, pp. 287–302, 2015.

[16] N. Clément, K. Nishiguchi, J. F. Dufreche, D. Guerin, A. Fujiwara, and D. Vuillaume, "A silicon nanowire ion-sensitive field-effect transistor with elementary charge sensitivity," *Applied Physics Letters*, vol. 98, no. 1, p. 014104, 2011.
[17] G. He, J. Li, H. Ci, C. Qi, and X. Guo, "Direct Measurement of Single-Molecule DNA Hybridization Dynamics with Single-Base Resolution," *Angewandte Chemie International Edition*, vol. 55, no. 31, pp. 9036–9040, Jul. 2016.
[18] J. Li *et al.*, "Direct real-time detection of single proteins using silicon nanowire-based electrical circuits," *Nanoscale*, vol. 8, no. 36, pp. 16172–16176, 2016.
[19] P. R. Nair and M. A. Alam, "Performance limits of nanobiosensors," *Applied Physics Letters*, vol. 88, no. 23, p. 233120, 2006.
[20] R. E. G. van Hal, J. C. T. Eijkel, and P. Bergveld, "A novel description of ISFET sensitivity with the buffer capacity and double-layer capacitance as key parameters," *Sensors and Actuators B: Chemical*, vol. 24, no. 1–3, pp. 201–205, Mar. 1995.
[21] M. Wipf *et al.*, "Selective Sodium Sensing with Gold-Coated Silicon Nanowire Field-Effect Transistors in a Differential Setup," *ACS Nano*, vol. 7, no. 7, pp. 5978–5983, Jul. 2013.
[22] G.-J. Zhang, A. Agarwal, K. D. Buddharaju, N. Singh, and Z. Gao, "Highly sensitive sensors for alkali metal ions based on complementary-metal-oxide-semiconductor-compatible silicon nanowires," *Applied Physics Letters*, vol. 90, no. 23, p. 233903, 2007.
[23] A. Cao *et al.*, "Metal–Organic Polyhedra-Coated Si Nanowires for the Sensitive Detection of Trace Explosives," *Nano Lett.*, vol. 17, no. 1, pp. 1–7, Jan. 2017.
[24] R. Stoop *et al.*, "Implementing Silicon Nanoribbon Field-Effect Transistors as Arrays for Multiple Ion Detection," *Biosensors*, vol. 6, no. 2, p. 21, May 2016.
[25] M. Wipf *et al.*, "Potassium sensing with membrane-coated silicon nanowire field-effect transistors," in *2013 Transducers & Eurosensors XXVII: The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII)*, 2013, pp. 1182–1185.
[26] N. L. Netzer, I. Must, Y. Qiao, S.-L. Zhang, Z. Wang, and Z. Zhang, "Biomimetic supercontainers for size-selective electrochemical sensing of molecular ions," *Sci Rep*, vol. 7, p. 45786, 10 2017.
[27] E. Bakker, P. Bühlmann, and E. Pretsch, "Carrier-Based Ion-Selective Electrodes and Bulk Optodes. 1. General Characteristics," *Chem. Rev.*, vol. 97, no. 8, pp. 3083–3132, Dec. 1997.
[28] A. Cao, M. Mescher, D. Bosma, J. H. Klootwijk, E. J. R. Sudhölter, and L. C. P. M. de Smet, "Ionophore-Containing Siloprene Membranes: Direct Comparison between Conventional Ion-Selective Electrodes and Silicon Nanowire-Based Field-Effect Transistors," *Analytical Chemistry*, vol. 87, no. 2, pp. 1173–1179, Jan. 2015.
[29] M. B. Ali, R. Kalfat, H. Sfihi, J. M. Chovelon, H. B. Ouada, and N. Jaffrezic-Renault, "Sensitive cyclodextrin–polysiloxane gel membrane on EIS structure and ISFET for heavy metal ion detection," *Sensors and Actuators B: Chemical*, vol. 62, no. 3, pp. 233–237, Mar. 2000.
[30] M.-Y. Shen, B.-R. Li, and Y.-K. Li, "Silicon nanowire field-effect-transistor based biosensors: From sensitive to ultra-sensitive," *Biosensors and Bioelectronics*, vol. 60, pp. 101–111, Oct. 2014.

[31] P. Bergveld, “Thirty years of ISFETOLOGY: What happened in the past 30 years and what may happen in the next 30 years,” *Sensors and Actuators B: Chemical*, vol. 88, no. 1, pp. 1–20, 2003.
[32] B. Tian, T. Cohen-Karni, Q. Qing, X. Duan, P. Xie, and C. M. Lieber, “Three-Dimensional, Flexible Nanoscale Field-Effect Transistors as Localized Bioprobes,” *Science*, vol. 329, no. 5993, pp. 830–834, Aug. 2010.
[33] X. Chen *et al.*, “Multiplexed analysis of molecular and elemental ions using nanowire transistor sensors,” *Sensors and Actuators B: Chemical*, vol. 270, pp. 89–96, Oct. 2018.
[34] S. Zafar, C. D’Emic, A. Afzali, B. Fletcher, Y. Zhu, and T. Ning, “Optimization of pH sensing using silicon nanowire field effect transistors with HfO_2 as the sensing surface,” *Nanotechnology*, vol. 22, no. 40, p. 405501, 2011.
[35] L. Mu *et al.*, “Nanoelectronic Platform for Ultrasensitive Detection of Protein Biomarkers in Serum using DNA Amplification,” *Analytical Chemistry*, vol. 89, no. 21, pp. 11325–11331, Nov. 2017.
[36] S. Rigante *et al.*, “Sensing with Advanced Computing Technology: Fin Field-Effect Transistors with High-*k* Gate Stack on Bulk Silicon,” *ACS Nano*, vol. 9, no. 5, pp. 4872–4881, May 2015.
[37] T.-W. Lin *et al.*, “Label-free detection of protein-protein interactions using a calmodulin-modified nanowire transistor,” *Proceedings of the National Academy of Sciences*, vol. 107, no. 3, pp. 1047–1052, Jan. 2010.
[38] D. Zhang *et al.*, “Direct assessment of solid–liquid interface noise in ion sensing using a differential method,” *Applied Physics Letters*, vol. 108, no. 15, p. 151603, Apr. 2016.
[39] J. Li, S. Pud, M. Petrychuk, A. Offenhäusser, and S. Vitusevich, “Sensitivity Enhancement of Si Nanowire Field Effect Transistor Biosensors Using Single Trap Phenomena,” *Nano Lett.*, vol. 14, no. 6, pp. 3504–3509, Jun. 2014.
[40] N. K. Rajan, D. A. Routenberg, and M. A. Reed, “Optimal signal-to-noise ratio for silicon nanowire biochemical sensors,” *Applied Physics Letters*, vol. 98, no. 26, p. 264107, 2011.
[41] E. Simoen and C. Claeys, “The low-frequency noise behaviour of silicon-on-insulator technologies,” *Solid-State Electronics*, vol. 39, no. 7, pp. 949–960, Jul. 1996.
[42] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, “A physics-based MOSFET noise model for circuit simulators,” *IEEE Transactions on Electron Devices*, vol. 37, no. 5, pp. 1323–1333, May 1990.
[43] E. Simoen and C. Claeys, “On the ficker noise in submicron silicon MOSFETs,” p. 18, 1999.
[44] C. G. Theodorou *et al.*, “Low-Frequency Noise Sources in Advanced UTBB FD-SOI MOSFETs,” *IEEE Transactions on Electron Devices*, vol. 61, no. 4, pp. 1161–1167, Apr. 2014.
[45] H. Cho, K. Kim, J.-S. Yoon, T. Rim, M. Meyyappan, and C.-K. Baek, “Optimization of Signal to Noise Ratio in Silicon Nanowire ISFET Sensors,” *IEEE Sensors Journal*, vol. 17, no. 9, pp. 2792–2796, May 2017.
[46] T. Elewa, B. Boukriss, H. S. Haddara, A. Chovet, and S. Cristoloveanu, “Low-frequency noise in depletion-mode SIMOX MOS transistors,” *IEEE Transactions on Electron Devices*, vol. 38, no. 2, pp. 323–327, Feb. 1991.
[47] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3th ed. John Wiley & Sons, 2006.
[48] R. G. Hobbs, N. Petkov, and J. D. Holmes, “Semiconductor Nanowire Fabrication by Bottom-Up and Top-Down Paradigms,” *Chem. Mater.*, vol. 24, no. 11, pp. 1975–1991, Jun. 2012.

[49] "Extreme ultraviolet lithography," *Wikipedia*. 07-Mar-2019.
[50] A. E. Grigorescu and C. W. Hagen, "Resists for sub-20-nm electron beam lithography with a focus on HSQ: state of the art," *Nanotechnology*, vol. 20, no. 29, p. 292001, Jul. 2009.
[51] A. E. Grigorescu, M. C. van der Krogt, and C. W. Hagen, "Sub-10-nm structures written in ultra-thin HSQ resist layers using electron-beam lithography," 2007, p. 65194A.
[52] A. E. Grigorescu, M. C. van der Krogt, C. W. Hagen, and P. Kruit, "10nm lines and spaces written in HSQ, using electron beam lithography," *Microelectronic Engineering*, vol. 84, no. 5–8, pp. 822–824, May 2007.
[53] D. L. Olynick, B. Cord, A. Schipotinin, D. F. Ogletree, and P. J. Schuck, "Electron-beam exposure mechanisms in hydrogen silsesquioxane investigated by vibrational spectroscopy and in situ electron-beam-induced desorption," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 28, no. 3, p. 581, 2010.
[54] M. Häffner *et al.*, "Influence of temperature on HSQ electron-beam lithography," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 25, no. 6, p. 2045, 2007.
[55] J.-H. Zhao *et al.*, "Thermomechanical properties and moisture uptake characteristics of hydrogen silsesquioxane submicron films," *Applied Physics Letters*, vol. 74, no. 7, p. 944, 1999.
[56] C.-C. Yang and W.-C. Chen, "The structures and properties of hydrogen silsesquioxane (HSQ) films produced by thermal curing," *Journal of Materials Chemistry*, vol. 12, no. 4, pp. 1138–1141, Mar. 2002.
[57] D. A. Westly, D. M. Tennant, Y. Aida, H. Ohki, and T. Ohkubo, "Improved time dependent performance of hydrogen silsesquioxane resist using a spin on top coat," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 29, no. 6, p. 06FJ02, 2011.
[58] N. Clark, A. Vanderslice, R. Grove, and R. R. Krchnavek, "Time-dependent exposure dose of hydrogen silsesquioxane when used as a negative electron-beam resist," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 24, no. 6, p. 3073, 2006.
[59] F. C. M. J. M. van Delft, "Delay-time and aging effects on contrast and sensitivity of hydrogen silsesquioxane," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 20, no. 6, p. 2932, 2002.
[60] S. F. A. Rahman, N. A. Yusof, M. N. Hamidon, R. M. Zawawi, and U. Hashim, "Top-down fabrication of silicon nanowire sensor using electron beam and optical mixed lithography," in *Semiconductor Electronics (ICSE), 2014 IEEE International Conference on*, 2014, pp. 64–67.
[61] M. Avrami, "Kinetics of Phase Change. I General Theory," *The Journal of Chemical Physics*, vol. 7, no. 12, p. 1103, 1939.
[62] M. Avrami, "Kinetics of Phase Change. II Transformation-Time Relations for Random Distribution of Nuclei," *Journal of Chemical Physics*, vol. 8, no. 1940, pp. 212–224, 1940.
[63] M. Fanfoni and M. Tomellini, "The Johnson-Mehl-Avrami-Kohnogorov model: A brief review," *Il Nuovo Cimento D*, vol. 20, no. 7–8, pp. 1171–1182, Jul. 1998.
[64] X. Chen, T. Zhang, V. Constantoudis, S.-L. Zhang, and Z. Zhang, "Aged hydrogen silsesquioxane for sub-10nm line patterns," *Microelectronic Engineering*, vol. 163, pp. 105–109, Sep. 2016.
[65] T. H. P. Chang, "Proximity effect in electron-beam lithography," *Journal of Vacuum Science and Technology*, vol. 12, no. 6, p. 1271, Nov. 1975.

[66] P. N. Floriano *et al.*, "Use of Saliva-Based Nano-Biochip Tests for Acute Myocardial Infarction at the Point of Care: A Feasibility Study," *Clin. Chem.*, vol. 55, no. 8, p. 1530, Jul. 2009.
[67] J. M. Klostranec *et al.*, "Convergence of Quantum Dot Barcodes with Microfluidics and Signal Processing for Multiplexed High-Throughput Infectious Disease Diagnostics," *Nano Lett.*, vol. 7, no. 9, pp. 2812–2818, Sep. 2007.
[68] G. Davis, I. R. Lauks, C. Lin, and C. J. Miller, "Apparatus and methods for analyte measurement and immunoassay," U.S. Patent 8,017,382, 02-Sep-2011.
[69] J. Moyer, D. Wilson, I. Finkelshtein, B. Wong, and R. Potts, "Correlation Between Sweat Glucose and Blood Glucose in Subjects with Diabetes," *Diabetes Technology & Therapeutics*, vol. 14, no. 5, pp. 398–402, May 2012.
[70] S. L. Knight, R. P. Taylor, A. A. Polliack, and D. L. Bader, "Establishing predictive indicators for the status of loaded soft tissues," *J Appl Physiol*, vol. 90, no. 6, p. 2231, Jun. 2001.
[71] C. Groussard, I. Morel, M. Chevanne, M. Monnier, J. Cillard, and A. Delamarche, "Free radical scavenging and antioxidant effects of lactate ion: an in vitro study," *Journal of Applied Physiology*, vol. 89, no. 1, pp. 169–175, Jul. 2000.
[72] M. B. Glier, T. J. Green, and A. M. Devlin, "Methyl nutrients, DNA methylation, and cardiovascular disease," *Mol. Nutr. Food Res.*, vol. 58, no. 1, pp. 172–182, Jan. 2014.
[73] R. Schliebs and T. Arendt, "The cholinergic system in aging and neuronal degeneration," *Behavioural Brain Research*, vol. 221, no. 2, pp. 555–563, Aug. 2011.
[74] D. B. Speedy, T. D. Noakes, and C. Schneider, "Exercise-associated hyponatremia: A review," *Emergency Medicine*, vol. 13, no. 1, pp. 17–27, 2001.
[75] M. F. Bergeron, "Heat cramps: fluid and electrolyte challenges during tennis in the heat," *Journal of Science and Medicine in Sport*, vol. 6, no. 1, pp. 19–27, Mar. 2003.
[76] T. Xiao, F. Wu, J. Hao, M. Zhang, P. Yu, and L. Mao, "In Vivo Analysis with Electrochemical Sensors and Biosensors," *Analytical Chemistry*, vol. 89, no. 1, pp. 300–313, Jan. 2017.
[77] P. Bühlmann and L. D. Chen, "Ion-Selective Electrodes With Ionophore-Doped Sensing Membranes," in *Supramolecular Chemistry*, John Wiley & Sons, Ltd, 2012.
[78] P. Uutela, R. Reinilä, P. Piepponen, R. A. Ketola, and R. Kostiainen, "Analysis of acetylcholine and choline in microdialysis samples by liquid chromatography/tandem mass spectrometry," *Rapid Communications in Mass Spectrometry*, vol. 19, no. 20, pp. 2950–2956, 2005.
[79] T. A. Patterson and J. W. Kosh, "Simultaneous quantitation of arecoline, acetylcholine, and choline in tissue using gas chromatography/electron impact mass spectrometry," *Biological Mass Spectrometry*, vol. 21, no. 6, pp. 299–304, 1992.
[80] N. Chauhan, J. Narang, and U. Jain, "Highly sensitive and rapid detection of acetylcholine using an ITO plate modified with platinum-graphene nanoparticles," *The Analyst*, vol. 140, no. 6, pp. 1988–1994, 2015.
[81] F.-R. Dai and Z. Wang, "Modular Assembly of Metal–Organic Supercontainers Incorporating Sulfonylcalixarenes," *J. Am. Chem. Soc.*, vol. 134, no. 19, pp. 8002–8005, May 2012.

[82] F.-R. Dai, U. Sambasivam, A. J. Hammerstrom, and Z. Wang, "Synthetic Supercontainers Exhibit Distinct Solution versus Solid State Guest-Binding Behavior," *J. Am. Chem. Soc.*, vol. 136, no. 20, pp. 7480–7491, May 2014.
[83] N. L. Netzer, F.-R. Dai, Z. Wang, and C. Jiang, "pH-Modulated Molecular Assemblies and Surface Properties of Metal–Organic Supercontainers at the Air–Water Interface," *Angew. Chem. Int. Ed.*, vol. 53, no. 41, pp. 10965–10969, Oct. 2014.
[84] F.-R. Dai, D. C. Becht, and Z. Wang, "Modulating guest binding in sulfonyl-calixarene-based metal–organic supercontainers," *Chem. Commun.*, vol. 50, no. 40, pp. 5385–5387, Apr. 2014.
[85] N. L. Netzer, I. Must, Y. Qiao, S.-L. Zhang, Z. Wang, and Z. Zhang, "Biomimetic supercontainers for size-selective electrochemical sensing of molecular ions," *Scientific Reports*, vol. 7, p. 45786, Apr. 2017.
[86] L. R. Stoop *et al.*, "Implementing Silicon Nanoribbon Field-Effect Transistors as Arrays for Multiple Ion Detection," *Biosensors*, vol. 6, no. 2, 2016.
[87] R. L. Stoop *et al.*, "Competing surface reactions limiting the performance of ion-sensitive field-effect transistors," *Sensors and Actuators B: Chemical*, vol. 220, pp. 500–507, Dec. 2015.
[88] E. Bakker, P. Bühlmann, and E. Pretsch, "Carrier-based ion-selective electrodes and bulk optodes. 1. General characteristics," *Chemical Reviews*, vol. 97, no. 8, pp. 3083–3132, 1997.
[89] S. Ogawara, J. L. Carey, X. U. Zou, and P. Bühlmann, "Donnan Failure of Ion-Selective Electrodes with Hydrophilic High-Capacity Ion-Exchanger Membranes," *ACS Sensors*, vol. 1, no. 1, pp. 95–101, Jan. 2016.
[90] X. Chen, S. Chen, Q. Hu, S.-L. Zhang, P. M. Solomon, and Z. Zhang, "Device noise reduction for silicon nanowire field-effect-transistor based sensors by using a Schottky junction gate," *ACS Sens.*, Jan. 2019.
[91] Z. Zhang, S.-L. Zhang, M. Östling, and J. Lu, "Robust, scalable self-aligned platinum silicide process," *Appl. Phys. Lett.*, vol. 88, no. 14, p. 142114, Apr. 2006.
[92] Z. Zhang *et al.*, "SB-MOSFETs in UTB-SOI Featuring PtSi Source/Drain With Dopant Segregation," *IEEE Electron Device Letters*, vol. 29, no. 1, pp. 125–127, Jan. 2008.
[93] J. Yin, W. Cai, Y. Zheng, and L. Zhao, "Effect of Pt film thickness on PtSi formation and film surface morphology," *Surface and Coatings Technology*, vol. 198, no. 1, pp. 329–334, Aug. 2005.
[94] K. Akarvardar, B. M. Dufrene, S. Cristoloveanu, P. Gentil, B. J. Blalock, and M. M. Mojarradi, "Low-frequency noise in SOI four-gate transistors," *IEEE Transactions on Electron Devices*, vol. 53, no. 4, pp. 829–835, Apr. 2006.
[95] E. Simoen, A. Veloso, Y. Higuchi, N. Horiguchi, and C. Claeys, "On the Oxide Trap Density and Profiles of 1-nm EOT Metal-Gate Last CMOS Transistors Assessed by Low-Frequency Noise," *IEEE Transactions on Electron Devices*, vol. 60, no. 11, pp. 3849–3855, Nov. 2013.
[96] S. Pud *et al.*, "Liquid and Back Gate Coupling Effect: Toward Biosensing with Lowest Detection Limit," *Nano Lett.*, vol. 14, no. 2, pp. 578–584, Feb. 2014.
[97] K. Bedner *et al.*, "Investigation of the dominant 1/f noise source in silicon nanowire sensors," *Sensors and Actuators B: Chemical*, vol. 191, pp. 270–275, Feb. 2014.
[98] A. Tarasov, W. Fu, O. Knopfmacher, J. Brunner, M. Calame, and C. Schönenberger, "Signal-to-noise ratio in dual-gated silicon nanoribbon field-effect sensors," *Applied Physics Letters*, vol. 98, no. 1, p. 012114, 2011.

[99] D. Zhang *et al.*, “An ion-gated bipolar amplifier for ion sensing with enhanced signal and improved noise performance,” *Applied Physics Letters*, vol. 105, no. 8, p. 082102, Aug. 2014.
[100] R. R. Harrison, “A Versatile Integrated Circuit for the Acquisition of Biopotentials,” in *2007 IEEE Custom Integrated Circuits Conference*, 2007, pp. 115–122.
[101] D. Zhang *et al.*, “An ion-gated bipolar amplifier for ion sensing with enhanced signal and improved noise performance,” *Applied Physics Letters*, vol. 105, no. 8, p. 082102, Aug. 2014.
[102] Q. Hu *et al.*, “Current gain and low-frequency noise of symmetric lateral bipolar junction transistors on SOI,” in *2018 48th European Solid-State Device Research Conference (ESSDERC)*, 2018, pp. 258–261.
[103] K. Akarvardar, B. M. Dufrene, S. Cristoloveanu, P. Gentil, B. J. Blalock, and M. M. Mojarradi, “Low-frequency noise in SOI four-gate transistors,” *IEEE Transactions on Electron Devices*, vol. 53, no. 4, pp. 829–835, Apr. 2006.

Acta Universitatis Upsaliensis

Digital Comprehensive Summaries of Uppsala Dissertations from the Faculty of Science and Technology 1794

Editor: The Dean of the Faculty of Science and Technology

A doctoral dissertation from the Faculty of Science and Technology, Uppsala University, is usually a summary of a number of papers. A few copies of the complete dissertation are kept at major Swedish research libraries, while the summary alone is distributed internationally through the series Digital Comprehensive Summaries of Uppsala Dissertations from the Faculty of Science and Technology. (Prior to January, 2005, the series was published under the title "Comprehensive Summaries of Uppsala Dissertations from the Faculty of Science and Technology".)

Distribution: publications.uu.se
urn:nbn:se:uu:diva-381049

ACTA
UNIVERSITATIS
UPSALIENSIS
UPPSALA
2019