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# Contacts and Interconnects for Germanium-based Monolithic 3D Integrated Circuits

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ACTA
UNIVERSITATIS
UPSALIENSIS
UPPSALA
2019

ISSN 1651-6214
ISBN 978-91-513-0687-2
urn:nbn:se:uu:diva-380573

Dissertation presented at Uppsala University to be publicly examined in Polhemsalen, Ångströmlaboratoriet, Lägerhyddsvägen 1, Uppsala, Friday, 20 September 2019 at 13:15 for the degree of Doctor of Philosophy. The examination will be conducted in English. Faculty examiner: PhD Fabrice Nemouchi (CEA-Leti, Grenoble, France).

**Abstract**

Jablonka, L. 2019. Contacts and Interconnects for Germanium-based Monolithic 3D Integrated Circuits. *Digital Comprehensive Summaries of Uppsala Dissertations from the Faculty of Science and Technology* 1824. 85 pp. Uppsala: Acta Universitatis Upsaliensis. ISBN 978-91-513-0687-2.

Three-dimensional integrated circuits have great potential for further increasing the number of transistors per area by stacking several device tiers on top of each other and without the need to continue the evermore complicated and expensive down-scaling of transistor dimensions. Among the different approaches towards the realization of such circuits, the monolithic approach, i.e. the tier-by-tier fabrication on a single substrate, is the most promising one in terms of integration density. Germanium is chosen as a substrate material instead of silicon in order to take advantage of its low fabrication temperatures as well as its high carrier mobilities. In this thesis, the work on two key components for the realization of such germanium-based three-dimensional integrated circuits is presented:the source/drain contacts to germanium the interconnects.

As a potential source/drain contact material, nickel germanide is investigated.In particular, the process temperature windows for the fabrication of morphologically stable nickel germanide layers formed from initial nickel layers below 10 nm are identified and the reaction between nickel and germanium is further studied by means of in-situ x-ray diffraction. The agglomeration temperature of nickel germanide is increased by 100 °C by the addition of tantalum and tungsten interlayers and capping layers. In an effort to more thoroughly characterize the contacts, a method to reliably extract the specific contact resistivity is implemented on germanium.

As a potential interconnect material cobalt is investigated. In a first step, highly conductive cobalt thin films are demonstrated by means of high-power impulse magnetron sputtering. The high conductivity of the cobalt films is owing to big grains, high density, high purity, and smooth interfaces. In a second step, the potential of high-power impulse magnetron sputtering for the metallization of nanostructures is further explored.

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ISSN 1651-6214
ISBN 978-91-513-0687-2
urn:nbn:se:uu:diva-380573 (http://urn.kb.se/resolve?urn=urn:nbn:se:uu:diva-380573)

*"Another direction of improvement is to make physical machines three dimensional instead of all on a surface of a chip. That can be done in stages instead of all at once; you can have several layers and then many more layers as the time goes on."*

— Richard Feynman, 1985 [1]

# List of papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I **Formation of nickel germanides from Ni layers with thickness below 10 nm**
L. Jablonka, T. Kubart, D. Primetzhofer, A. Abedin, P.-E. Hellström, M. Östling, J. Jordan-Sweet, C. Lavoie, S.-L. Zhang, and Z. Zhang
*Journal of Vacuum Science & Technology B*, vol. 35, no. 2, p. 020602, Mar. 2017.
DOI: 10.1116/1.4975152.

II **Improving the morphological stability of nickel germanide by tantalum and tungsten additions**
L. Jablonka, T. Kubart, F. Gustavsson, M. Descoins, D. Mangelinck, S.-L. Zhang, and Z. Zhang
*Applied Physics Letters*, vol. 112, no. 10, p. 103102, Mar. 2018.
DOI: 10.1063/1.5019440.

III **A novel route to a reliable extraction of the specific contact resistivity of the germanium/nickel germanide interface**
L. Jablonka, A. Abedin, P.-E. Hellström, S.-L. Zhang, and Z. Zhang
*Manuscript*

IV **Highly conductive ultrathin Co films by high-power impulse magnetron sputtering**
L. Jablonka, L. Riekehr, Z. Zhang, S.-L. Zhang, and T. Kubart
*Applied Physics Letters*, vol. 112, no. 4, p. 043103, Jan. 2018.
DOI: 10.1063/1.5011109.

V **Metal filling by high power impulse magnetron sputtering**
L. Jablonka, P. Moskovkin, Z. Zhang, S.-L. Zhang, S. Lucas, and T. Kubart
*Accepted at Journal of Physics D*, Jun. 2019.
DOI: 10.1088/1361-6463/ab28e2.

# Author's contributions

I Ex-situ part of the experimental, part of the manuscript writing.

II All of the experimental except for TEM and APT, manuscript writing.

III All of the experimental except for TEM, manuscript writing.

IV All of the experimental except for HiPIMS and TEM, most of the analysis, major part of the writing.

V Fabrication of the filling structures, part of the characterization and data evaluation, minor part of the writing.

# Related work

The following contributions were made during my studies, but are not included in this thesis:

1. L. Jablonka, "Beer – the cause of and answer to all of physics problems," in *International Conference of Physics Students 2015*, Zagreb, Croatia, 2015.

2. L. Jablonka, T. Kubart, F. Gustavsson, D. Primetzhofer, A. Abedin, P.-E. Hellström, M. Östling, J. L. Jordan-Sweet, C. Lavoie, S.-L. Zhang, and Z. Zhang, "Scalability Study of Nickel Germanides," in *Materials for Advanced Metallization 2016*, Brussels, Belgium, 2016, pp. 201–202.

3. M. Smolarczyk, L. Jablonka, S. Reuter, and H. Hillmer, "Self-aligned molding technology (SAMT) for fabrication of 3D structures with a foldable imprint mold," *Applied Nanoscience*, May 2019.

4. T. Tran, L. Jablonka, B. Bruckner, S. Rund, D. Roth, M. A. Sortica, P. Bauer, Z. Zhang, D. Primetzhofer, "Electronic interaction of slow hydrogen and helium ions with nickel-silicon systems," submitted to *Physical Review A*, May 2019.

# Contents

# Acronyms

**2D** two-dimensional
**3D** three-dimensional
**3D-SIC** 3D-Stacked Integrated Circuit
**3D-SOC** 3D-System-on-Chip
**3DIC** three-dimensional integrated circuit

**ALD** atomic layer deposition
**APT** atom probe tomography

**CBKR** cross-bridge Kelvin resistor
**CMP** chemical mechanical polishing
**CVD** chemical vapor deposition

**DCMS** direct current magnetron sputtering

**EBL** electron beam lithography
**EDS** energy-dispersive X-ray spectroscopy

**FET** field-effect transistor
**FIB** focused ion beam

**HAADF** high-angle annular dark-field
**HiPIMS** high-power impulse magnetron sputtering

**IC** integrated circuit
**ITRS** International Technology Roadmap for Semiconductors

**MOSFET** metal oxide semiconductor field effect transistor

**PE** plasma-enhanced

**RBS** Rutherford back-scattering
**RIE** reactive ion-etching
**RTP** rapid thermal processing

**SEM** scanning electron microscopy
**STEM** scanning transmission electron microscopy

**TEM** transmission electron microscopy
**TLM** transmission line model
**TSV** through silicon via

**XRD** X-ray diffraction
**XSEM** cross-sectional scanning electron microscopy

# 1. Introduction

Continuously downscaling the dimensions of metal oxide semiconductor field effect transistors (MOSFETs) in integrated circuits (ICs) has been the leitmotif of the semiconductor industry for decades [2]. Smaller device dimensions lead to faster switching speed, but also to a larger number of transistors per area. Thus, performance and cost efficiency could be improved at the same time.

These gains in device density have been achieved by shrinking the dimensions of the active devices in one device layer (two-dimensional (2D) scaling) while simultaneously scaling other relevant parameters to ensure device performance [3], [4]. At critical dimensions in the order of several atoms, however, it becomes increasingly difficult to continue the downscaling for both technological and economical reasons [5]. To avoid the challenges of continuous downscaling while still increasing the device density, the concept of stacking several device layers on top of each other is almost suggesting itself. In fact, this idea has been around for several decades [6]. The comparably high manufacturing costs per transistor, however, have inhibited the industrial realization of such three-dimensional (3D) interconnect technology [6], [7]. The increasing investments necessary for competitive 2D scaling, but also the potential of integrating different materials and technology nodes, and reducing the length of interconnects, have reignited the interest in three-dimensional integrated circuits (3DICs) in recent years [8].

One of the most pressing issues that prevents monolithic 3DICs from growing up is the fabrication of high quality devices in the upper tiers while maintaining the performance of the tiers beneath. Especially the high temperature steps (>1000 °C) involved in the fabrication of Si-based MOSFETs deteriorate the performance in the lower tiers [9]. Maintaining high device performance on all tiers is, however, crucial, as the gains of 3D integration would otherwise diminish. A way to alleviate the thermal stress on the devices in the lower tiers is the replacement of Si with Ge in the upper tiers [10]. Germanium can be processed at inherently lower temperatures (below 600 °C [11]) and could allow the realization of 3DICs with multiple tiers as illustrated in Figure 1.1.

This thesis work was conducted against the backdrop of fabricating such a 3DIC based on Ge. In particular, this work deals with two parts relevant for the realization of such circuits: the contacts to the source and drain areas of the MOSFETs and the interconnects between the different tiers. The usefulness of the presented results is, however, not limited to such 3DICs.

Before delving into the main findings of the thesis, chapter 2 deepens the background knowledge on 3D integration and gives a foretaste on the irks and

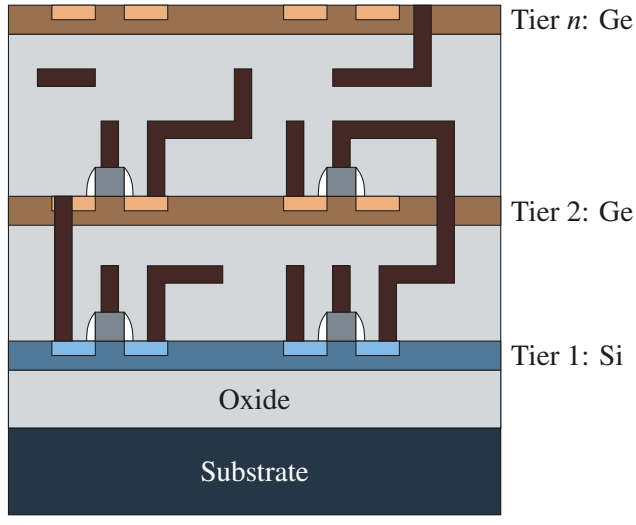



*Figure 1.1.* Conceptual schematics for a 3DIC based on Ge.

quirks of Ge. The most important characterization methods used in this thesis are introduced in chapter 3. The findings regarding nickel germanide—a material for the source/drain-contacts—are glanced at in chapter 4 and discussed in greater detail in Papers I and II. Chapter 5 and Paper III are dedicated to measurement structures for the extraction of the Ge/germanide specific contact resistivity and their fabrication. The work on the interconnects revolves around the fabrication of highly conductive cobalt thin films and the filling of contact holes and is treated in chapter 6 as well as in Papers IV and V. The thesis is concluded by a summary in chapter 7.

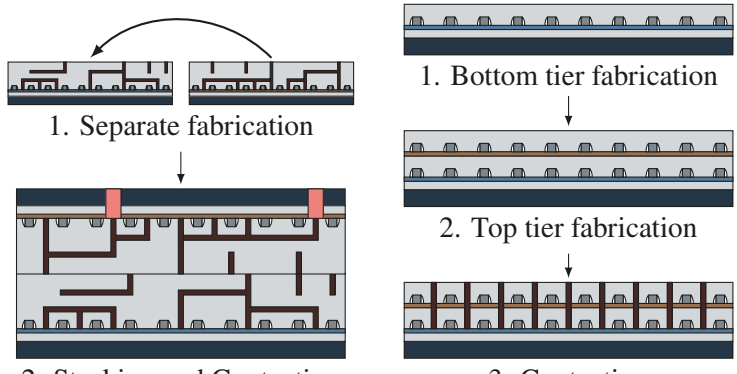
# 2. Background

Section 2.1 clarifies a few definitions on 3DICs, section 2.2 provides more details on the monolithic 3DIC approach that builds the project around this thesis work, and section 2.3 gives an overview about germanium.

## 2.1 3D ≠ 3D

There are many different approaches towards 3D interconnect technology and while all of them arrange active devices in a three-dimensional way, the degree of integration—and with that the benefits compared to 2D circuits—vary greatly. The International Technology Roadmap for Semiconductors (ITRS) from 2009 provides a useful naming convention based on the abstraction level at which the 3D integration happens [12], [13]. In the simplest case of 3D-Packaging, the fundamental elements are packaged circuits that are, for example, connected via wire-bonding. In a more complicated integration, larger circuit blocks are stacked and connected via through silicon vias (TSVs) to form 3D-Stacked Integrated Circuits (3D-SICs) or a 3D-System-on-Chip (3D-SOC). The highest degree of integration is achieved when the fundamental elements are single transistors that are connected via local interconnects. The latter concept is referred to as three-dimensional integrated circuits (3DICs).

The two pathways leading towards 3DICs are commonly denoted as polylithic (parallel) and monolithic (sequential) processing. Choosing the pathway is a trade-off between simplicity of integration and achievable device density. In polylithic processing the tiers are fabricated on separate wafers or dies and bonded together at end (Figure 2.1a). This simplifies the device fabrication as established process flows can be used for the separate tiers. The device density that can be achieved with polylithic processing is, however, limited by the alignment accuracy for bonding the separate tiers together of about 1 µm [15], [16]. Therefore, the inter-tier interconnects, cannot be smaller than that. In sequential processing the device and metal layers of the upper tiers are grown directly on top of the lower tiers (Figure 2.1b). This puts huge constraints on the device fabrication as the devices in the first tiers are exposed to all subsequent process steps of the following tiers. Especially process steps involving high temperatures, like dopant activation, pose a challenge. The possible alignment accuracy is much better (about 10 nm) and allows for a denser spacing of the inter-tier interconnects [17]–[20]. Sequential processing offers interesting new possibilities for cell design [21], [22] and the heterointegration of different




(a) Parallel processing (b) Sequential processing

*Figure 2.1.* Two roads lead to 3DICs. Adapted from [15].

materials. For example, pMOS and nMOS devices could be fabricated on different tiers [23], [24] or III-V semiconductors, Ge, and Si could be combined [25], [26]. Overall, the monolithic pathway has great potential and is fairly unexplored and is therefore the chosen pathway of the project surrounding this thesis work.

## 2.2 Monolithic 3DICs

The main challenge in the realization of 3DICs lies in ensuring the device performance in all tiers. To ensure this, high quality substrates are needed in the upper tiers, the performance of the devices in the upper and lower tiers has to match, and upper tiers need to be fabricated at low temperatures [15], [27]. In addition, the vertical interconnects need have a low resistance and a high density.

Several methods have been explored for the fabrication of high quality substrates in the upper tiers such as laser crystallization, seed crystallization and direct wafer bonding [13]. The two former methods can involve relatively high temperatures of more than 1000 or 900 °C to crystallize the device layers, which is detrimental for the quality or the lower tiers or requires the implementation of heat shielding layers, which lowers the integration density. Direct wafer bonding involves the transfer of an entire wafer onto the tiers [18], [28], [29]. The bonding temperatures are low and the transferred substrate can be of high quality. As the process is not limited to silicon it allows the combination of heterogeneous materials. This can for example be used to fabricate sensors directly on top of logic circuits [30].

One of the main arguments for 3DICs that is often put forward is the reduction of the wirelength compared to 2D systems. Planar downscaling not

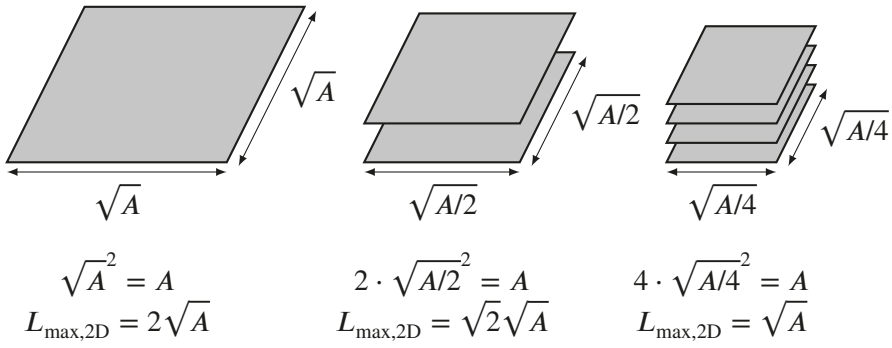



*Figure 2.2.* When a circuit with an area $A$ is split up into $n$ tiers, the length of the longest interconnect $L_{\max,2D}$ reduces with a factor of $\sqrt{n}$. Adapted from [13].

only increases the number of transistors per area, but also the number of wires and their total length. In extremely scaled devices this contributes massively to parasitic losses and time delays. A simple estimation shows how 3D stacking of $n$ device tiers can reduce the length of the longest interconnects within one tier $L_{\max,2D}$ (Figure 2.2). For a constant area $A$, $L_{\max,2D}$ scales with $1/\sqrt{n}$ [13]. More thorough estimations also take the inter-tier interconnects into account. The estimated gains in density and performance, however, are strongly dependent on the assumptions for the process platforms [31]–[33]. Whether 3D integration actually is cost-efficient is another story in which the number of process steps and the respective yield play a major role [9].

## 2.3 Germanium

Even though the first transistor that was invented at Bell Labs in 1947 was based on Ge [34], Si became the basis for the first integrated circuits in the 1960s and has remained so until today [35], [36]. The reasons for the success of Si are manifold. For instance, Si could be fabricated with higher purity and could withstand higher temperatures [37]. The main advantage of Si, however, was the superior quality of its native oxide [37]–[39]: $SiO_2$ could be grown in a very controlled manner and passivates the semiconductor surface very efficiently. Germanium, on the contrary, forms a range of sub-oxides $Ge_xO_y$ with inferior surface passivation capabilities. Moreover, the water-solubility of $GeO_2$ greatly complicates the process integration, whereas $SiO_2$ can be patterned and handled more easily. The benefits of $SiO_2$ eventually led to the development of the planar process [40] and the mass production of transistors.

Despite the aforementioned issues, Ge has been reintroduced into modern ICs [41]. To further improve the MOSFET performance, strain was induced in the channels which increases the mobility [42]. First, biaxially strained Si channels were grown on relaxed SiGe virtual substrates, whereby the tensile

*Table 2.1.* Selected properties of Si and Ge [58].

| Semiconductor | Band gap [eV] | Electron mobility [$cm^2/(V\,s)$] | Hole mobility [$cm^2/(V\,s)$] |
|---|---|---|---|
| Si | 1.12 | 1450 | 500 |
| Ge | 0.66 | 3900 | 1800 |

strain could be controlled by the Ge content leading to higher electron mobility [42], [43]. Later, SiGe was embedded in the source-drain areas to induce compressive uniaxial strain in the channel leading to higher hole mobility [42], [44]. At the same time, the scaling requirements on the gate dielectrics lead to the replacement of $SiO_2$ by other dielectrics with higher dielectric constant. With $SiO_2$ being replaced anyway, there has been increased effort to fabricate field-effect transistors (FETs) based on pure Ge [45] in order to utilize the increased electron and hole mobilities of Ge compared to Si (Table 2.1). In view of an application in monolithic 3DICs, Ge is particularly interesting for the upper tiers as it can be processed at temperatures below 550 ℃.

Some of main obstacles for fabricating Ge FETs with high performance are the passivation of the Ge-dielectric interface, the low $I_{on}/I_{off}$ ratio, the relatively unexplored surface chemistry, and the lack of knowledge about the contact resistivities of germanides [39], [46]–[48]. As another example, Ge substrate loss during annealing shall not go unmentioned here, as it proved to be a major impediment for realizing the contact resistivity measurement structures in Paper III and chapter 5. The substrate loss of Ge is related to the desorption of GeO during annealing [49], [50], [52]–[61]. Proposed mechanisms include the decomposition of $GeO_2$ and subsequent reaction with the Ge substrate [49], [54], [61] and the diffusion of GeO through $GeO_2$ [56].

# 3. Characterization Techniques

Device fabrication and material studies require a wide range of characterization techniques in order to assess electrical properties, dimensions and topographies, compositions etc. Here, the most important characterization techniques used in the appended papers are introduced.

## 3.1 Four-point probe measurements

A simple and quick way to assess the electrical properties of a thin film are four-point probe measurements [4], [64]. Four collinear, equally-spaced probes are brought into contact with the sample surface (Figure 3.1). A current $I$ is passed through the outer probes, while the potential difference $V$ is measured between the inner probes. The sheet resistance $R_{\mathrm{sh}}$ can then be calculated according to

$$R_{\mathrm{sh}} = F \cdot \frac{V}{I}, \tag{3.1}$$

where $F$ is a correction factor for the shape of the sample. If the probe spacing $s$ is much smaller than the sample diameter and the thickness $t$ of the uniform film is much smaller than $s$, $F$ can be approximated as $\pi/\ln 2 \approx 4.532$. The tool used in this work was equipped with probes spaced by a distance of 1 mm. Hence, for smaller samples like in Papers I & II, $F$ needs to be adjusted according to Figure 3.1b. To denote that $R_{\mathrm{sh}}$ is not the resistance of the sample even though Equation 3.1 gives the unit Ω, $R_{\mathrm{sh}}$ is commonly expressed as Ω/□. If $t$ is known, the film resistivity $\rho$ can be calculated via

$$\rho = R_{\mathrm{sh}} \cdot t. \tag{3.2}$$

Thanks to the short measurement time, four-point probe measurements are commonly used to access the uniformity in thickness or resistivity of thin films by measuring at different locations. A contour plot of a 100 mm wafer after epitaxial growth of B-doped Ge is shown in Figure 3.2 and demonstrates good uniformity.

## 3.2 Electron microscopy

To analyze topography and cross-sections of samples with a high spatial resolution at the nanometer range, scanning electron microscopy (SEM) is a powerful method. An electron beam is focused by electromagnetic lenses and swept

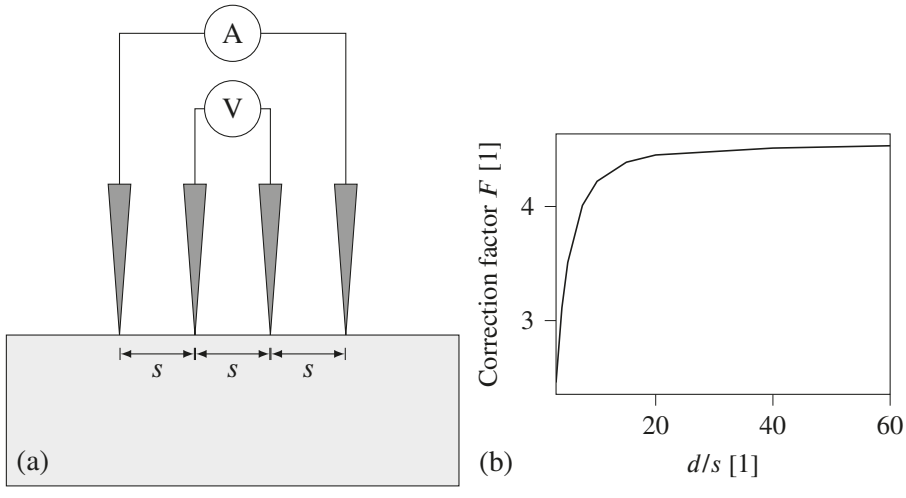



*Figure 3.1.* (a) Four point probe setup (b) Correction factor $F$ for different ratios of the sample diameter $d$ to the probe spacing $s$.

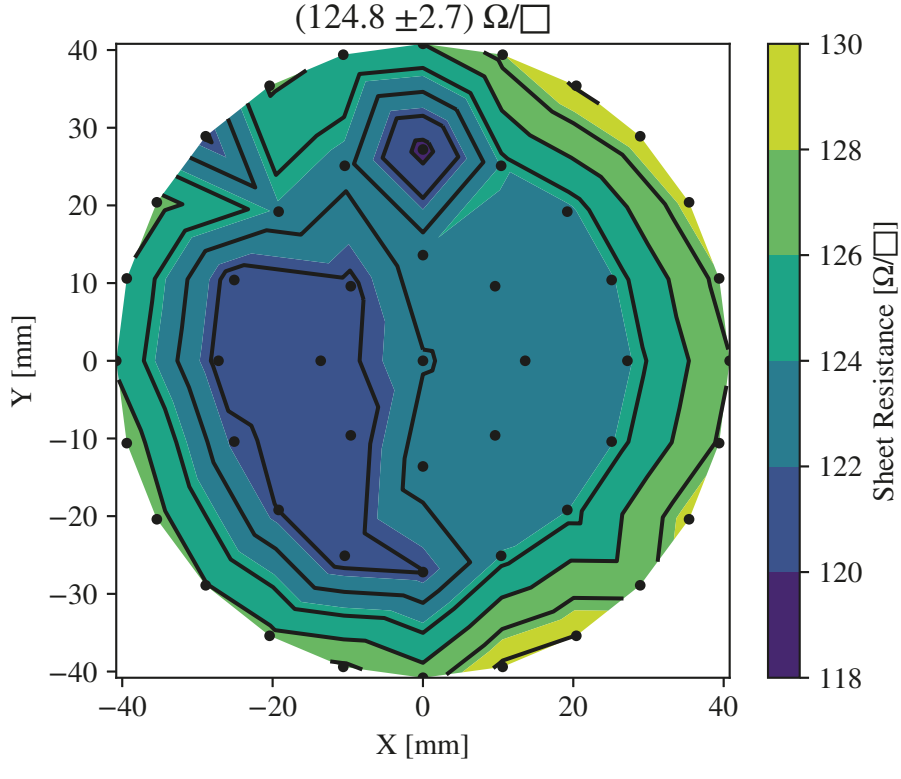



*Figure 3.2.* Contour plot of the sheet resistance mapped across a 100 mm wafer after epitaxial growth of B-doped Ge.

over the sample surface spot-by-spot. These impinging electrons can get back-scattered from the surface and subsequently be counted in a detector. Incoming electrons can also excite core electrons in the sample. If the energy transfer to the core electrons is high enough, these secondary electrons get ejected from the sample and can be detected in a separate detector.

Looking at cross-section by means of electron microscopy can provide additional insight on the sample structure. That the manner in which the cross-sections are prepared greatly influences the image quality is visualized in Figure 3.3. In the simplest case, the samples are cleaved. While this is sufficient for measuring e.g. film thicknesses, the analysis of smaller structures like filled contact holes is complicated by samples breaking around the holes or by deposits falling off the holes. Figure 3.3a shows a cross-section of contact holes after cleaving. The contact hole in the center appears to be not filled whereas the holes on the left and right are filled. To make more precise cross-sections of samples, a focused ion beam (FIB) can be used to specifically cut out certain areas. Figure 3.3b shows the sample surface from the top after performing such a FIB cut. The obtained cross-sectional SEM image after the cut appears much smoother (Figure 3.3c).

Higher resolutions are possible by analyzing the electrons that are transmitted through a sample with transmission electron microscopy (TEM). For the TEM sample preparation a FIB is used to cut out a lamella with thickness below 100 nm. A TEM image of a comparable contact is shown Figure 3.3d.

## 3.3 X-ray diffraction

To investigate the crystal structure of a sample, X-ray diffraction (XRD) can be used. Incoming monochromatic X-ray radiation of wavelength $\lambda$ is directed onto the sample and gets scattered by the atoms. As the atoms in a crystal are ordered in a regular array of lattice planes, the scattered X-ray waves interfere and form a diffraction pattern that is characteristic of a specific crystalline material. In the $\theta/2\theta$-configuration, the X-ray source is placed at an angle of $\theta$ with respect to the sample surface, while the detector is placed at an exit angle of $2\theta$ with respect to the incoming beam. Diffraction is observed from a set of lattice planes with interplanar spacing $d$ when the Bragg condition

$$n\lambda = 2d \sin\theta \tag{3.3}$$

is fulfilled, where $n$ is a positive integer [65]. When measured in-situ during the annealing of a sample as done in Paper I and shown in Figure 4.3, XRD can provide valuable information about the phase formation sequence and kinetics.

Thin films are commonly analyzed in the grazing-incidence configuration in order to maximize the interaction volume of the beam with the thin film and thereby the respective signals. Exemplary diffractograms of Co thin films are shown in Figure 3.4.

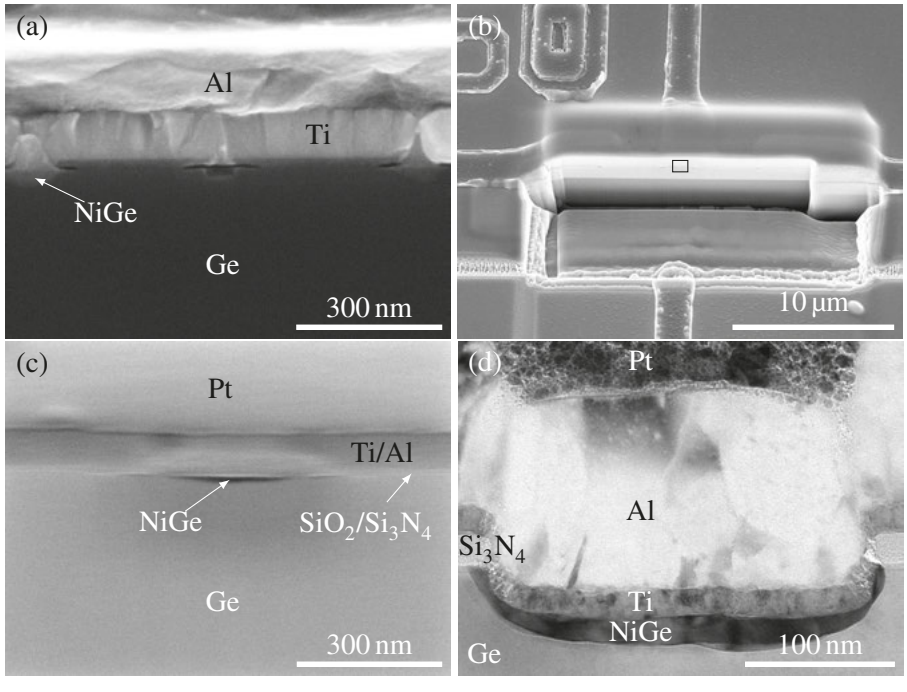



*Figure 3.3.* Cross-sectional electron microscopy is used to analyze the contact formation. The way the cross-sections are prepared influences the image quality. (a) SEM micrograph of a cleaved sample. (b) SEM micrograph of a sample after FIB-cut at a tilt angle of 60°. (c) SEM micrograph of the highlighted area in (b). (d) TEM micrograph of a lifted out lamella.

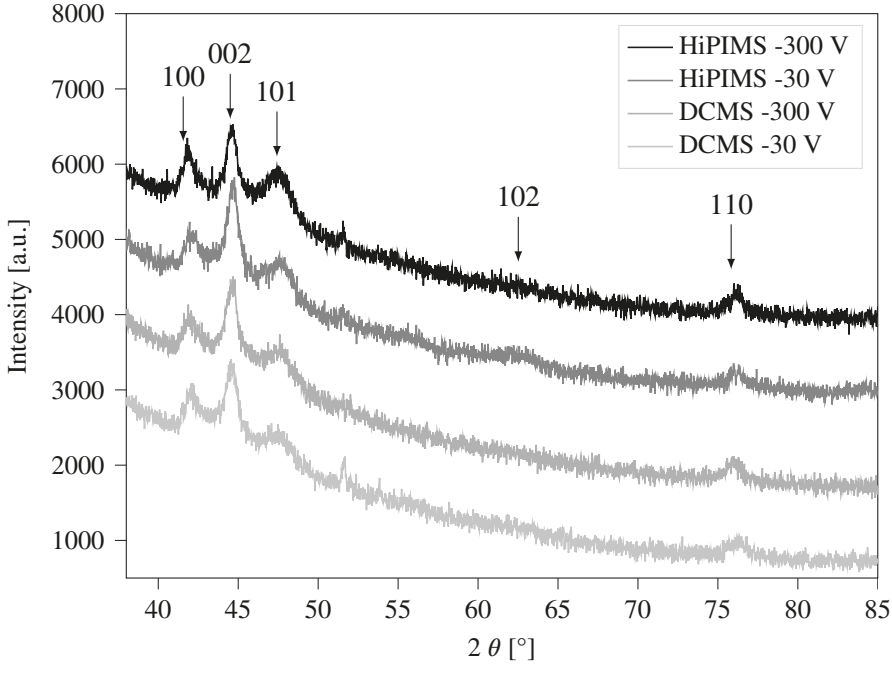



*Figure 3.4.* Grazing-incidence XRD of Co films (Paper IV). The measurements were performed by Oleksandr Bilousov.

In polycrystalline materials with completely randomly oriented grains, at least some grains will have lattice planes oriented in parallel to the sample surface and the $\theta/2\theta$-configuration is suitable for characterizing the material. However, if the film is textured, i.e. a preferential alignment of the grains towards the substrate is present, certain diffraction peaks will be missing from the diffractogram. For example, in the in-situ XRD measurements of Figure 3.5 no peaks are visible in the temperature range between the disappearance of Ni and the appearance of NiGe. A different configuration, in which every possible grain orientation can be assessed, is the Schulz method [66]. Here the detector is kept at $2\theta$, but the diffractometer also allows to change tilt ($\chi$) and rotation ($\phi$) angles. The downside of measuring in this configuration is the greatly prolonged measurement time. A reduction of the measurement time is possible by using X-rays with higher intensities from synchrotrons as well as area-detectors that record a range of $2\theta$ angles simultaneously. The resulting data is conveniently displayed as a pole-figure, where $\chi$ is the radial distance, $\phi$ the polar angle, and the color corresponds to the measured intensity, see Figure 3.6.

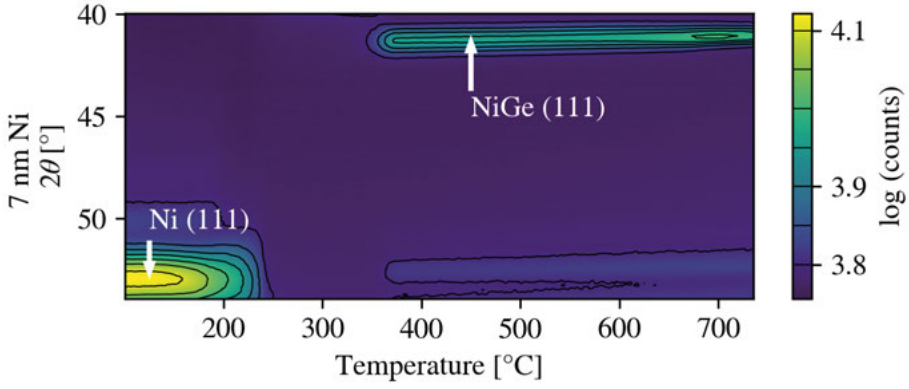



*Figure 3.5.* In-situ XRD (Paper I). Data from Christian Lavoie, IBM.

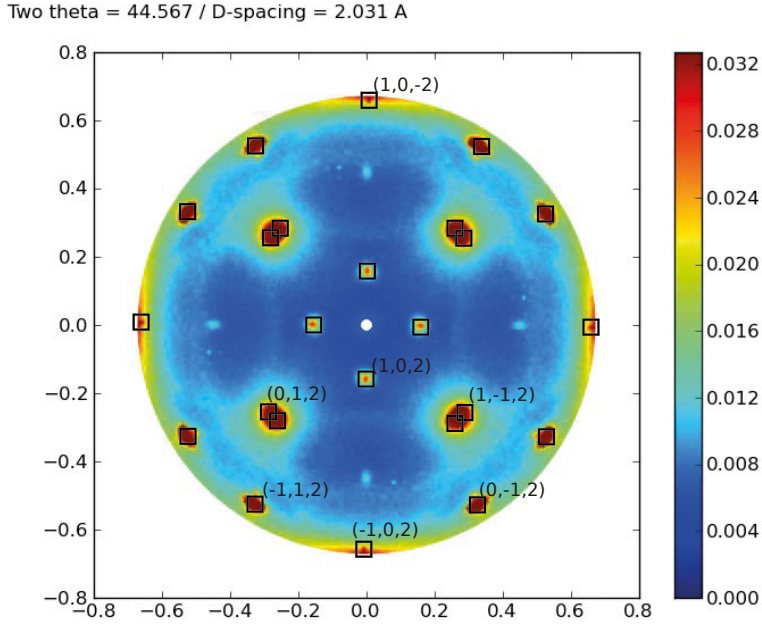



*Figure 3.6.* Pole figure of the $(10\bar{1}2)$ plane of $\varepsilon$-$Ni_5Ge_3$ measured for a 7 nm Ni film on Ge (100) quenched at 250 ˚C. Courtesy of Christian Lavoie (IBM).

## 3.4 Ion beam analysis

The interaction of accelerated ions with thin films can be used to measure compositions, elemental distributions and areal densities with high precision. For this a beam of ions is directed onto a sample. The incoming ions lose energy by exciting electrons or interacting with nuclei. This can trigger a wide range of processes, that can be used for the analysis of thin films. In this thesis, back scattering techniques were mainly employed. Here, the energy of ions that have collided with nuclei and were scattered back is measured. The energy of the detected ion depends on its mass, its initial energy, and its path through the irradiated sample. The resulting energy spectrum can be analyzed and fitted to obtain composition and areal densities of the layers.

For the studies in Papers I, II and IV Rutherford back-scattering (RBS) was used to study the areal densities of the thin films. In particular, $^4He^+$ with 2 MeV was used at a scattering angle $\theta$ of 170°. When such a light ion hits a heavier atom, it gets scattered back elastically. The ratio of the ion energies before ($E_0$) and after ($E_1$) an elastic collision depends on the mass of the incoming ion $M_1$, the mass of the target atom $M_2$, and the scattering angle $\theta$ and is expressed by the kinematic factor K [67]

$$K = \frac{E_1}{E_0} = \left( \frac{M_1 \cos\theta + \sqrt{M_2^2 - M_1^2 \sin^2\theta}}{M_1 + M_2} \right)^2 . \tag{3.4}$$

The incoming ions not only lose energy when hitting nuclei but also when colliding inelastically with electrons while passing through the sample. Therefore, ions that get backscattered from nuclei deeper in the sample will have a lower energy than ions scattered from the surface (for a given angle and target mass). The energy loss per unit path length $\mathrm{d}E/\mathrm{d}x$ in an elemental film is described by the stopping cross-section $\epsilon$

$$\epsilon = \frac{1}{n} \cdot \frac{\mathrm{d}E}{\mathrm{d}x}, \tag{3.5}$$

where $n$ is the atomic density [68].

Typical RBS spectra are shown in Figures 3.7 & 3.8, respectively. The spectrum in the former figure was used to measure the areal density of a Co film and the amount of incorporated Ar therein. The spectra in the latter figure illustrate how thin-film reactions can be studied by means of RBS. Comparing the positions of the Ta peak before and after annealing shows that Ta is located on top of NiGe after annealing, as the peak is shifted to higher energy. This indicates that Ni is the dominant diffusing species in the reaction with Ge.

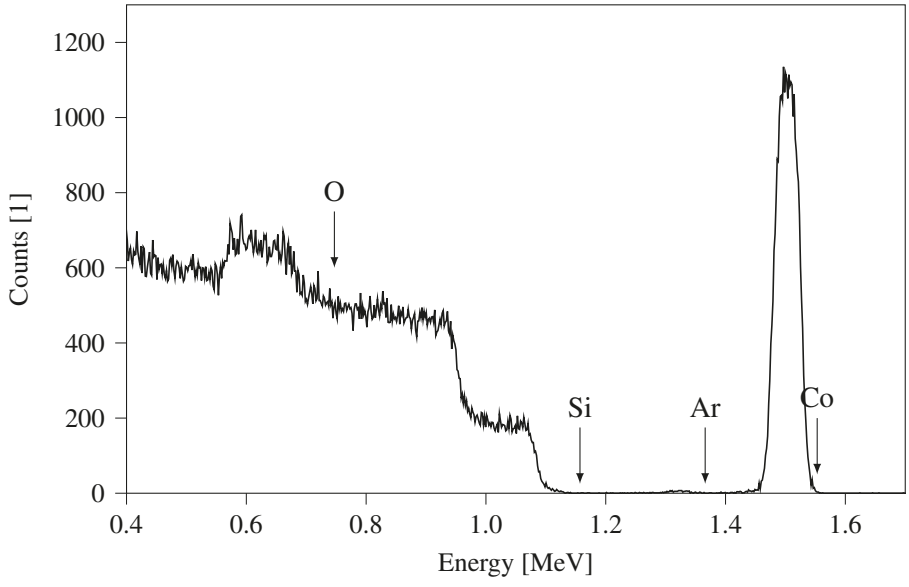



*Figure 3.7.* RBS spectrum of a Co film deposited on a $Si/SiO_2$ substrate by DCMS at a substrate bias of −300 V. About 1.1 % Ar is incorporated in the Co film (Paper IV).

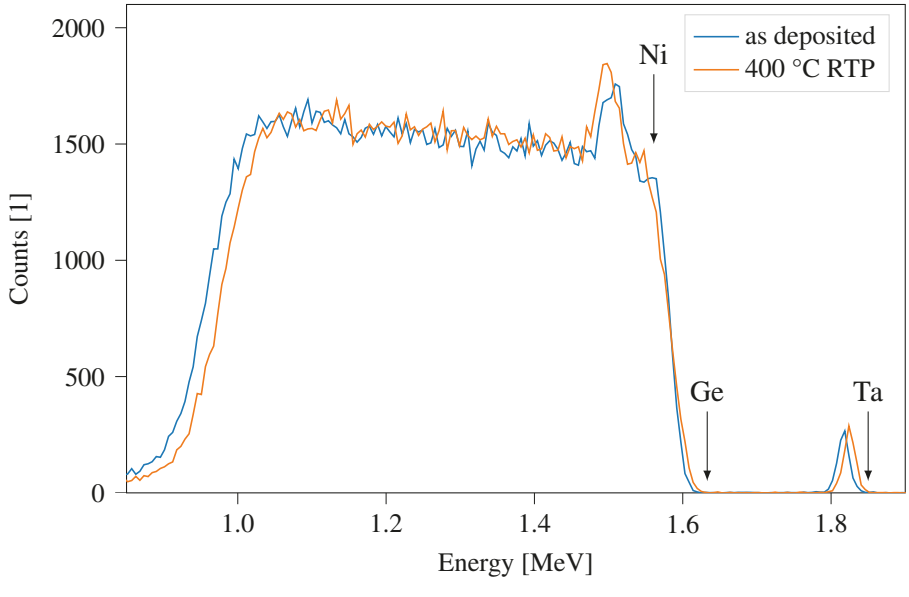



*Figure 3.8.* RBS spectra of Ge/0.5 nm Ta/5 nm Ni before and after annealing. After RTP Ta is located on top of Ni indicating that Ni is the dominant diffusing species during the formation of NiGe.

## 3.5 Atom probe tomography

With atom probe tomography (APT) three-dimensional images can be acquired with single atom sensitivity on almost atomic scale [69]. For this, a needle-shaped probe is cut from a region of interest in the sample using a FIB (Figure 3.9). The probe is transferred to an ultra-high vacuum chamber, cooled down to temperatures of 20 to 50 K, and placed in front of a counter electrode as illustrated in Figure 3.10. Atoms are successively removed from the tip of this probe in form of ions by field evaporation [70]. For this, a constant potential of 2 to 10 keV is applied between the specimen and the counter electrode. The ionization is then initiated by periodically applying either electrical pulses or laser pulses. The evaporated positive ions are accelerated towards the counter electrode, pass through the aperture and hit a position-sensitive detector after a certain time-of-flight. The evaporation rate is kept low to avoid simultaneous hits of ions and to reduce the stress on the tip.

The recorded data can be used to reconstruct the initial structure of the probe: The identity of the ions can be inferred from the time-of-flight from evaporation until detection. The initial x-y position of the atoms is determined by where the ions hit the detector, while the z-position is determined from the order in which the ions arrive at the detector [69]. After reconstructing the initial structure of the probe, a variety of properties, such as elemental concentrations per volume, concentration profiles, or element segregation at interfaces can be studied.

When evaporating stacked thin-film structures like in Paper II, attention has to be paid to the thermally insulating layers and the required electric fields. The first set of samples consisted of a Si/$SiO_2$/Si/Ge/NiGe/Ta stack. The poor heat conduction through the $SiO_2$ layer caused 4 out of 6 prepared probes to break during evaporation. If the probe had been cut in parallel and not perpendicular to the sample as described in [71], the number of broken tips possibly could have been reduced. The second set of samples consisted of a Si/Ge/NiGe/W stack, so heat conduction was not a problem. However, the disparity between the evaporation fields of W and Ni/Ge is very high (W requires a very high evaporation field of ∼60 V/nm [72, p. 9]). This can cause too high evaporation rates when transitioning from the W to the NiGe layer leading to bigger clusters instead of single ions arriving at the detector, or even to breaking probes. Figure 3.11 shows the reconstructed probe of a W-containing sample that did not break during evaporation.

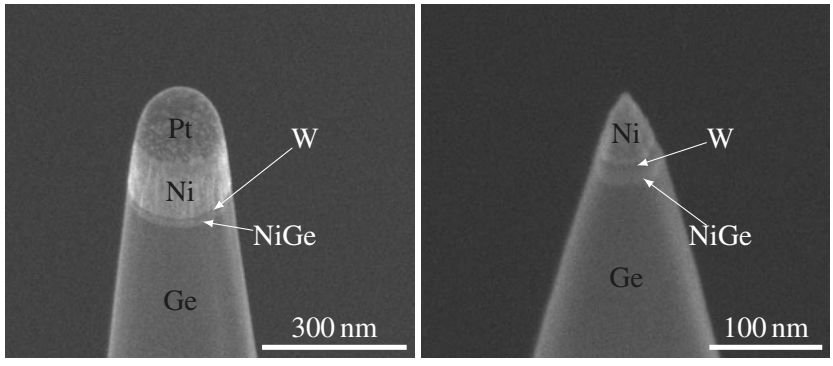



*Figure 3.9.* SEM micrographs of a probe being prepared for APT. The probes were prepared by Marion Descoins.

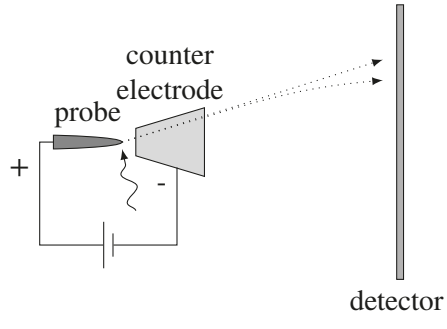



*Figure 3.10.* APT schematics.

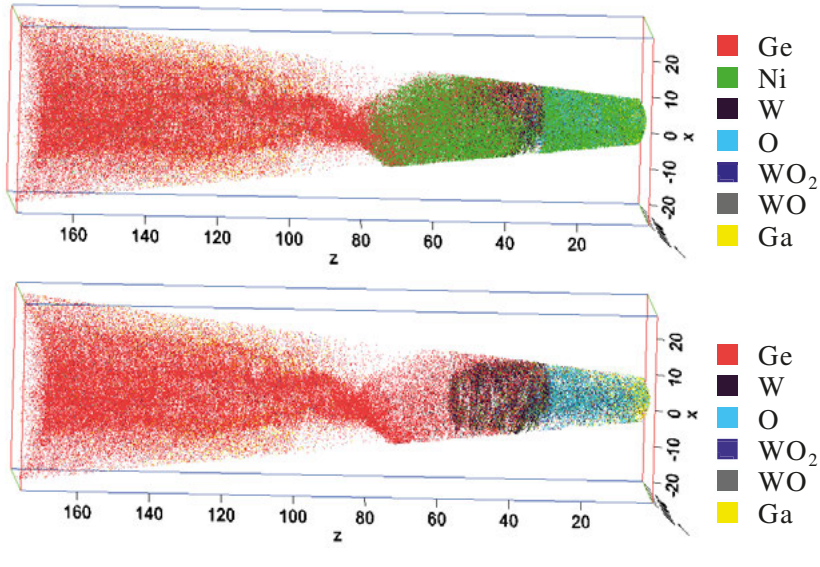



*Figure 3.11.* A reconstructured probe after APT. Both images show the same probe, but Ni is not displayed in the bottom image.

# 4. Source/drain contact materials

At the beginning of the study of contact materials for Ge-based 3DICs stands the selection of a proper material. A systematic study by Gaudet *et al.*, who screened thin films of transition metals for their reaction with Ge, identified NiGe as one the most promising candidates based on its low formation temperature, low resistivity, and good morphological stability [73]. Further studies by several different groups have subsequently investigated NiGe in greater detail, but focused on initial Ni thicknesses of 10 nm and above [74]–[79]. Thus, having the integration into Ge-based 3DICs in mind, we studied the reaction of Ni films thinner than 10 nm with Ge in more detail, focusing on the phase formation sequence, the electrical resistivity, and the morphological stability of the formed nickel germanides. In an attempt to increase the process temperature window of thin NiGe, interlayers and capping layers of Ta and W were deposited prior to the NiGe formation. We found that the morphological stability against agglomeration could be increased without increasing the sheet resistance (Paper II).

## 4.1 Self-aligned germanidation

Contacts to the source and drain areas of MOSFETs are commonly formed via a self-aligned process. This allows for more densely packed devices and greatly simplifies the process integration as no additional lithography step is needed. The process consists of three steps and is illustrated in Figure 4.1. Firstly, a thin metal film is deposited onto the sample, where the gate structure has already been defined. Secondly, the substrate is annealed and the thin film reacts with the semiconductor but not with the dielectrics. Lastly, unreacted metal is removed by a selective wet etch.[1]

The self-aligned contact formation on Si has been studied extensively in the past and the integration on Ge can be based on this knowledge. In both cases, the metal film is commonly deposited via evaporation or sputtering (see section 6.2). The subsequent annealing is preferably long enough to form the desired phase and short enough to avoid the diffusion of dopants or metal. In this work, rapid thermal processing (RTP) was used, a process in which the sample can be heated up in a quick and uniform way by means of lamps. The reaction temperatures of metals with Ge are typically lower than with its

[1] There can be an additional annealing step after the selective etch to obtain the desired phase.

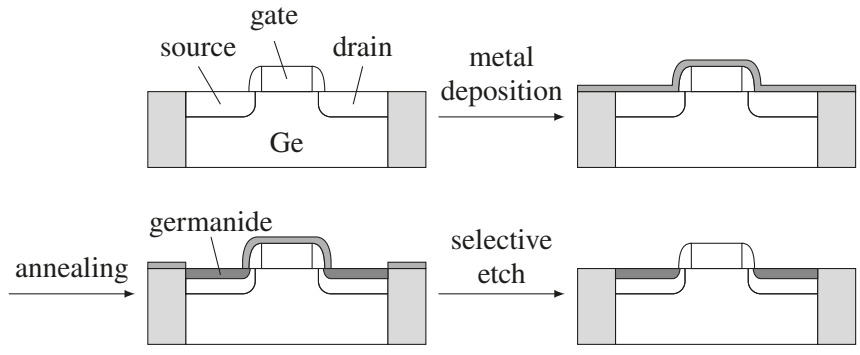



*Figure 4.1.* Self-aligned contact formation occurs in three steps: Metal deposition, annealing, and selective etch.

lighter homologue Si (a welcome circumstance considering the limited thermal budget in 3DICs). The typical selective etch to remove unreacted Ni on Si-based substrates is Caro's acid (a mixture of $H_2SO_4$ and $H_2O_2$). This etchant is, however, not compatible with Ge due its oxidizing properties and the water solubility of $GeO_2$. In this thesis work a 10 vol % aqueous solution of HCl at 55 °C was used to selectively remove unreacted Ni [80].

## 4.2 Nickel germanides

When integrating nickel germanide contacts into a fabrication flow it is important to exactly know at which temperatures the desired low-resistivity phase NiGe is present. A quick way to deduce the presence of NiGe is measuring the $R_{sh}$ after annealing (see section 3.1). An exemplary plot of the $R_{sh}$ in dependence of the RTP temperature is shown for an initial Ni thickness of 8 nm in Figure 4.2. The measured $R_{sh}$ can be divided into three temperature ranges. In region I (below 300 °C) the formation of NiGe is incomplete, i.e. Ni has not reacted with Ge at all and/or a Ni-rich germanide with higher resistivity is present. Region II marks the sole presence of NiGe with low resistivity, the so-called process window. In region III (500 °C and above) the NiGe film first forms voids and then agglomerates. In Paper I a similar graph also presents the relation for thinner and thicker Ni films.

### 4.2.1 Phase formation

Sheet resistance measurements after RTP (ex-situ) only give a bit of information about the electrical properties of the final thin film. To gain more insight into the processes during the phase formation, in-situ XRD measurements were undertaken while annealing Ni films (2 to 9 nm) on Ge(100) (Figure 4.3). It is noted that the temperature ramp rate of 3 °C/s was slower than the RTP ramp

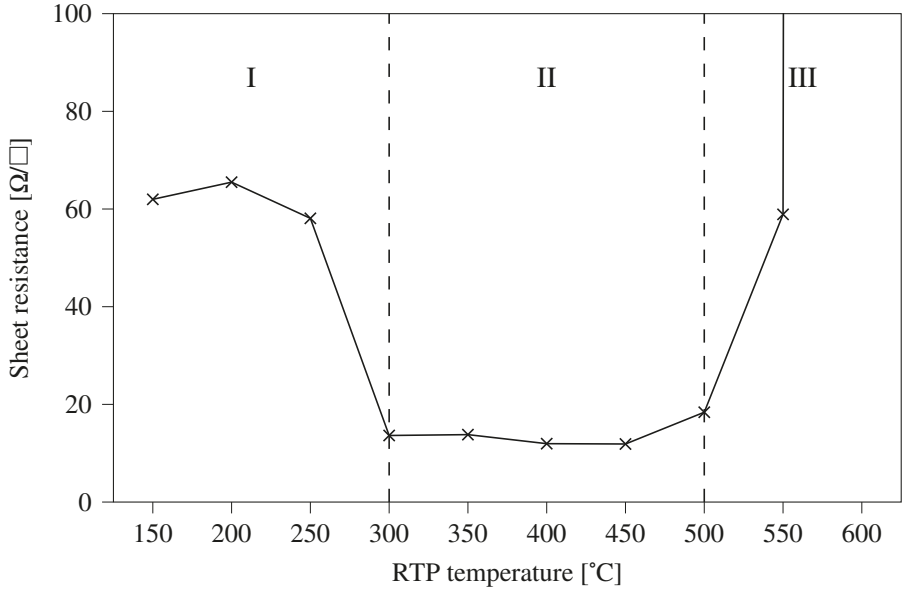



*Figure 4.2.* Sheet resistance vs RTP temperature (10 ˚C/s) for 8 nm Ni on Ge.

rate of 10 ˚C/s in order to have enough aquisition time. Two characteristic peaks are visible in the diffractograms and can be assigned to the presence of elemental Ni (∼53°) and NiGe (∼41°). Three interesting observations can be inferred from the thickness- and temperature-dependent presence of the two phases: (I) Thicker Ni layers lead to Ni still being present at higher temperatures. (II) The appearance of NiGe has a minimum for 5 and 7 nm at 360 ˚C. For thinner and thicker initial Ni films, the NiGe formation occurs at higher temperatures. (III) Ni and NiGe are not present at the same time. In the following these observations are explained.

(I) Since Ni is the dominant diffusing species [76] thicker Ni layers prolong the reaction to the intermediate phase, whose completion is indicated by the disappearance of the Ni peak.

To explain observation (II) an excursion into classical nucleation theory is needed [81]–[84]. The driving force for the formation of a new phase is the gain in Gibbs free energy $\Delta G$, while the formation is impeded by the change in surface energy due to the formation of new interfaces. $\Delta G$ can be expressed by

$$\Delta G = ar^3 \Delta g_V + br^2 \Delta\sigma, \tag{4.1}$$

where $r$ is the radius of the nucleus, $a$ and $b$ are geometrical constants describing the shape of the nucleus, $\Delta g_V$ is the Gibbs free energy change per unit volume of the nucleus, $\Delta\sigma$ the surface energy change per unit area. For a stable phase $\Delta g_V$ is negative, whereas $\Delta\sigma$ is usually positive. Since the contribution of $\Delta g_V$ in Equation 4.1 scales with $r^3$, while the surface energy contribution

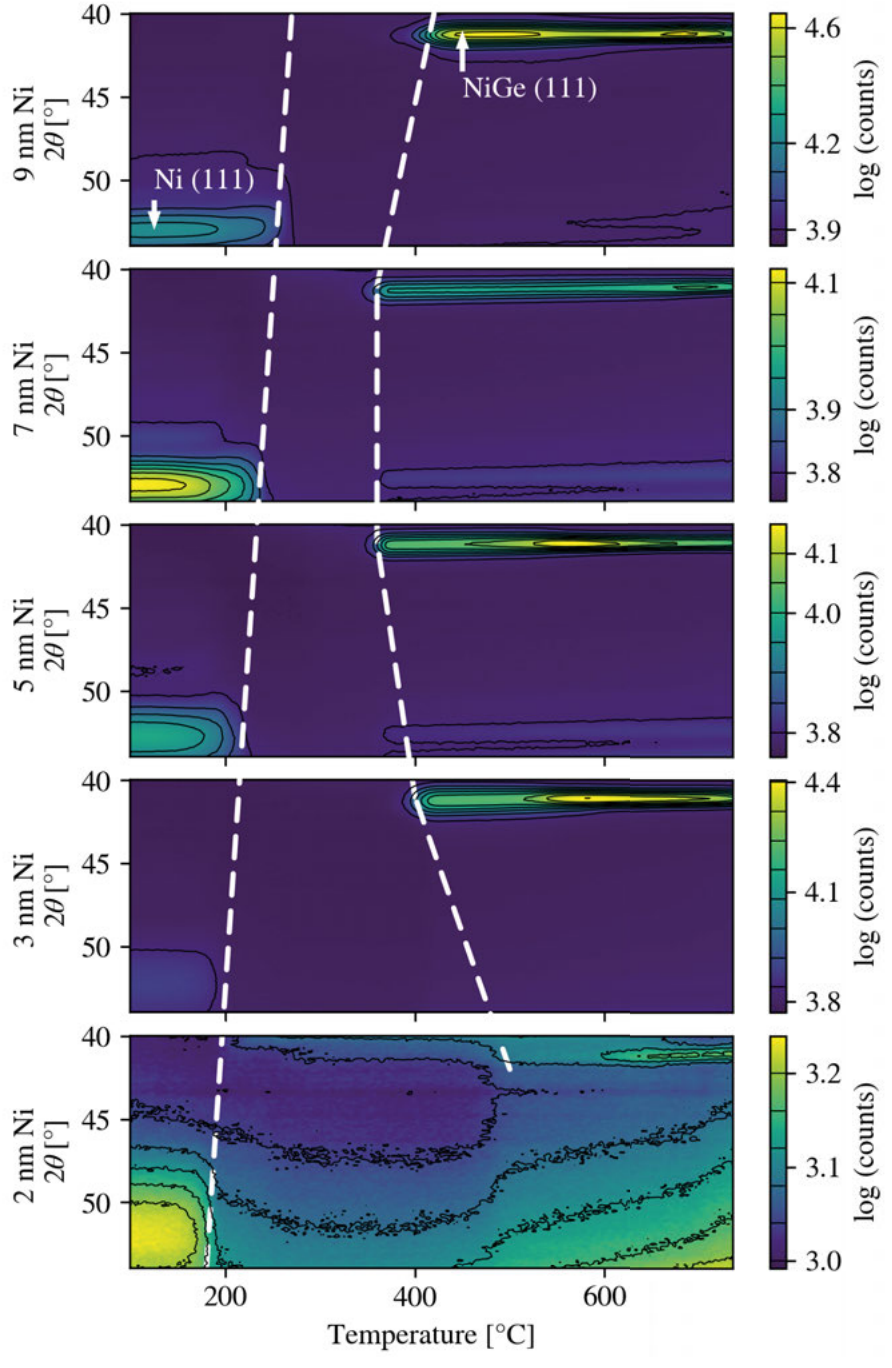



*Figure 4.3.* In-situ XRD (Paper I). Data from Christian Lavoie, IBM.

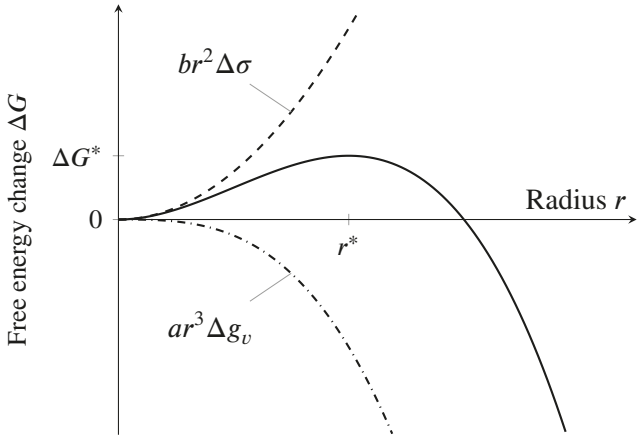



*Figure 4.4.* Energy curve for phase nucleation. Adapted from [85].

scales with $r^2$, $\Delta G$ has a maximum at a critical radius $r^*$ (Figure 4.4). The maximum of the curve occurs at a critical radius $r^*$. Nuclei with a radius bigger than $r^*$ are more likely to grow than to shrink. The maximum, $\Delta G^*$, is a measure for the energy barrier that has to be overcome to grow the new phase. There is a specific thickness $d_s$ above which a new phase grows spontaneously. Below $d_s$ higher temperatures are required to nucleate a new phase [81]. In Paper I the initial Ni thickness corresponding to this specific thickness was estimated to be 4.7 nm.

Observation III gives important information about the phase formation sequence. For thicker Ni layers a simultaneous growth of the Ni-rich germanide phase and NiGe had been observed [74], [86]. Here the Ni-rich germanide is not visible in in-situ XRD. However, for a simultaneous growth of both phases, elemental Ni and NiGe have to be present at the same time [74], [79]. As this is not the case, a sequential phase formation can be deduced for initial Ni thicknesses of 2 to 9 nm.

The nature of the intermediate Ni-rich phase had been ambiguous in the past. Some groups identified the phase as $Ni_2Ge$ [87], others as $Ni_3Ge_2$ [88], others as $Ni_5Ge_3$ [74], [76], [80], [86], [89]–[92]. De Schutter *et al.* have studied the intermediate phase in great detail and identified the phase as $\epsilon$-$Ni_5Ge_3$ [79], [93]. Our pole-figure measurements of samples with an initial Ni thickness of 7 nm quenched at 250 and 320 °C (temperatures at which no peak was observed with in-situ XRD) confirmed the presence of $\epsilon$-$Ni_5Ge_3$ (Paper I).

### 4.2.2 Degradation

The minimization of the total energy of the surfaces and interfaces is also limiting the upper end of the process temperature window. At elevated temperatures, otherwise homogeneous NiGe layers form voids and ultimately even

disconnected islands (Figure 4.5), which is accompanied by an increase in sheet resistance. This so-called agglomeration negatively affects device performance, power consumption and reliability. As the driving force for agglomeration increases with decreasing NiGe thickness, thinner layers agglomerate at lower temperatures [82], [94].

In order for a film to agglomerate, atomic transport is necessary. As diffusion is usually faster on the surface and along grain boundaries, a strategy to suppress agglomeration is the addition of elements with higher melting points that can inhibit this diffusion. In Paper II, Ta and W interlayers and capping layers ranging from 0.2 to 3.0 nm in thickness are deposited along with Ni. The addition of these layers influences the temperature process window for NiGe as indicated by the measured $R_{sh}$ after RTP (Figure 4.5). The highest retardation of agglomeration was found for a 1 nm thick W interlayer. By this, the NiGe agglomeration could be retarded by up to 100 °C. Despite the initial position of Ta and W, both elements are found on top of NiGe after annealing as confirmed by RBS (cf. Figure 3.8), APT, and TEM. When Ta and W are deposited as an interlayer between Ge and Ni, the NiGe formation gets retarded to higher temperatures since the initial Ni diffusion towards Ge gets inhibited. Interlayers of 2 nm W even suppress the NiGe formation completely by acting as a diffusion barrier. Due to the retarded NiGe formation, the process temperature window is at best shifted when using interlayers, whereas it can be enlarged when using W and Ta capping layers.

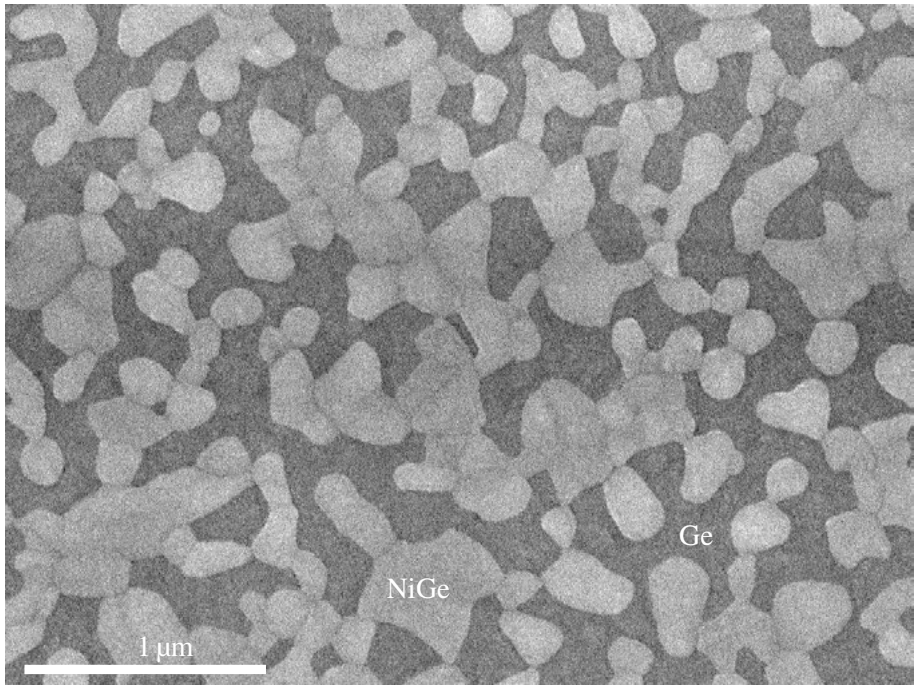



*Figure 4.5.* Top-view SEM of a 6 nm thick Ni film on Ge after RTP at 500 °C. The NiGe has agglomerated into disconnected structures.

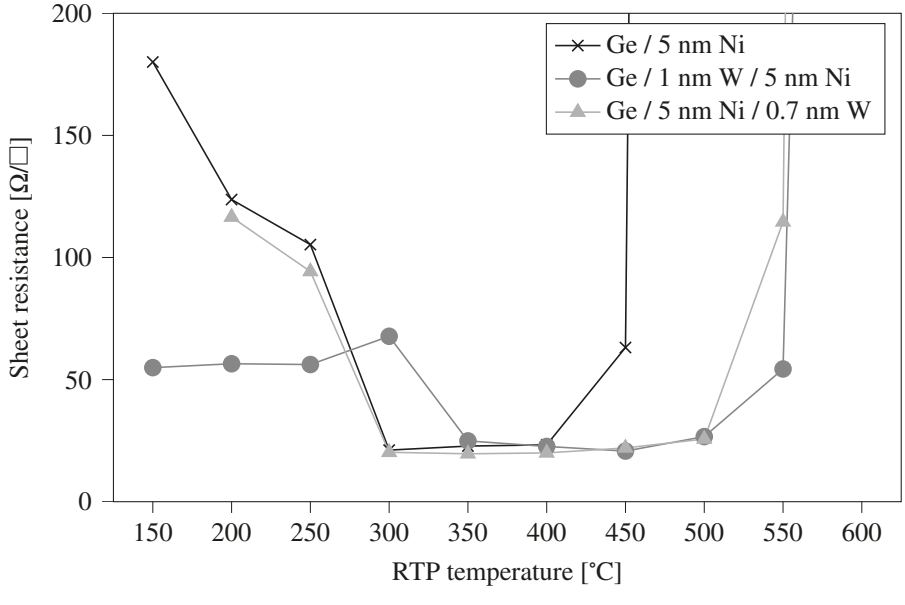



*Figure 4.6.* The addition of a W interlayer or capping layer can retard the agglomeration of NiGe by 100 °C. The W interlayer, however, also retards the formation of NiGe by 50 °C. Adapted from Paper II.

# 5. Contact resisitivity measurements

While the low sheet resistances of NiGe films presented in the preceeding chapter are promising, the more relevant parameter to benchmark the contact is the specific contact resistivity $\rho_c$, which is defined as

$$\rho_c = R_c \cdot A, \tag{5.1}$$

where $R_c$ is the contact resistance and $A$ is the contact area. In this chapter, a measurement structure for determining $\rho_c$ with high precision is introduced (section 5.1). Even though the structure had been demonstrated on Si before [95]–[98], the way to a successful integration on Ge was paved with many obstacles. In section 5.2 the main challenges are elucidated, and the established process flow is discussed. The measurement methodology is described in more detail in section 5.3 and results are shown in section 5.4 and Paper III.

## 5.1 Measurement structures

In the transmission line model (TLM) structure, the voltage drop $V$ between two neighboring contacts of width $W$ and spacing $d$ is measured for a known current $I$. The resistance $R_T = V/I$ is the sum of twice the contact resistance and a series resistance originating from the semiconductor substrate. By measuring $R_T$ for different $d$, several parameters can be obtained from the linear fit. The slope is equal to $R_{sh}/W$, the intercept with the ordinate is $R_c$, and the intercept with the abscissa is $-2L_T$. For $L \geq 1.5L_T$, the specific contact resistivity can then be calculated as

$$\rho_c = R_c W L_T, \tag{5.2}$$

and for $L \leq 0.5L_T$ as

$$\rho_c = R_c W L. \tag{5.3}$$

Often the smallest contact spacing $d$ is in the micrometer range. Then, the extrapolation has to occur over a large distance which causes the uncertainty of $\rho_c$ to be rather big. It is possible to fabricate TLM structures with smaller $d$ (nano-TLM) [99], but this requires the use of chemical mechanical polishing (CMP).

The cross-bridge Kelvin resistor (CBKR) allows for a more direct extraction of $\rho_c$ than the TLM method. As illustrated in Figure 5.2, a current $I$ is driven

between terminals 1 and 2, while the voltage difference is measured between terminals 3 and 4. The contact resistance $R_c$ is given by

$$R_c = \frac{V_3 - V_4}{I} \tag{5.4}$$

and $\rho_c$ can be calculated using Equation 5.1. Here, it is assumed that the voltage drop along the semiconductor can be neglected. Current crowding around the contact, due to the overlap $\delta$, causes an overestimation of $\rho_c$ [100].

To avoid some of the aforementioned limitations, the e-contact method that is shown in Figure 5.3 is used to determine $\rho_c$ in this thesis work [95]. A current is forced between the terminals $I^-$ and $I^+$, while the potential difference is measured between the terminals $V_1$ and $V_2$. Using this four-probe configuration eliminates parasitic resistances as much as possible, so that the measured resistance $R$ is given by the sum of the contact resistance $R_c$ and the spreading resistance $R_{sp}$ as

$$\begin{aligned} R &= R_c + R_{sp} \\ &= \frac{4\rho_c}{d^2} + C\frac{\rho_s}{d}, \end{aligned} \tag{5.5}$$

where $\rho_s$ is the substrate resistivity, $d$ is the contact diameter, and $C$ a correction factor. Thus, the contact resistance is proportional to $d^{-2}$ and the spreading resistance is proportional to $d^{-1}$. For big contact lengths, $R$ is dominated by the spreading resistance, whereas for small contact lengths, $R$ is dominated by the contact resistance. Measuring $R$ for different contact diameters $d$ allows the extraction of $\rho_c$ as shown by the log-log-plot in Figure 5.4. Compared to TLM and CBKR the e-contact method allows for more precise measurements and simpler fabrication and is thus choosen for this work.

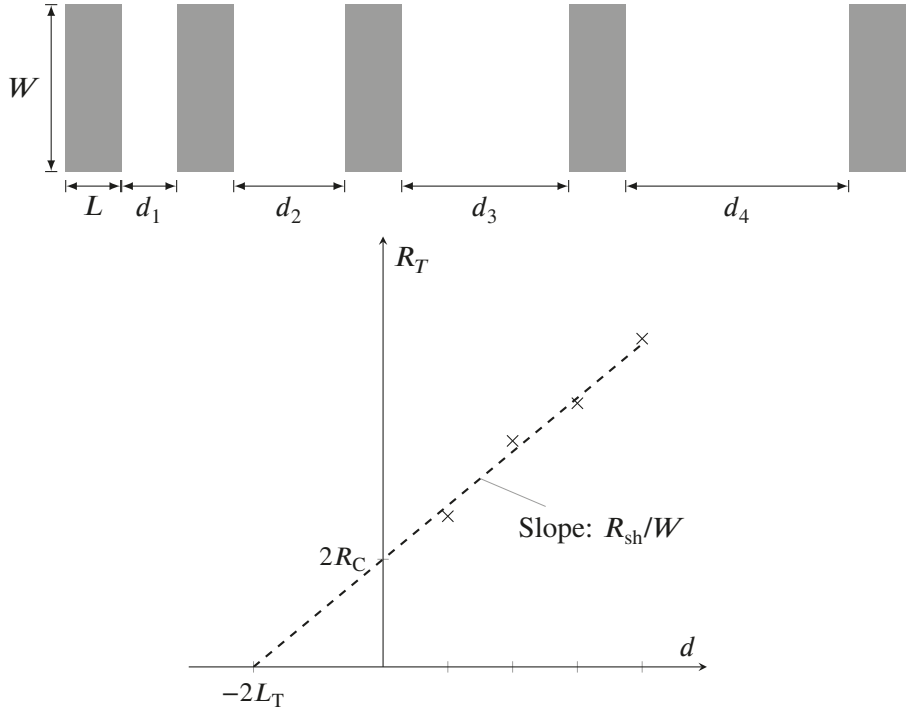



*Figure 5.1.* TLM structure.

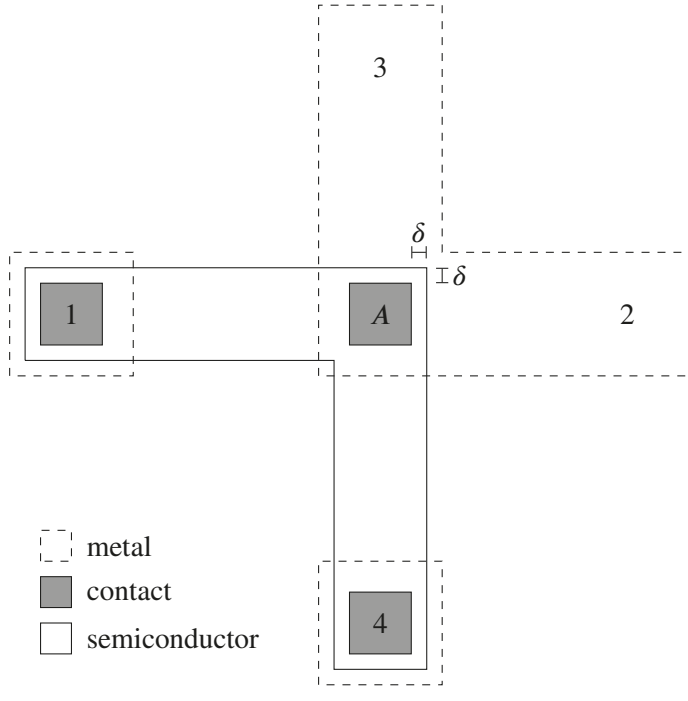



*Figure 5.2.* CBKR structure.

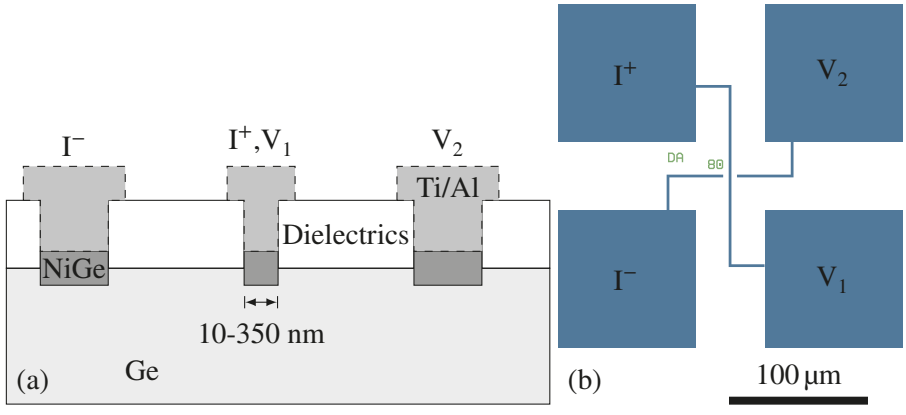



*Figure 5.3.* E-contact measurement structure. (a) Schematic cross-section, (b) mask layout top-view.

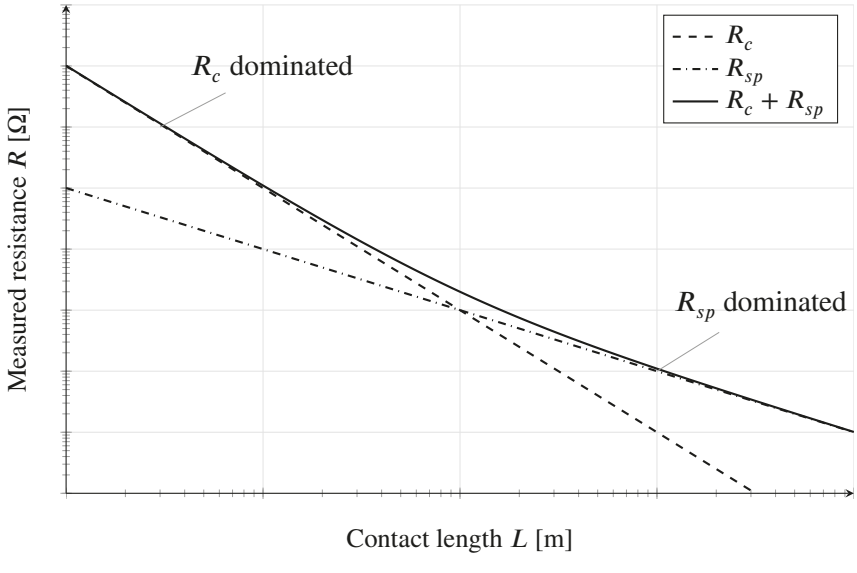



*Figure 5.4.* E-contact method, log-log plot.

## 5.2 Integration with Ge

For Si- and SiGe-based circuits the e-contact method shown in the previous section was firstly demonstrated by Ohuchi *et al.*[95] and was later adapted to extract $\rho_c$ as low as $4 \times 10^{-10}\,\Omega\,\mathrm{cm}^2$ [96]–[98]. On Ge-substrates such structures are realized for the first time in Paper III. Two major challenges were faced during the realization on Ge. Firstly, a compatible high quality dielectric had to found (subsection 5.2.1). Secondly, process flows for the fabrication of small contact holes had to be established in-house (subsection 5.2.2). The final process flow is described in subsection 5.2.3.

### 5.2.1 Dielectrics

A high quality of the dielectrics is essential for the proposed measurement structure. A single pinhole in the dielectric can provide a leakage path that will lead to an underestimation of the contact resistance. At the same time, the dielectrics cannot be too thick either as otherwise the aspect ratios of the contact will become too big to be properly etched or filled.

The reported implementations based on Si and SiGe use $Si_3N_4$ films grown by low-pressure chemical vapor deposition (CVD) [95]–[97]. This process [101], [102] is, however, not compatible with Ge as it severely deteriorates the surface (Figure 5.5), supposedly due to a reaction of Ge with the precursors $SiH_2Cl_2$ and $NH_3$ or due to Ge oxidation and subsequent GeO during the loading/unloading of the substrates into the furnace. In this work, an insulator stack consisting of 5 nm $SiO_2$ grown by atomic layer deposition (ALD) and 20 nm $Si_3N_4$ grown by plasma-enhanced (PE) CVD at 400 ˚C was used. Figure 5.6 shows the measured resistance in dependence of the nominal contact hole diameter using an as-deposited $SiO_2/Si_3N_4$ stack. While a trend demonstrating a hole-diameter dependent resistance is emerging for bigger holes, many data points exhibiting lower resistance are present as highlighted by the triangle. The reason is not an error in hole diameter, but rather that the as-deposited $Si_3N_4$ layer is electrically leaky as was confirmed by additional measurements on unpatterned $Si_3N_4$ layers. In order to densify the $Si_3N_4$ layer, additional thermal treatments were carried out. On Si test substrates annealing the nitride layers at 600 to 700 ˚C in $N_2$-atmosphere for 30 s using RTP (RTP-600S by Modular Process Technology Corporation) was sufficient to suppress the leaking. On Ge, however, the same process caused the silicon nitride film to crack and delaminate (Figures 5.7a & 5.7b). The most likely explanation for this behavior is Ge substrate loss by desorption of GeO as described in section 2.3. Annealing in another RTP tool (Mattson 100 RTP Systems) equipped with an oxygen sensor ensuring $O_2$-levels below 2 ppm could not suppress the film cracking either. Eventually, the insulator stack was annealed in $H_2$-atmosphere at 700 ˚C using an ASM Epsilon 2000, which provided an oxygen-free environment and led to a uniform, non-leaking insulator-stack (Figure 5.7c).

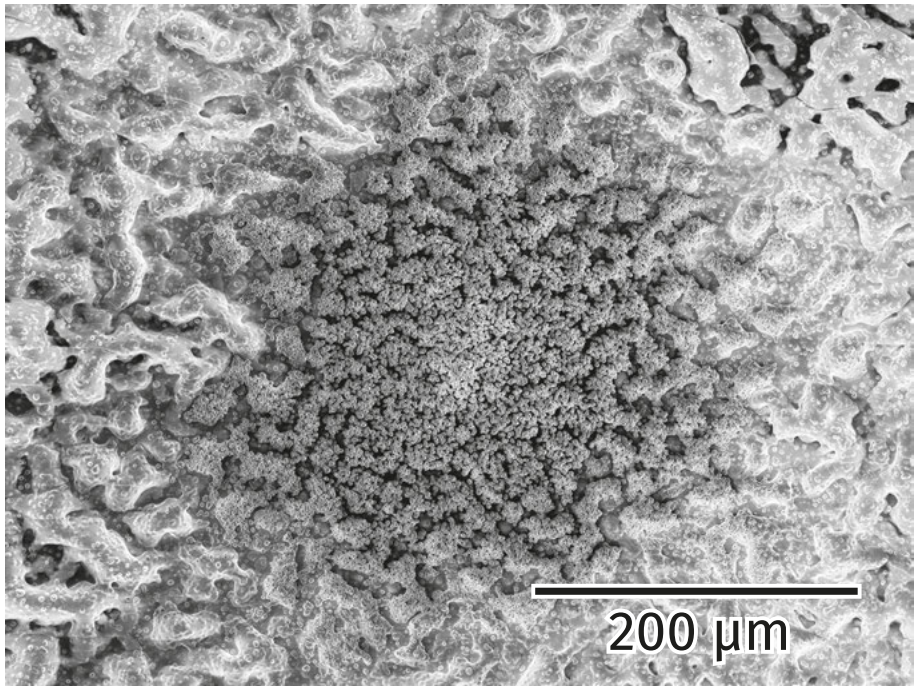



*Figure 5.5.* Trying to grow $Si_3N_4$ on Ge using a low-pressure CVD process leads to artistically appealing but otherwise useless surfaces.

### 5.2.2 Electron beam lithography

Electron beam lithography (EBL) is used for defining the contact holes and contact pads of the measurement structure illustrated in Figure 5.3. A field electron emission source is used to emit electrons. The electrons are focused on and steered across the sample by a system of electrostatic and magnetic lenses. The sample stage can be moved with a precision in the nanometer-range as well. The sample itself is coated with an electron-sensitive resist. Where exposed to the electron beam, the resist changes its solubility towards a solvent (developer) [103]. Sub-10 nm resolutions were demonstrated with the tool used in this thesis [104]. Exemplary SEM micrographs of lines and holes patterned in negative and positive resist, respectively, are shown in Figure 5.8.

Crucial for achieving small contact holes with reproducible dimensions is the quality of the alignment marks. As shown in Figure 5.9a, the alignment on a mark occurs in two steps. Firstly, the location of the mark is determined by scanning across the whole mark vertically and horizontally. Secondly, the beam is focused by repeatedly scanning along the edges. The positions and focus values of the respect alignment marks are used as reference points on the sample and to correct for rotation, tilt, and scaling. High quality alignment marks have well-defined sharp edges with a high contrast towards the electron beam. From low quality alignment marks it is not possible to obtain repro-

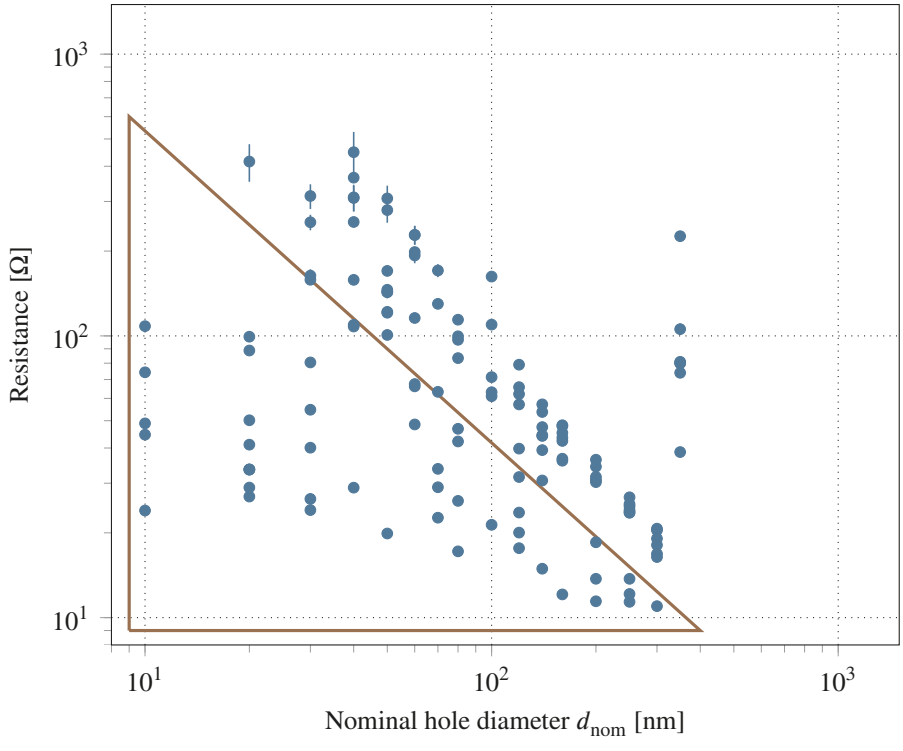



*Figure 5.6.* Resistance measurements using the e-contact method on a sample without annealing the $SiO_2/Si_3N_4$ insulator stack. The relatively low resistances of the data points inside the triangle are caused by leakage through the insulator stack.

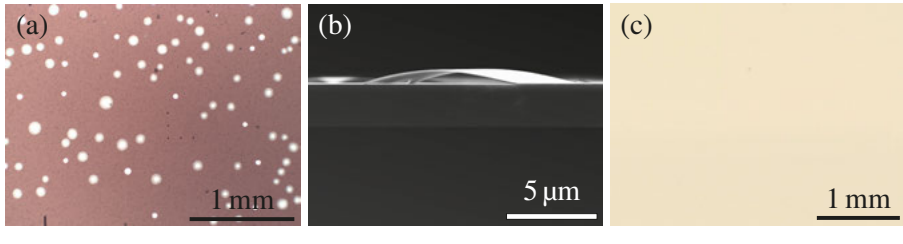



*Figure 5.7.* After annealing using RTP, the $SiO_2/Si_3N_4$ stack on Ge cracks and delaminates, as shown by the top-view optical microscope image in (a) and the XSEM micrograph in (b). Annealing in $H_2$-atmosphere yields a continuous and well-insulating stack as shown by the top-view optical microscope image in (c).

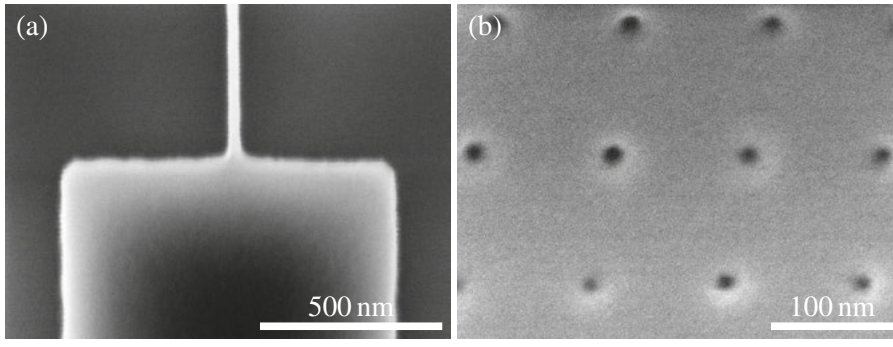



*Figure 5.8.* Top-view SEM micrographs of (a) a pad and a line exposed in hydrogen silsesquioxane and (b) an array of holes exposed in AR-P 6200.09.

ducible focus values. If the focus plane lies too far above the actual sample surface, the exposed structures will appear larger than intended (Figure 5.9b). If the focus plane lies too far below the actual sample surface, the exposed structures will be disconnected (so-called stitching errors, Figure 5.9c). The easiest way to manufacture high quality alignment marks is by evaporating a metal through a patterned mask in a lift-off process. Such metal marks can, however, be incompatible with common process flows. On the one hand, metals are not allowed in many process tools due to contamination risks. On the other hand, the marks might be covered by deposition steps and thus no longer visible during subsequent lithography steps. Therefore, a process for etching alignment marks into Ge was developed.

It is important that the sidewalls of the etched alignment marks be as steep as possible. Otherwise, no reproducible focus is obtained. Furthermore, the marks should have a flat bottom. The best marks on Ge were obtained by reactive ion etching using an Applied Materials Precision 5000 Mark II with a 45 s long etching process (40 sccm $BCl_3$, 30 sccm $Cl_2$, 40 sccm $N_2$, pressure 200 mTorr RF power 600 W) with the resist UV-5 2300-0.5 as a soft mask.

### 5.2.3 Final process flow

The established final process flow from substrate growth to electrical measurements is summarized in Figure 5.10 and described in more detail as follows. First, 2 µm in-situ B-doped Ge is epitaxially grown on n-type Si substrates by reduced pressure CVD using an ASM Epsilon 2000 [105]. Immediately afterwards a 5 nm thick $SiO_2$ layer is grown by ALD followed by the deposition of 20 nm silicon nitride grown by PE-CVD at 400 °C. Subsequently, the sample is annealed in $H_2$-atmosphere at 700 °C for 2 min using the same ASM Epsilon 2000. As these steps proved to be very sensitive towards contamination, they were performed on the same day and the use of tweezers was minimized.

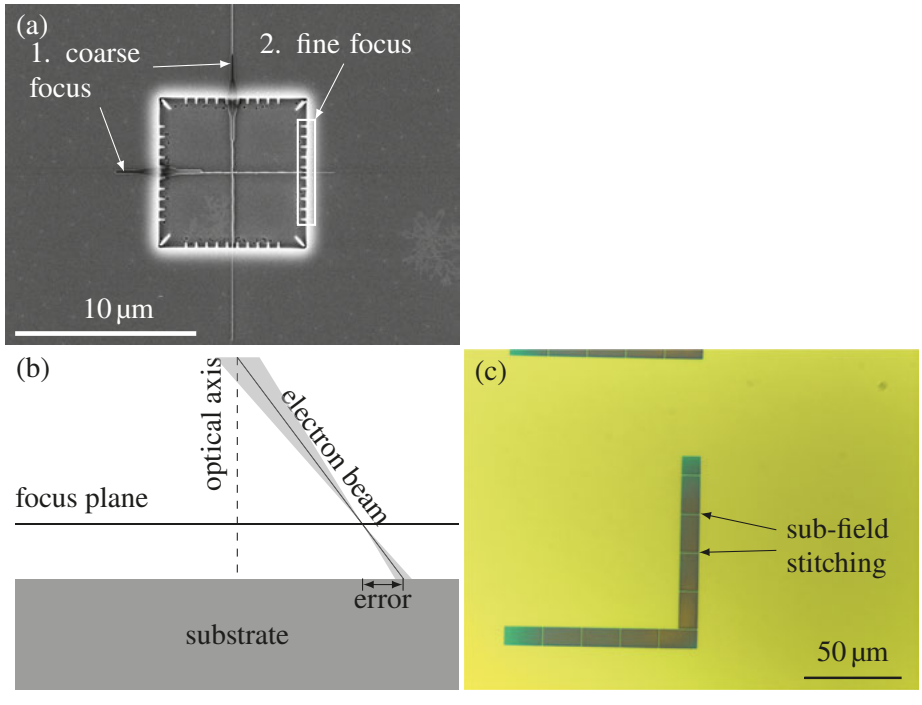



*Figure 5.9.* (a) Top-view SEM micrograph of an etched alignment mark after EBL. The negative resist remains where it was exposed to the electron beam during focusing. (b) Beam widening due to wrong focus. (c) Top-view optical microscope image showing sub-field stitching errors.

For patterning the alignment marks, the positive resist UV-5 2300-0.5 is spin-coated onto the wafer at a spinning speed of 3000 rpm, baked on a hotplate at 130 °C for 2 min, and exposed using EBL with a relatively high beam current of about 7 nA.[1] After exposure the sample is baked on a hotplate at 130 °C for 90 s. The resist in the exposed areas is dissolved in MF-CD-26 (a tetramethylammonium hydroxide based developer), for 60 s before the wafer is rinsed in water for 90 s. The alignment marks are etched by reactive ion-etching (RIE) in an Applied Materials Precision 5000 Mark II using a 20 s silicon nitride etch (5 sccm $CHF_3$, 8 sccm $CF_4$, 5 sccm $O_2$, pressure 50 mTorr, RF power 150 W, magnetic field 5 mT) followed by a 45 s germanium etch (40 sccm $BCl_3$, 30 sccm $Cl_2$, 40 sccm $N_2$, pressure 200 mTorr RF power 600 W). Residual resist is removed in oxygen plasma at 1000 W for 10 min.

Before patterning the contact holes using EBL, the wafer is cleaned in acetone and isopropanol, and the resist AR-P 6200.09 by Allresist is spin-coated at 6000 rpm. For the exposure a beam current of 1.7 nA is used. Then the resist is developed in AR 600-546 by Allresist for 60 s, followed by a 60 s water rinse. The resist is hard-baked at 110 °C for 30 min, before opening the contact holes using the same silicon nitride dry etch described in the previous paragraph. The remaining resist can be removed in oxygen plasma as above or using the remover ARP 600-71 by Allresist.

For the self-aligned contact formation, the samples are first etched in 0.5 % HF for 1 min and then immediately loaded into a von Ardenne CS730S sputtering system, where Ni is deposited using a pulsed DCMS process (150 W, $6 \times 10^{-3}$ Torr Ar atmosphere, pulse frequency 250 kHz, pulse time 496 ns, deposition rate 0.5 nm/s). The samples are annealed to 350 °C for 30 s in $N_2$-atmosphere at a ramp rate of 10 °C/s using RTP. Unreacted Ni is removed in a 10 vol % aqueous solution of HCl at 55 °C for 2 min.

The top contacts are fabricated using a lift-off process. First EBL is used with the same procedure as for the alignment mark fabrication. Prior to thermally evaporating 20 nm Ti and 180 nm Al, the sample is dipped in 0.5 % HF for 30 s. For the actual lift-off the sample is soaked in mr-REM 700 by Microresist at 60 °C for at least 1 h and then rinsed off in water and isopropanol.

To determine the contact size, the contacts formed in the contact hole arrays (see Figure 5.11) are analyzed by means of top-view SEM and cross-sectional TEM. Finally, the devices are measured using a semi-automatic probe station.

[1] At first glance it may seem odd to use EBL for defining the EBL alignment marks. However, for exposing such relatively big structures (8 µm) it is sufficient to focus the electron beam on scratches in the resist at the edge of the wafer. At other stages of this project, alignment marks defined using optical lithography were successfully used as well.

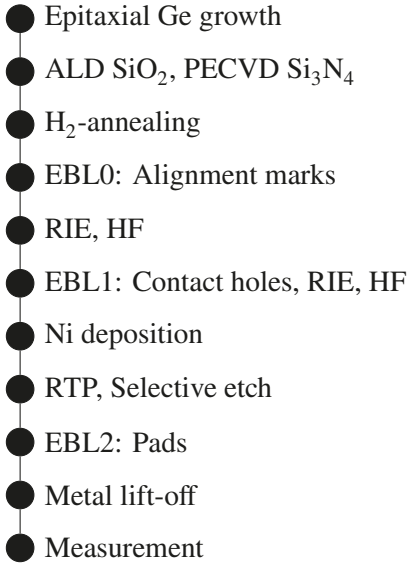



*Figure 5.10.* Established fabrication flow for the e-contact method.

## 5.3 Methodology

The evaluation of the electrical measurements occurs in two steps. Firstly, a profound statistical treatment is needed. Secondly, the effective contact area has to be determined.

Each processed sample creates a huge amount of data that requires a careful treatment. The sample used here contains 1536 devices (4 dies per sample, 16 nominal hole diameter per die, and 24 devices per hole size). Not every device is working. If there is no electrical connection on a device—due to misalignment, failed contact hole etching or failed contact hole filling, for example—just noise is measured. These measurement are discarded, if the ratio of standard deviation to mean value of the resistance exceeds 0.1. The other possible error that can occur are leaking devices. A single pinhole in the dielectric might have been metallized and provide a leakage path. This can lead to an underestimation of the resistance or to treating an otherwise broken device as a working one. Each die contains a set of contact pads to get an idea about the overall likeliness of leakage.

To get a better impression of the distribution and to identify outliers, boxplots as shown in Figure 5.12 are used. The box contains 50 % of the measured devices and the line inside the box denotes the median value. The whiskers denote the upper and lower limit of the devices that are within 1.5 times of the box width. Devices below or above these whiskers are considered outliers.

The biggest uncertainty for the determination of $\rho_c$ is the actual contact area. To determine it, first top-view SEM micrographs are taken for about 10 contacts per $d_{nom}$. The contact area is measured based on the contrast and ex-

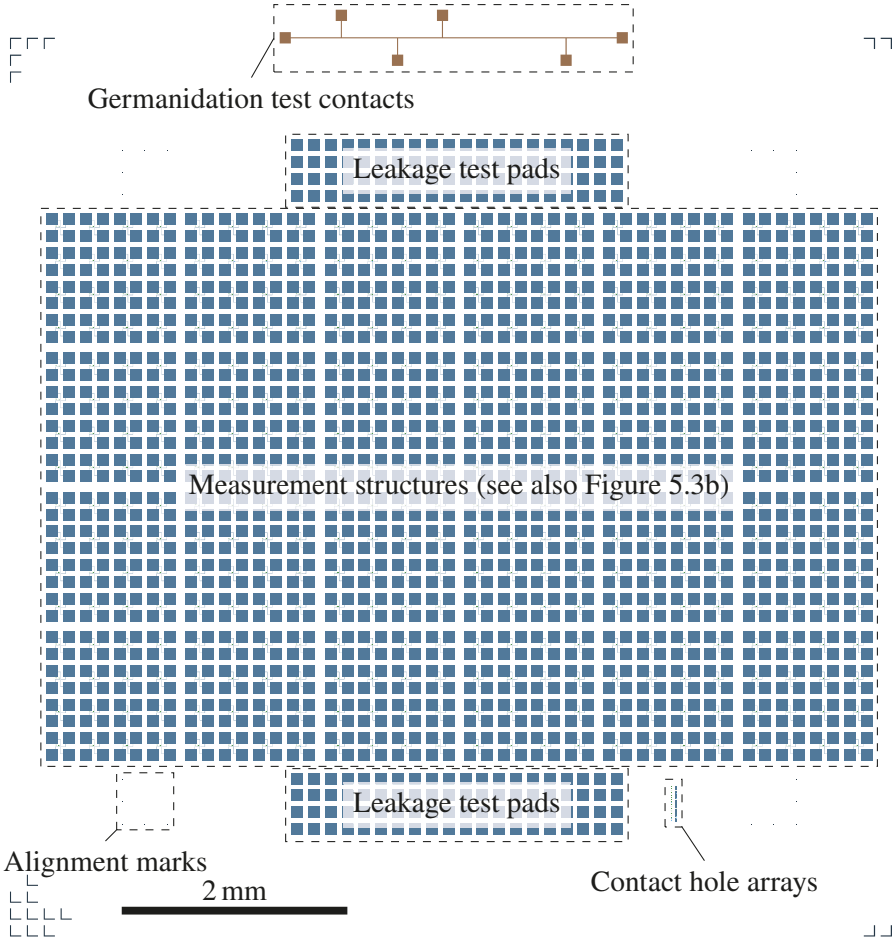



*Figure 5.11.* Final mask layout for the e-contact method.

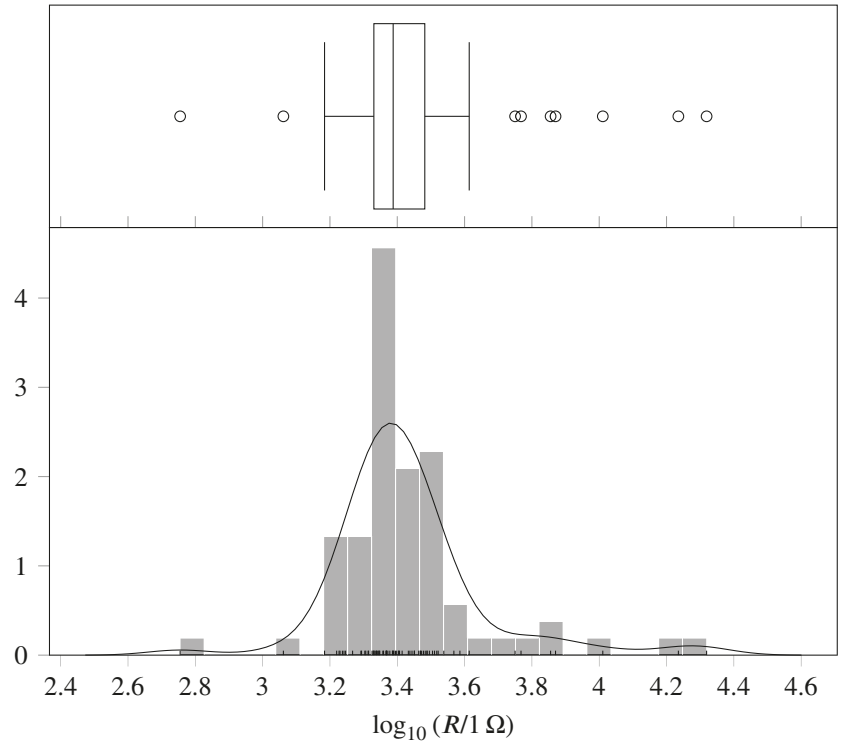



*Figure 5.12.* Distribution of the measured resistances and corresponding boxplot for contacts with a $d_{\mathrm{nom}}$ of 80 nm.

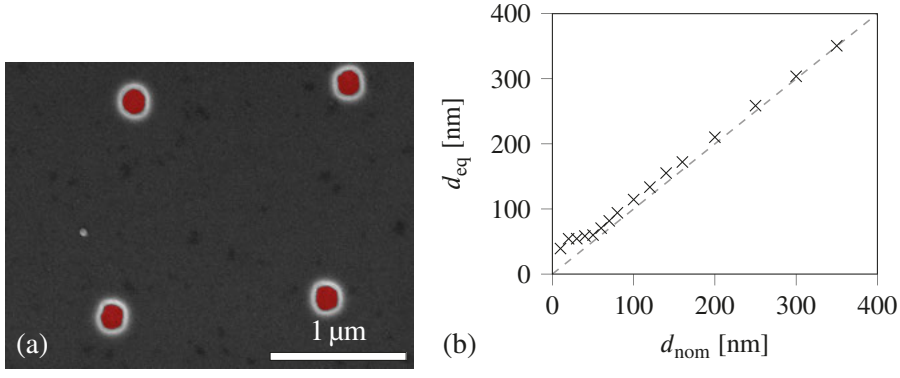



*Figure 5.13.* (a) Top-view SEM of contact holes with a nominal diameter of 160 nm after self-aligned germanidation. The red mask highlights the area used for determining the equivalent hole diameter. (b) Equivalent hole diameter $d_{eq}$ vs. nominal hole diameter $d_{nom}$.

pressed as $d_{eq}$ (Figure 5.13). To also account for the actual shape of the contact holes being non-planar, cross-sectional TEM is used. The contacts are approximated as truncated cones and the shape-corrected area is expressed as $d_{eff}$.[2]

## 5.4 Results

The measured resistance is dependent on the hole diameter (Figure 5.14). Considering the median values alone, the expected contact-resistance dominated regime can already be surmised. The spread of the measured resistance, however, varies greatly and requires further scrutiny. While bigger holes have a very narrow distribution of the measured resistance, the whiskers of the smaller holes extend over several orders of magnitude.

The yield per nominal holesize shows that devices with smaller holes are more likely to fail (Figure 5.15). In other words, the number of devices used for the boxplots of smaller holes is much lower. Aggregating the measurements for comparable $d_{eq}$ (the overlapping boxplots in Figure 5.14), does not reduce the spread, which suggests that poor statistics alone are not responsible for the spread.

The scanning transmission electron microscopy (STEM) cross-section of a wider contact shows that the contact is slightly recessed into the germanium substrate, but that a continuous NiGe contact is formed and properly metallized by Ti/Al (Figure 5.16). A comparable cross-section of a smaller contact

[2] Ohuchi *et al.* assume ellipsoidal contacts, which certainly is a better approximation [95]. More cross-sections of different hole diameters are needed to correct the contact area more reliably. As shown in section 5.4, improving the contact hole etch and the metallization is more important at this stage.

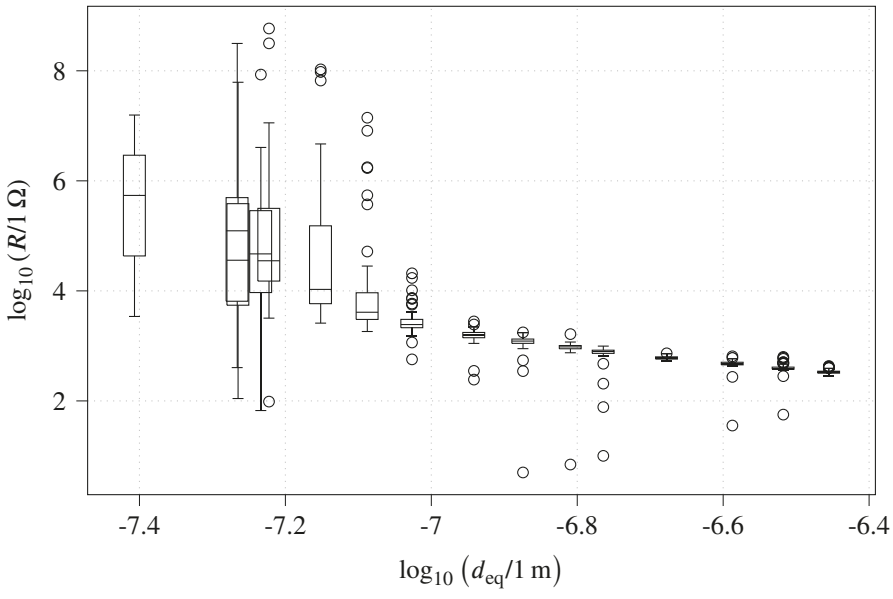



*Figure 5.14.* log-log boxplot of the measured resistance $\boldsymbol{R}$ in dependence of the equivalent hole diameter $d_{\mathrm{eq}}$.

shows that Ti and Al do not properly reach the NiGe contact at the bottom (Figure 5.17a). As the upper part of the NiGe is still connected, the measurement on this particular hole contact will most likely still yield a working device. The actual contact area is hard to define here and it takes little imagination to understand that such improper filling might cause a big spread in resistance. An improperly formed contact in a wider contact hole as shown in Figure 5.17b will most likely be considered as an outlier.

The recess of the contacts into Ge is most likely caused by an excessive contact hole etch. Reducing the etching time should not only reduce the recess but also lower the aspect ratio of the smaller contact holes. This should allow for a better metallization by electron-beam evaporation. Another way to improve the metallization is to change the metallization process to electroplating or to sputtering in combination with CMP.

Due to the observed problems in metallization and the big uncertainty of the resultant measurements, holes with $d_{\mathrm{eq}} < 80\,\mathrm{nm}$ are disregarded in the further analysis. Besides that, the smallest holes are not needed for the extraction of the specific contact resistivity at these substrate dopant levels. For the sample shown in Figure 5.18 a $\rho_{\mathrm{c}}$ of $2.6\,\Omega\,\mathrm{cm}^2$ with lower and upper boundaries of 1.8 and $4.8\,\Omega\,\mathrm{cm}^2$, respectively, can be extracted.

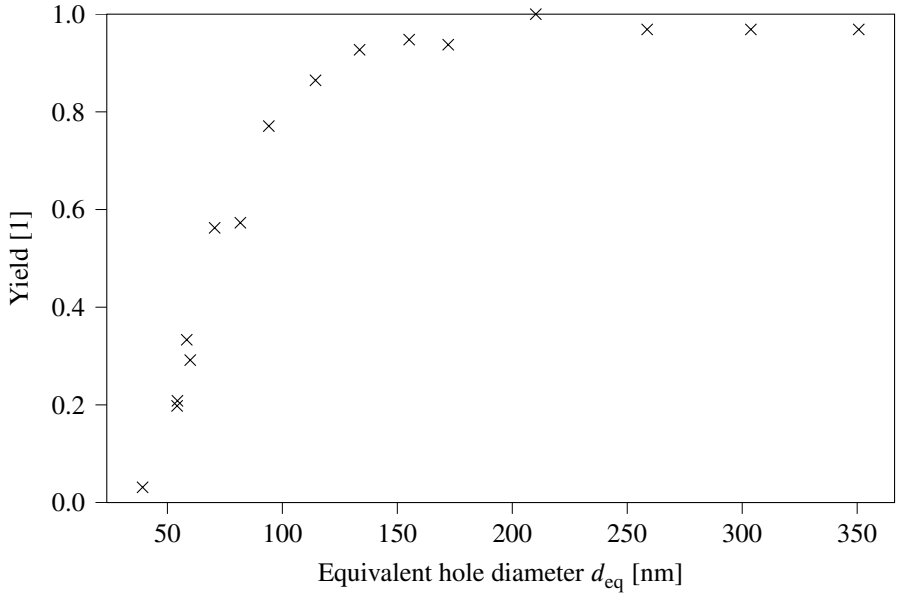



*Figure 5.15.* Yield in dependence of the equivalent hole diameter. Each datapoint is based on measurements on 96 different devices.

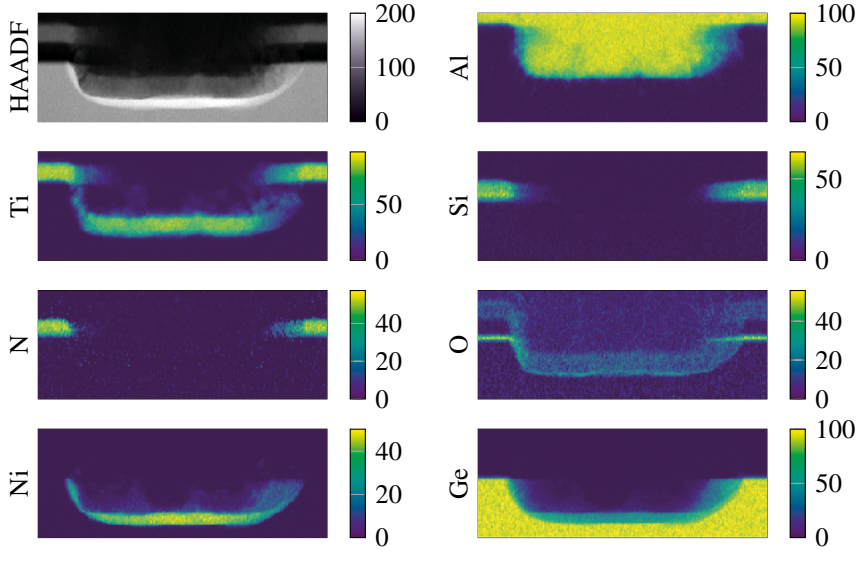



*Figure 5.16.* HAADF-STEM micrograph and respective EDS maps of a contact hole with $d_{nom} = 250\,nm$.

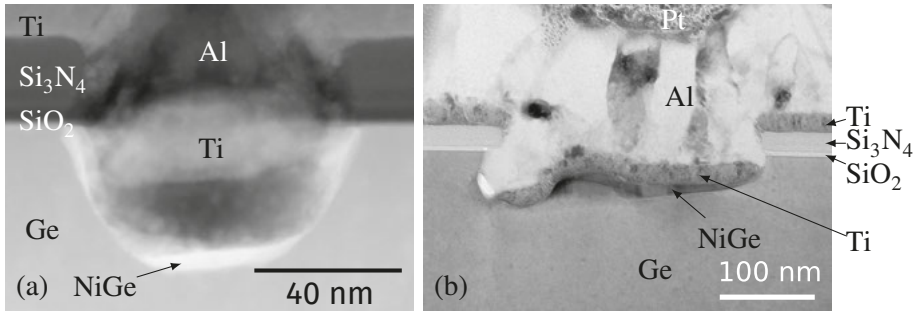



*Figure 5.17.* Examples for improperly formed contacts. (a) STEM micrograph ($d_{\mathrm{nom}}$ = 50 nm), (b) TEM micrograph ($d_{\mathrm{nom}}$ = 250 nm).

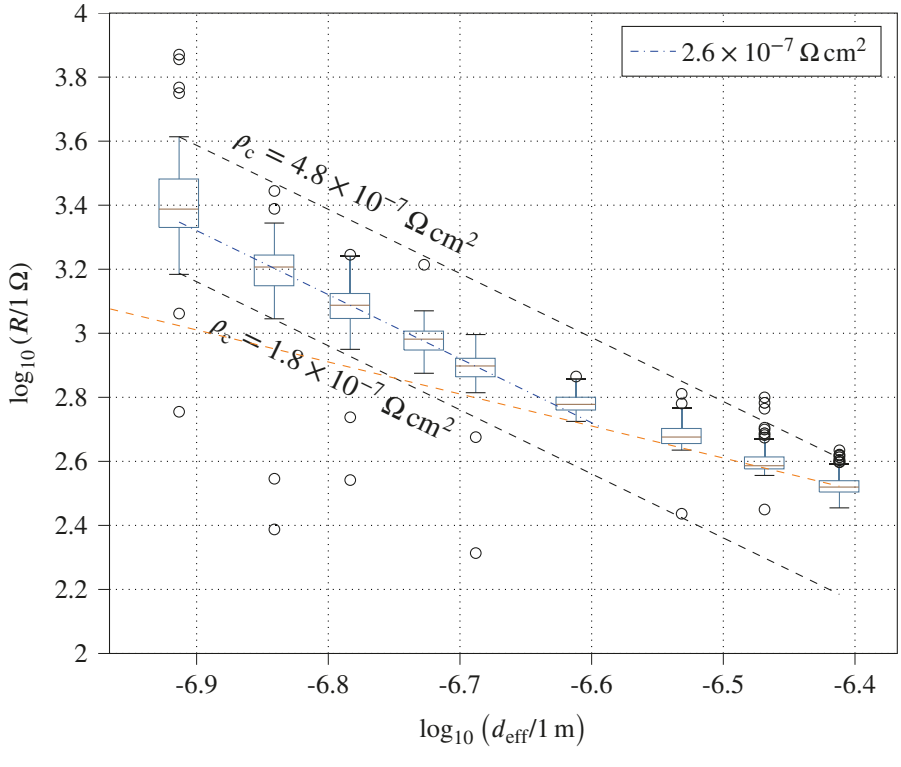



*Figure 5.18.* Extraction of $\rho_c$. To correct for the actual contact area truncated cones with a height of 35 nm and an angle of 60° between base and sidewall were assumed. On this scale not all outliers are visible.

# 6. Interconnects

High resistance in the interconnects and the ensuing increase in dissipated power can easily become the performance bottleneck in extremely scaled 3D- and 2D-ICs. The main reason for the increased resistivity at downscaled dimensions is the increased influence of surface scattering (section 6.1). One approach to reduce the interconnect resistance is to replace Cu—the preferred interconnect material since its first introduction by IBM in 1997 [106]—with an interconnect material better performing at these dimensions. We investigated Co as an alternative to Cu for two reasons: firstly, for its shorter electron mean free path $\lambda_e$ and secondly for its low electromigration that renders liner layers unnecessary and frees up additional space for the interconnect metal that would otherwise be occupied by liner [107]. The electrical performance of Co thin films is strongly dependent on the deposition technique (Papers IV & V). In section 6.2 the two applied magnetron sputtering variants, direct current magnetron sputtering (DCMS) and high-power impulse magnetron sputtering (HiPIMS), are introduced. The main results of deposited Co films and filled holes with Cu and Co are summarized in section 6.3.

## 6.1 Resistivity

In general, the resistivity of a material increases when one or more dimensions are confined. While the goal of studying interconnects for ICs is of course to fabricate nanowires (confinement in two dimensions), material studies on thin films (confinement in one dimension) can already reveal important material characteristics. The increased resistivity of thin films compared to the bulk resistivity $\rho_0$ of the respective single-crystalline material can be attributed to increased electron scattering at the grain-boundaries and at the film interfaces [108].

The increased resistivity due to surface scattering is described by the Sondheimer model [109]:

$$\rho_s = \rho_0 \left[ 1 - \frac{3}{2\kappa}(1-p) \int_1^\infty \left( \frac{1}{t^3} - \frac{1}{t^5} \right) \frac{1 - e^{-\kappa t}}{1 - pe^{-\kappa t}} \mathrm{d}t \right]^{-1} \tag{6.1}$$

with

$$\kappa = \frac{a}{\lambda_e}, \tag{6.2}$$

where $a$ is the film thickness, and $p$ is a specularity parameter.

The increased resistivity due to grain-boundary scattering $\rho_i$ is described by the Mayadas-Shatzkes model as [110]:

$$\rho_i = \rho_0 \left[1 - \frac{3\alpha}{2} + 3\alpha^2 - 3\alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)\right]^{-1} \tag{6.3}$$

with

$$\alpha = \frac{\lambda_e}{d} \frac{R}{1-R}, \tag{6.4}$$

where $\lambda_e$ is the electron mean free path, $d$ is the average diameter of (columnar) grains, and $R$ is a coefficient for the reflection at the grain-boundaries.

While both, Equation 6.1 and Equation 6.3, are only valid in classical terms, they provide a guideline on how to minimize the resistance in interconnects. Firstly, since both, $\rho_i$ and $\rho_s$, are proportional to $\rho_0$ and $\lambda_e$, a low value of the product $\rho_0 \cdot \lambda_e$ is an indication for a potentially suitable material [107]. Secondly, to further lower the resistivity for a given material, bigger grains (leading to higher $d$) and smoother surfaces (leading to higher $p$) are desirable.

Figure 6.1 illustrates the thin film resistivity of Co and Cu thin films using Equation 6.3 as the bulk resistivity in Equation 6.1. Even though $\rho_0$ of Cu is considerably lower than $\rho_0$ for Co, for thin enough films the resistivity of Co is lower due to the shorter $\lambda_e$ of Co (11.8 nm compared to 39.9 nm [107]). Depending on the assumed grain size $d$, there is a thickness below which Co films possess a lower resistivity than Cu films. For nanowires the influence of surface scattering is even stronger than for thin films [111].

## 6.2 Sputtering

For the deposition of thin-films, magnetron sputtering has become the most important technique. The process conditions are crucial for the quality of the resulting thin films. In the following, the two sputtering variants used in this thesis, DCMS and HiPIMS, are described.

### 6.2.1 Direct current magnetron sputtering

A schematic setup of the process chamber for DCMS is shown in Figure 6.2. A target is mounted on a magnetron and placed inside a vacuum chamber together with the substrate. An inert gas (typically Ar) is introduced into the process chamber [113]. Between the target and the chamber walls an electric field is applied so that the sputtering target acts as a cathode for a glow discharge. Ions are accelerated towards the cathode creating secondary electrons. These electrons get accelerated away from the cathode, gain energy, and ionize additional atoms. Eventually a plasma is formed. The magnetic field is used to confine the electrons to the vicinity of the target thus increasing the plasma

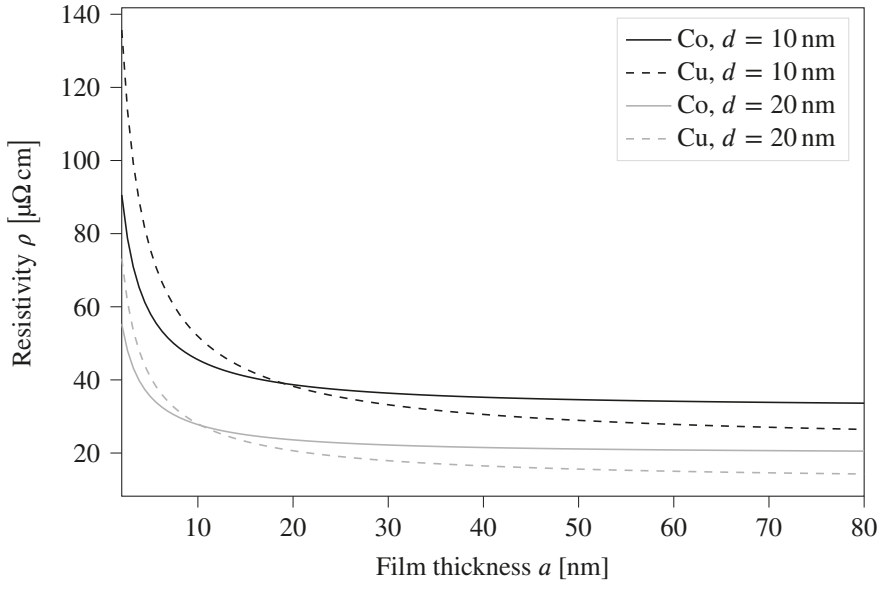



*Figure 6.1.* Simulated resistivity for Co and Cu thin films with two different grain sizes $d$ using Equations 6.1 & 6.3 ($R = 0.7$, $p = 0.2$).

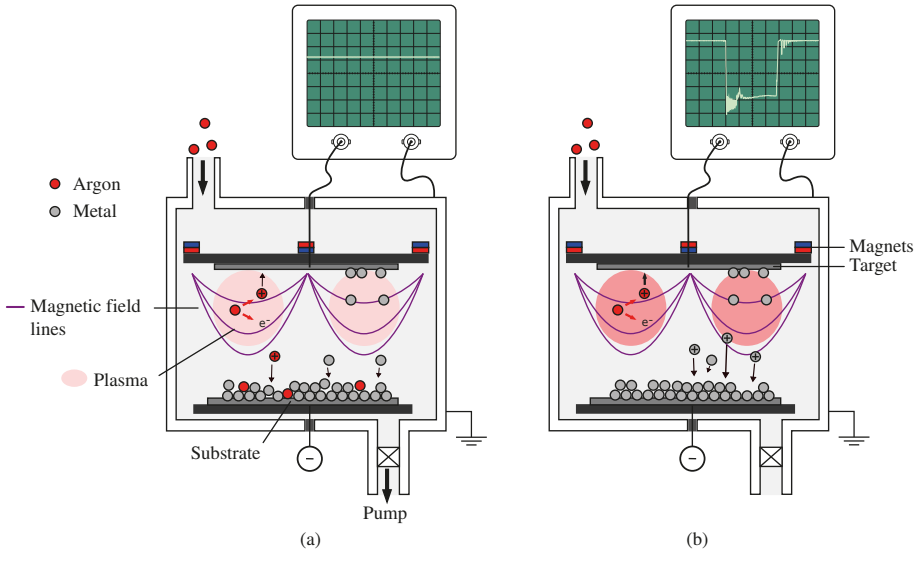



*Figure 6.2.* (a) Direct current magnetron sputtering. (b) High-power impulse magnetron sputtering. Based on [112].

density at a lower pressure. The generated Ar-ions are accelerated towards the target, where they eject ("sputter") atoms and ions from the target. These sputtered species eventually condensate on the substrate and form a film. The widespread use of DCMS is owing to its high deposition rates, good thin film uniformity, and good scalability.

### 6.2.2 High-power impulse magnetron sputtering

HiPIMS is an advancement of conventional DCMS that allows for a higher plasma density and thus an ionization of the sputtered material. Existing vacuum chambers for DCMS can be used for HiPIMS as well—only the connected power supply has to be changed (Figure 6.2b). Instead of providing continuous power to the target, a high voltage of 500 to 1000 V is applied in short pulses of typically 10 to 500 µs at a frequency of typically 10 to 1000 Hz [113]. While the time-averaged power of about 1 W/cm$^2$ is comparable to the one in DCMS, the peak power of about $10^3$ W/cm$^2$ is considerably higher [113]. Despite using a comparable time-averaged power as in DCMS, the plasma density during the pulse-on time in HiPIMS is about two orders of magnitude higher ($\sim 10^{19}$/m$^3$). Thus, the fraction of metal ions in the flux arriving at the substrate is very high (depending on the material up to 90 % [114]). This is the key advantage over DCMS, as the energy and the direction of ions can be controlled by applying additional electric fields.

A typical waveform for a HiPIMS pulse is shown in Figure 6.3. The voltage pulse that is applied to the target causes high ionization. In synchronization with the HiPIMS pulse a bias voltage pulse is applied to the substrate to further accelerate the metal ions. The time of flight before the ions reach the substrate (and give rise to the bias current shown Figure 6.3) causes a substantial part of the deposition to happen during the pulse-off time. The use of HiPIMS for thin film deposition leads to smooth and dense elemental films and is also beneficial for adhesion and the deposition on complex-shaped substrates [113], [115].

## 6.3 Main findings

### 6.3.1 Thin films (Paper IV)

Cobalt films with thicknesses between 6 and 62 nm were deposited onto 260 nm $SiO_2$ on Si wafers using DCMS and HiPIMS at two different substrate bias conditions. The resistivity of these films was found to depend on the thickness and on the sputtering process conditions (Figure 6.4). Going from thick to thin films, the resistivity increased for all process conditions—as is expected given the increased influence of surface scattering described in section 6.1. For comparable thicknesses, the lowest resistivity was found in films deposited at higher substrate biases and when using HiPIMS. In particular, Co films deposited by HiPIMS at a substrate bias of −300 V were the most conductive

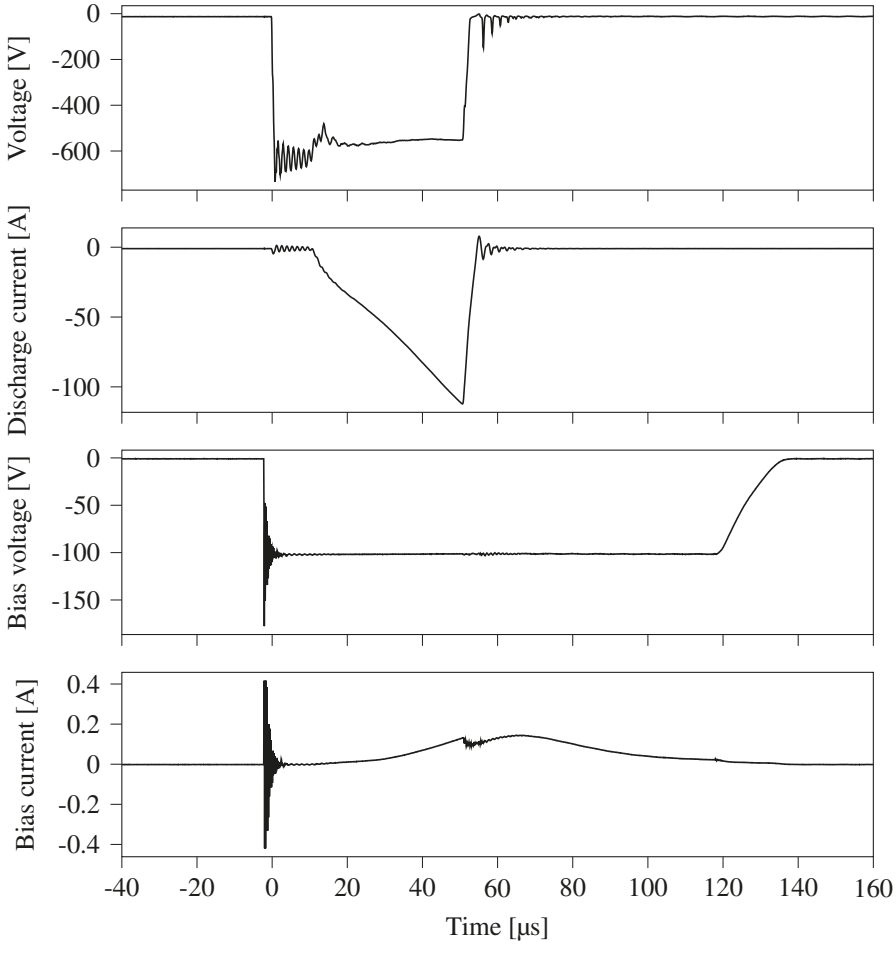



*Figure 6.3.* Waveforms for voltage, discharge current, bias voltage and bias current at a frequency of 100 Hz as used for depositing Co using HiPIMS in Paper IV.

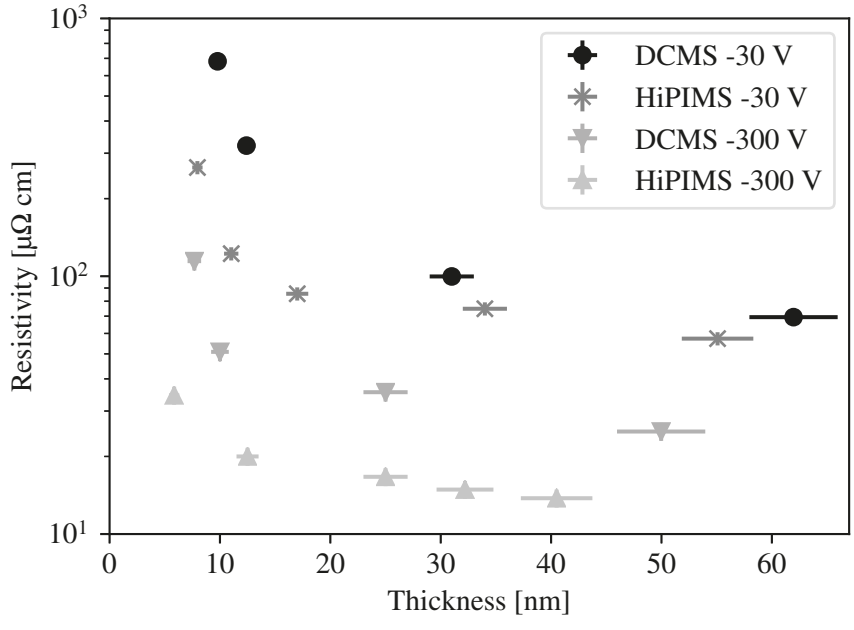



*Figure 6.4.* Resistivity of Co films depending on film thickness and process conditions. Adapted from Paper IV.

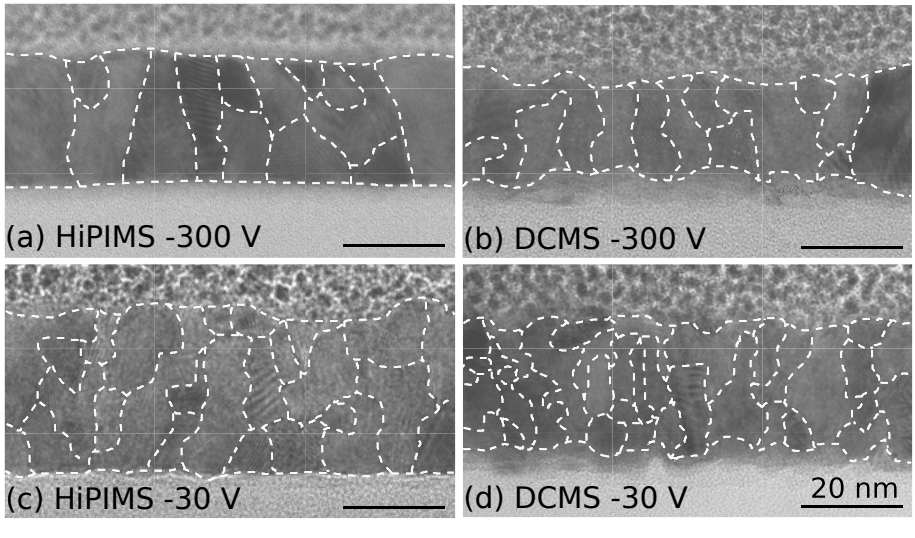



*Figure 6.5.* TEM micrographs of selected Co films on $SiO_2$ with manually added dashed lines highlighting the grains. The use of HiPIMS over DCMS as well as higher substrate biases leads to bigger grains and smoother interfaces. Reprinted from Paper IV, with the permission of AIP Publishing; not licensed under CC BY-SA 4.0.

ones. The cross-sectional TEM micrographs shown in Figure 6.5 reveal the microstructural differences leading to the observed resistivities: the more conductive films have bigger grains as well as smoother interfaces. The film thicknesses obtained from TEM in combination with the areal densities from RBS measurements (cf. Figure 3.7) allow the calculation of the atomic density of the films. The film deposited by HiPIMS at −300 V has a density in the range of the Co bulk density, whereas the density of the DCMS −30 V film is 30 % lower.

Crucial for the improved film quality is the higher degree of metal ionization during HiPIMS and the consequently greater energetic flux of Co ions arriving at the substrate. The ion energy (a few hundred eV) is high enough to implant ions closely below the surface of the substrate (stopping power: ∼100 eV/nm). This can decrease the difference in surface energies and facilitate the nucleation density leading to both smoother interfaces and denser films (Paper IV) [113], [116], [117]. Additionally, the higher ion energy increases the adatom mobility leading to bigger grains [113], [116], [118], [119]. If the ion energy exceeds the displacement energy, atoms of the growing film can even be resputtered and further increase the film smoothness. While the ion energy is increased by applying higher substrate bias in DCMS as well, the effect is more pronounced in HiPIMS due to the higher ion fraction.

Another observed advantage of having a metal-ion dominated plasma is that less Ar gets incorporated into the films. Ar ions can be neutralized in vicinity of the target and reflected towards the substrate, where they get incorporated in the growing film [120]. Here, incorporated Ar can act as additional electron scattering centers that lead to an increased resistivity [121]. The Ar content measured by RBS in the Co film grown by DCMS at −300 V was 1.1 %, whereas no Ar was detected in the HiPIMS-deposited films.

### 6.3.2 Via filling (Paper V)

With conventional DCMS the filling performance is limited by the pinch-off effect. Before the hole is completely filled, the film growing on the surface outside closes off, thereby creating a void below (Figure 6.6c). The reason is the wide range of incident angles that incoming metal species possess during DCMS. Only a small fraction is able to reach the bottom and the majority of the atoms reaching the hole gets deposited at the top part of the opening. Applying a higher substrate bias improves the degree of filling only a little as the plasma is dominated by neutrals whose direction is not influenced by the electric field. The higher degree of metal ionization in the HiPIMS plasma and the more directed ion flux should be beneficial for filling the holes. Therefore, we investigated the filling of holes with ranging diameters ranging from 10 to 250 nm and a depth of 260 nm comparing DCMS and HiPIMS at different substrate biases as well as Co and Cu. The holes were arranged in an array to

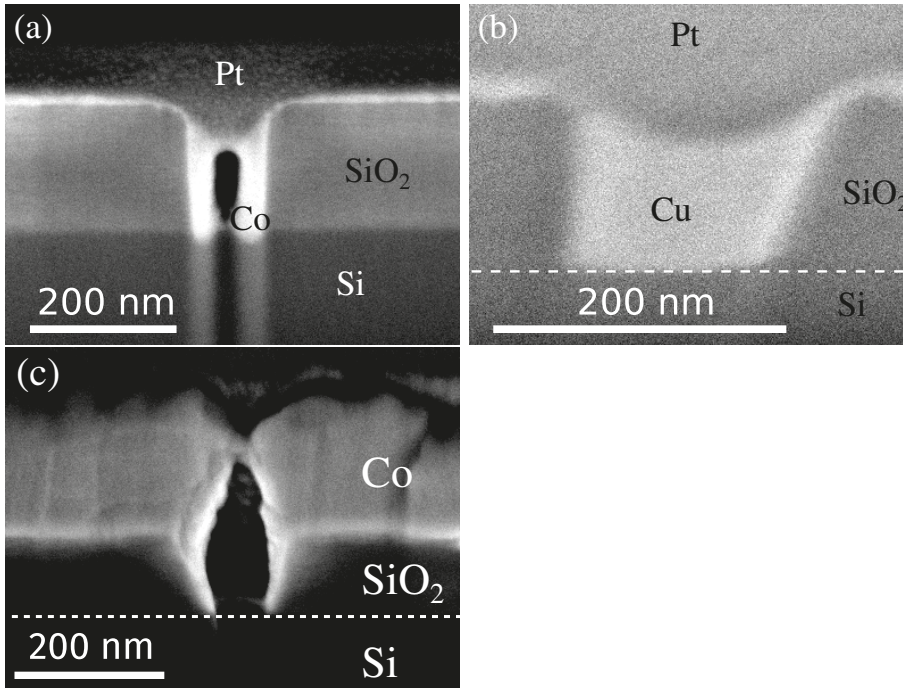



*Figure 6.6.* XSEM images of filled holes. (a) Co HiPIMS −800 V, (b) Cu HiPIMS −400 V, (c) Co DCMS 0 V.

allow for easier cross-sectioning and defined by EBL using the same process conditions as described for the contact hole formation in subsection 5.2.2.

Two main trends were observed. Firstly, the use of HiPIMS does indeed increase the deposition rate at the bottom of the holes. Secondly, the deposition rate on the top, i.e. outside of the holes, decreases with increasing ion energy due to more pronounced resputtering. While these trends were observed for both Co and Cu, the deposition rates and the degree of filling were much lower for Co than for Cu. Figures 6.6a and 6.6b show XSEM micrographs of the best hole fillings that were obtained for Co and Cu, respectively. It should be emphasized that—in an attempt to increase the ion flux at the substrate and thereby the degree of filling as well as to get a more stable discharge—the substrate bias and the pressure in Co HiPIMS were increased from −400 V to −800 V and from 0.5 Pa to 1 Pa, respectively. In addition, stronger magnetic fields were used for sputtering the ferromagnetic Co, which might reduce the ion flux at the substrate by stronger back-attraction of metal ions to the target. A possible way to alleviate this back-attraction (and the starting point for a possible follow-up study) could be the use of weaker magnetic fields. This would require higher discharge voltages which is generally possible, just not with the setup used in this study.

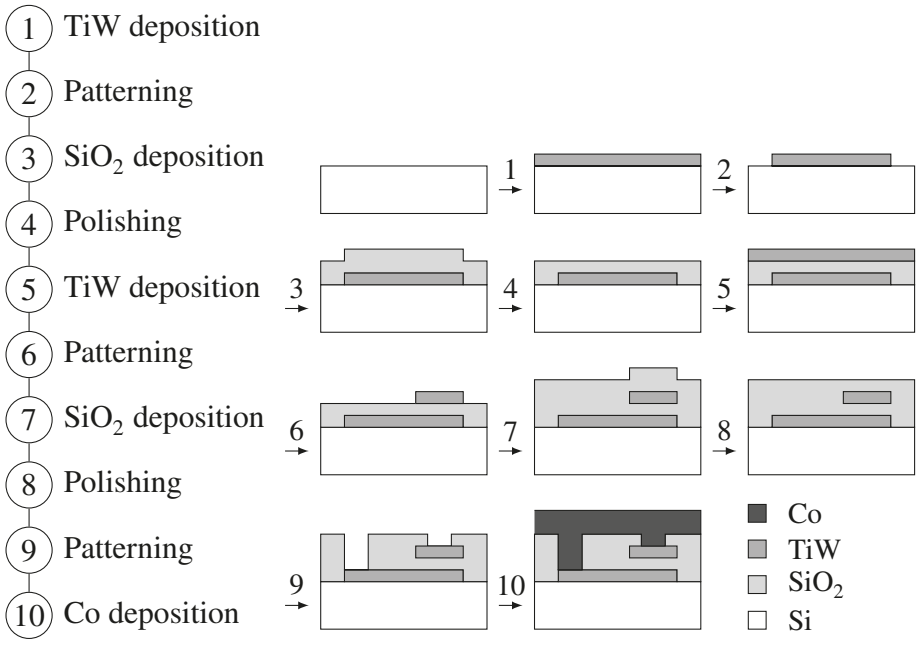



*Figure 6.7.* Process flow for the inter-tier interconnect demonstrator.

### 6.3.3 Outlook

For the realization of 3DICs, the various device tiers need to be interconnected. To demonstrate the Co metallization with HiPIMS, a dummy structure was fabricated according to the process flow in Figure 6.7. The lateral dimensions on this demonstrator are relaxed—the squared contacts have a side length of 1 µm. At these dimensions the two TiW layers could be contacted by Co using a single HiPIMS run without any void formation (Figure 6.8).

In a real Ge-based 3DIC the process flow would be more advanced. Instead of depositing TiW (steps 1 and 5), a Ge substrate would need to be transferred and bonded. The patterning steps (2 and 6) would include the transistor fabrication as well as the (NiGe) contact formation. In the last patterning step (9) the contact hole etch would need to stop on possibly very thin NiGe contacts. As long as no dry etch with acceptable selectivity towards NiGe is available, this etch needs to rely on a time-based stop. Given the different depths, the etching down to the different tiers would need to be done in separate steps to avoid over-etching in the upper tiers. This would mean an additional lithography step per device tier. After the Co deposition, additional patterning steps would follow. If no cobalt dry etch process with suitable selectivity towards $SiO_2$ is found, the fabrication could instead be done by depositing Co into patterned trenches and removing excessive Co by CMP.

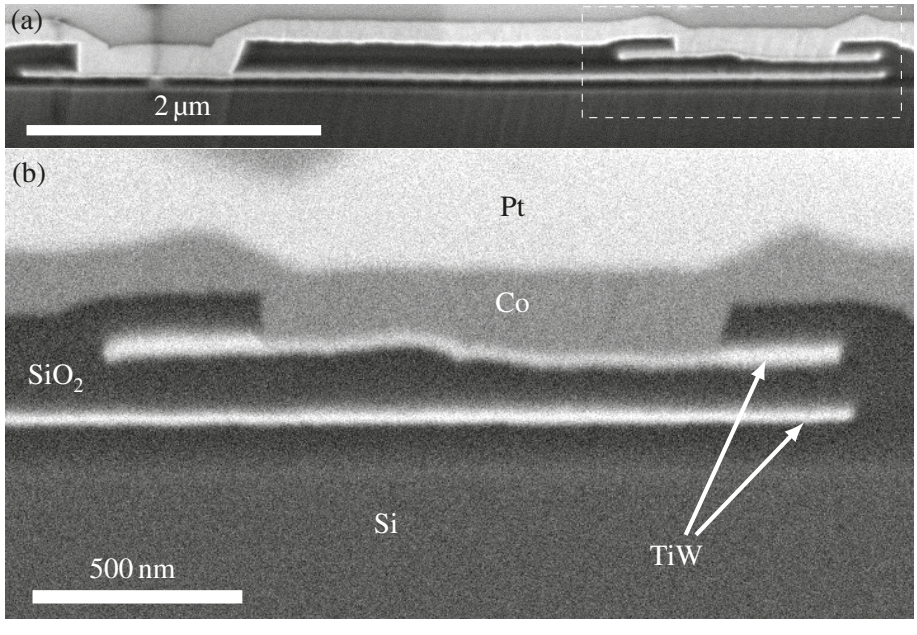



*Figure 6.8.* XSEM-micrographs of Co deposited by HiPIMS onto TiW contacts on two different tiers. (a) Overview using secondary electrons. (b) Close up SEM micrograph of the highlighted region in (a) using back-scattered electrons for better elemental contrast.

# 7. Summary & outlook

Paraphrasing Feynman's quote in the preface, the road to 3DICs can be taken in steps as time goes on. Here, I hope to have taken several of the necessary steps towards integrating the contacts and interconnects into Ge-based 3DICs.

In Paper I the process temperature windows for fabricating thin NiGe films were identified and (synchrotron) light was shed on the phase formation sequence at these thicknesses. The process temperature window was widened by the addition of Ta and W capping layers in Paper II. The platform established for measuring the specific contact resistivity of Ge/NiGe contacts in Paper III can be the basis for more thorough studies of contacts towards germanium. For example, the influences of many different parameters like substrate doping level, contact metals, and surface treatments remain to be explored.

One of the main challenges for extremely scaled ICs of any kind is the high resistance in the local interconnects. Cobalt emerged as a possible replacement for Cu in recent years and is now being used for the smallest local interconnects in the 10 nm node [122]. The study conducted in Paper IV highlights the great potential of Co by demonstrating highly conductive Co thin films deposited by HiPIMS. Key for the high quality of the films is the high degree of metal ionization during the sputtering. It leads to pure and smooth films with relatively big grains. Further advantage of the high degree of metal ionization in HiPIMS was taken in Paper V in which the filling of contact holes with Cu and Co studied. Compared to conventional DCMS, the degree of filling was improved. With the used conditions, the Cu filling outperformed the Co filling, but I am positive that the Co process can be tuned further to completely fill the holes. In the next steps, Co nanowires could be fabricated and Co interconnects be investigated electrically. For this, the recently established tools for ion milling at the Ångström Laboratory and the CMP process for Co at Electrum Laboratory could play a major role.

# Svensk sammanfattning

Den tekniska utvecklingen i halvledarindustrin präglades i årtionden av mantrat om att reducera transistorstorleken i integrerade kretsar. Det finns två slags fördelar med storleksreduceringen: Å ena sida kan klockfrekvensen höjas, å andra sidan kan antalet transistorer per ytenhet ökas. På så sätt förbättras både prestandan och kostnadseffektivitet, vilket är en enorm ekonomiskt drivkraft.

Integrerade kretsar består vanligtvis av ett skikt med aktiva komponenter och flera skikt med metalliska ledare som knyter ihop transistorerna till logiska grindar. Det här byggnadssättet har behållits under utvecklingen i sista decennier. I dagsläget har avstånden dock nått storleksordningar av några få atomer varför en fortsatt storleksreduktion försvåras. De ökande teknologiska och finansiella kostnader som krävs för att driva fram vidareutvecklingen avspeglar sig i också den globala marknadsstrukturen: Endast få tillverkare förmår att genomföra de stora investeringarna och ta de finansiella riskerna för att nå nästa teknologinod.

Ett alternativt sätt för att öka antalet transistorer per ytenhet är tredimensionella integrerade kretsar där transistorer befinner sig inte bara i ett utan i flera som ligger ovanpå varandra. Därmed kan transistorernas täthet höjas utan att deras storlek måste reduceras. Samtidigt kan ledarlängden och medföljande parasitiska motstånd minskas. Även om den här metoden inte är långsökt, är tredimensionella integrerade kretsar ändå relativt outforskade – att följa den tvådimensionella vägen har helt enkelt varit mer lovande. De ovan nämnda ökade kostnaderna för storleksreduceringen har dock återuppväckt intressen för tredimensionella integrerade kretsar.

Framställningen av tredimensionella integrerade kretsar kan principiellt ske på två sätt: Vid den *polylitiska* metoden tillverkas transistorerna med ledare först separat på olika skivor som sedan staplas skivorna ovanpå varandra och kopplas samman. Fördelen med den här metoden är att etablerade processer kan användas. Precisionen med vilken de enskilda skivorna kan passas mot varandra begränsar dock den nåbara integrationstätheten.

Vid den *monolitiska* metoden tillverkas transistorerna skikt på skikt på samma skiva. En sådan process är dock betydligt mer komplicerad eftersom transistorerna i de nedre lagren måste kunna stå emot alla följande steg i tillverkningen. I och med att högre integrationstäthet och att nya standardceller kan realiseras varför forskningsprojektet bakom den här avhandlingen följer monolitiska metoden.

Ett av de största problemen inför realiseringen av monolitiska tredimensionella integrerade kretsar är högtemperaturstegen. De är både essentiella för

aktiveringen av dopningsatomer och kritisk eftersom de kan göra redan tillverkade transistor i de nedre lagern obrukbara. I kisel, som är det vanligaste substratmaterialet kan temperaturen nå 1000 °C och mer. Å andra sidan kan germanium tillverkas vid betydligt lägre temperaturer (<600 °C) så att den monolitiska skikt-på-skikt-metoden verkar möjligt. Dessutom har laddningsbärare i germanium en högre mobilitet än i kisel så att germanium har blivit intressant även för vanliga tvådimensionella integrerade kretsar.

Den här avhandlingen betraktar två essentiella delar av sådana germaniumbaserade tredimensionella integrerade kretsar: kontaktmaterial till germanium transistorer och material för ledarna.

Som kontaktmaterial till germaniumtransistorer är nickelgermanid (NiGe) intressant eftersom den bildas vid låga temperaturer, har en låg elektrisk resistivitet och en hög morfologisk stabilitet. I detta arbete undersöktes reaktionen mellan tunna nickel filmer (<10 nm) och germaniumsubstrat. Först bestämdes temperaturerna vid vilka NiGe bildas respektive vid vilka dessa NiGe filmer agglomereras (artikel I). Eftersom kontaktmotståndet stigar vid både lägre och högre temperaturer krävs kännedomen om dessa temperaturer för att kunna tillverka germaniumtransistorer. I samma artikel udersöktes också reaktionen till NiGe närmare. Det visade sig att nickel filmer som i början är 2 till 9 nm tunna först reagerar fullständigt till $\epsilon$-$Ni_5Ge_3$ innan NiGe bildas. I tidigare arbeten med tjockare nickelfilmer observerades en samtidig tillväxt av båda faser.

För att utöka det tillämpliga temperaturområdet för NiGe undersöktes tillägg av volfram och tantal som mellan- och ytskikt. Oavsett deras ursprungliga position befann sig volfram och tantal slutligen ovanpå NiGe. På så sätt begränsas diffusionen av nickel och germanium så att NiGe agglomererar vid högre temperaturer. Mellanskikt fördröjer också reaktionen till NiGe, dvs NiGe bildas vid högre temperaturer, så att tillämpliga temperaturområdet förflyttas. Den största utvidgningen (100 °C) observerats med ytskikt av 1 nm volfram.

Medan de observerade egenskaper av NiGe är väldigt lovande är den mest relevanta parametern kontaktresistiviteten $\rho_c$. För att bestämma $\rho_c$ krävdes etableringen av en mätstruktur. Tillverkningsmetoden beskrivs i manus III. För en NiGe kontakt till bor-dopad germanium med en dopningskoncentration av $2 \times 10^{17}/\mathrm{cm}^2$ uppmättes $\rho_c$ till $2.6 \times 10^{-7}\,\Omega\,\mathrm{cm}^2$. En uppföljning av detta arbete skulle bygga på den här plattformen och undersöka ytterligare material, processparametrar och dopningar.

Även för ledarna är det intressant att ta alternativa material i betraktande. Eftersom elektriska motståndet i ledarna ökar när deras diameter minskar är reduceringen av detta motstånd en utmaning för både två- och tredimensionella integrerade kretsar. Jämfört med koppar som för närvarande är det förhärskande ledarmaterialet har kobolt en kortare medelfriväg för elektroner så att elektronernas spridningen i små strukturer minskar. Två artiklar i detta arbete behandlar därför koboltmetalliseringen. I artikel IV undersökas koboltbeläggningen med två olika varianter av magnetronsputtring: likspännings magnetronsputtring (DCMS) och högenergiimpulsmagnetronsputtring (HiPIMS).

Koboltbeläggningarna som tillverkades med HiPIMS visade en högre elektrisk ledningsförmåga. Detta resultat återspeglar flera gynsamma egenskaper som högre atomtäthet, större korn, slätare gränsytor och mindre inneslutning av argon. I artikel V undersökas fyllning av kontakthål med koppar och kobolt med HiPIMS närmare. Sammansättningen av partikelflödet vid nedslaget på substratet är avgörande för fyllnadsgraden. En hög andel joner i flödet och en hög jon energi leder fram till de bästa fyllningsresultat.

# Deutsche Zusammenfassung

Die technische Entwicklung in der Halbleiterindustrie war jahrzehntelang von dem Leitsatz geprägt, die Größe der Transistoren in integrierten Schaltkreisen kontinuierlich zu reduzieren. Dadurch konnten sowohl schnellere Taktraten als auch eine höhere Anzahl an Transistoren pro Flächeneinheit erreicht werden. Dies führte zu einer gleichzeitigen Steigerung von Leistungsfähigkeit und Kosteneffizienz – eine enorme wirtschaftliche Triebkraft.

Üblicherweise bestehen integrierte Schaltkreise aus einer Ebene von aktiven Bauteilen und mehreren darüberliegenden Ebenen aus metallischen Leiterbahnen, die die Transistoren miteinander zu logischen Schaltungen verbinden. Dieser generelle Aufbau wurde bei der Weiterentwicklung über die Jahrzehnte beibehalten. Mittlerweile sind die kritischen Dimensionen in der Größenordnung von einigen wenigen Atomen angelangt, wodurch eine weitere Verringerung immer schwieriger wird. Der zunehmende technologische, aber vor allem auch finanzielle Aufwand, der betrieben werden muss, um die Größenverringerung voranzutreiben, spiegelt sich nicht zuletzt in der globalen Unternehmensstruktur wider. Nur wenige Hersteller sind in der Lage die großen Investitionen für die nächsten Technologieknoten zu stemmen und die finanziellen Risiken einzugehen.

Einen alternativen Ansatz, um die Anzahl der Transistoren pro Flächeneinheit zu erhöhen, stellen dreidimensional-integrierte Schaltkreise dar. Hierbei befinden sich die Transistoren nicht nur in einer, sondern in mehreren übereinanderliegenden Ebenen. Folglich kann die Flächendichte der Transistoren erhöht werden, ohne die Größe der Transistoren verringern zu müssen. Zugleich kann durch den dreidimensionalen Aufbau die Länge der Leiterbahnen reduziert werden. Obwohl dieser Ansatz naheliegend ist, sind dreidimensional-integrierte Schaltkreise dennoch relativ unerforscht. Das Weitertreiben der Größenreduktion in lediglich einer Ebene schien schlichtweg vielversprechender. Die Kostensteigerung dieser Größenreduktion haben das Interesse an dreidimensional-integrierten Schaltkreisen jedoch wiedererweckt.

Um dreidimensionale integrierte Schaltkreise herzustellen, gibt es zwei prinzipielle Verfahrensweisen. Bei der polylithischen Methode werden die Transistoren samt Leiterbahnen zunächst auf unterschiedlichen Wafern gefertigt, übereinandergestapelt und anschließend miteinander verbunden. Dies hat den Vorteil, dass man auf etablierte Fertigungsprozesse zurückgreifen kann. Die Genauigkeit, mit der die einzelnen Wafer zueinander ausgerichtet werden können, limitiert letztlich die erreichbare Integrationsdichte.

Bei der monolithischen Methode werden die Transistoren hingegen Lage für Lage auf dem selben Substrat gefertigt. Dieser Herstellungsprozess ist allerdings bedeutend komplizierter, da die Transistoren in den unteren Ebenen mit allen weiteren Prozessschritten kompatibel sein müssen. Prinzipiell können mit der monolithischen Herangehensweise jedoch höhere Integrationsdichten und sogar neuartige Standardzellen realisiert werden, weshalb das Forschungsprojekt hinter dieser Doktorarbeit den monolithischen Ansatz verfolgt.

Eines der größten Probleme für die Realisierung von monolithischen dreidimensionalen integrierten Schaltkreisen stellen Hochtemperaturschritte dar. Diese sind sowohl essenziell, um Dotieratome zu aktiveren, als auch kritisch, da sie die bereits gefertigten Transistoren in den unteren Ebenen funktionsunfähig machen können. Bei Silizium, dem vorherrschenden Substratmaterial in der Halbleiterbranche, können diese Temperaturen 1000 °C und mehr erreichen. Germanium hingegen kann bei deutlich niedrigeren Temperaturen von weniger als 600 °C gefertigt werden, sodass die monolithische Schicht-für-Schicht Fertigung möglich erscheint. Davon abgesehen besitzt Germanium höhere Ladungsträgerbeweglichkeiten als Silizium, sodass Germanium selbst für herkömmliche 2D-integrierte Schaltkreise wieder interessant geworden ist.

Diese Arbeit beschäftigt sich mit zwei essentiellen Teilaspekten solcher dreidimensionaler, Germanium-basierter Schaltkreise: Zum einen mit Kontaktmaterialien für Germaniumtransistoren, zum anderen mit Materialien für Leiterbahnen.

Als Kontaktmaterial für Germaniumtransistoren ist Nickelgermanid (NiGe) aufgrund seines geringen spezifischen elektrischen Widerstandes, seiner geringen Bildungstemperatur und seiner hohen morphologischen Stabilität von Interesse. In dieser Arbeit wurde die Reaktion von dünnen Nickelschichten (<10 nm) mit Germaniumsubstraten untersucht. Dabei wurden zunächst die Temperaturen bestimmt, in denen NiGe gebildet wird bzw. bei denen diese NiGe-Schichten agglomerieren (Artikel I). Da sowohl unter- als auch oberhalb dieser Temperaturen der Kontaktwiderstand deutlich erhöht ist, ist die Kenntnis dieser Temperaturen für die Herstellung von Germaniumtransistoren erforderlich. Im Zuge desselben Artikels wurde auch die Reaktion hin zum NiGe genauer untersucht. Dabei wurde festgestellt, dass Nickel bei anfänglichen Dicken von 2 bis 9 nm zunächst vollständig mit Germanium zu $\epsilon$-$Ni_5Ge_3$ reagiert und erst anschließend NiGe gebildet wird. In früheren Arbeiten mit dickeren Nickelschichten war ein gleichzeitiges Wachstum der beiden Phasen beobachtet worden.

Um den nutzbaren Temperaturbereich für NiGe zu erweitern, wurde der Zusatz von Wolfram und Tantal als Zwischen- und Deckschicht untersucht (Artikel II). Unabhängig von der anfänglichen Position fanden sich Wolfram und Tantal nach abgeschlossener Reaktion oberhalb der NiGe-Schicht. Dies schränkt die Diffusion von Nickel und Germanium ein, sodass NiGe erst bei höheren Temperaturen agglomeriert. Im Falle von Zwischenschichten wird NiGe allerdings auch erst bei höheren Temperaturen gebildet, wodurch sich ledig-

lich eine Verschiebung des nutzbaren Temperaturbereiches ergibt. Die größte Erweiterung des Temperaturbereiches wurde bei Deckschichten aus 1 nm Wolfram beobachtet.

Während die beobachteten Eigenschaften von NiGe sehr vielversprechend sind, ist die relevanteste Kenngröße jedoch der spezifische Kontaktwiderstand $\rho_c$. Für dessen Bestimmung war die Etablierung einer $\rho_c$-Messstruktur nötig. Der Herstellungsprozess ist in Manusskript III beschrieben. Für einen NiGe-Kontakt zu B-dotierten Ge mit einer Dotierkonzentration von $2 \times 10^{17}/\mathrm{cm}^3$ wurde ein $\rho_c$ von $2.6 \times 10^{-7}\,\Omega\,\mathrm{cm}^2$ extrahiert. Eine Fortführung dieser Arbeit könnte auf genau dieser Plattform aufbauen und gezielt weitere Materialien, Prozessbedingungen und Dotierungen untersuchen.

Auch bezüglich der Leiterbahnen ist die Betrachtung alternativer Materialien von Interesse. Der mit der Reduktion des Leitungsquerschnittes einhergehende zunehmende elektrische Widerstand in Leiterbahnen stellt sowohl bei zwei- als auch dreidimensional-integrierten Schaltkreisen eine Herausforderung dar. Im Vergleich zu Kupfer, dem derzeit vorherrschenden Material zur Metallisierung von Leiterbahnen, ist die mittlere freie Weglänge von Elektronen in Cobalt verkürzt, sodass Elektronen in kleineren Strukturen weniger stark gestreut werden. Zwei Artikel dieser Doktorarbeit beschäftigen sich daher mit der Cobaltmetallisierung. In Artikel IV wird die Abscheidung von dünnen Cobaltschichten mittels zwei verschiedener Varianten der Kathodenzerstäubung untersucht, dem Gleichspannungsmagnetronsputtern (DCMS) und dem Hochenergieimpulsmagnetronsputtern (HiPIMS). Die mittels HiPIMS hergestellten Cobaltschichten zeichnen sich dabei durch eine höhere Leitfähigkeit aus. Zurückzuführen ist dies auf höhere Atomdichten, größere Korngrößen, glattere Grenzflächen und geringen Argoneinschluss. In Artikel V wurde das Auffüllen von Kontaktlöchern mit Cobalt und Kupfer mittels HiPIMS genauer untersucht. Von entscheidender Bedeutung für den erreichbaren Füllgrad ist die Zusammensetzung des Teilchenstroms beim Erreichen der zu metallisierenden Oberfläche. Ein hoher Anteil von Ionen sowie eine hohe Teilchenenergie führen zum bestem Füllverhalten.

# Acknowledgments

Zhen, thank you for all your advice and for your irrepressible optimism, especially in the those moments when I was convinced that focusing on woodwork or brewing instead would be the better choice.

Shili, thank you for your special diligence when reviewing my work even when it was late at night and deadlines were nigh!

Tomas, you were the unofficial third supervisor of this work. Thank you, not only for all the discussions and for setting up the sputtering processes, but also for always having an open ear and a watching eye (or two).

I would like to particularly thank Örjan, Amit, Leif, Rimantas, Farhad, Victoria, Per-Erik, Gabriel, Yong-Bin, and to everyone else taking responsibility for the tools at MSL and Electrum. Thank you for all your help and instruction and especially for fixing the tools over and over again. Without you, this work would not have been possible.

Thank you, Fredrik for your FIB and TEM work. Thank you, Lars for your FIB and TEM work and all the other fun moments. Dominique and Marion, thank you for welcoming me in Marseille and for the great APT analysis. Christian, for the friendly discussions and for sharing the in-situ XRD data and pole-figures. Marcos, Tuan, and Daniel for all the help and collaboration regarding the ion beam analysis. Oleksandr and Tobias for the XRD analyses. Pavel and Stéphane for the sputtering simulations.

Thanks to the other PhD students at KTH: Laura, Ahmad, Kostas, Ganesh, Panos, Mattias, Szymon. It was always a pleasure to discuss and chat with you. Not the least, you made the long train rides for doing 20 s etches seem more worthwhile! Special thanks to Ahmad and Kostas for providing me with Ge substrates and recipes for the Epsilon.

Xi, thank you for enduring to stay in an office with me, the great discussions on EBL or RL, and for sharing so many process details. Malkolm, thank you for introducing me to the group and to trallpunk, the countless discussions, and for building up my caffeine tolerance. Patrik, tack för att du välkommnade mig i gruppen, för alla de konstiga men trevliga diskussioner och för att bygga upp min tolerans mot kaffein. Asta, thank you for all the inspiration and for always lightening up the more boring days; it's a pen that you left before we could finish our book. Katharina, for all the friendly smiles and nice (German) words. Christopher, for all the philosophizing. Shabnam, for sharing some very useful words of wisdom. Shuangshuang, for all the interesting discussions on EBL, helping me fabricate my ugliest sample ever, and for pretending that I would stand a chance against you in table-tennis. Piotr, dziękuję za kalambury. Ray,

for teaching me to love *that sound*. Björn, for saving my eyesight. Xingxing, Umut, Qitao, Chenyu, Darcy, Mandy, Jie, Sven, Tove, Quentin, Ngan, Tomas, Si, Fredrik, Patrice, Nishant, Jan, Jes, Carl, Nina, Bart, Pia, Volodymyr, Long, and Michelle for being awesome colleagues! Jörgen, for trying to teach me device physics and downhill skiing; the screws in my hand will always remind me of you. Jonathan, thank you for the review and all the suggestions for improving this thesis. Wolfgang, für die vielen schönen Geschichten. Adam, for having a sense of humor and being a voice of reason. Uwe, thank you for being a never-ending source of inspiration and motivation, thank you for letting me try out my experiments on your students and for letting me lecture in your course, und danke für das viele Rätsellösen. Everyone joining the Fredagsöl for bringing a family vibe to FTE.

Besides the academic family, I am grateful for having found and kept so many friends along the way. Thank you Arry, Jo, Shayoni, Shwetha, Ana, Lara, Marcel and Franco for making my start here in Uppsala so wonderful. It was very sad to see you all go elsewhere one after the other. Danke an die KAZler für die schönen Trainingslager! Ett stort tack till alla runt East Aros Ultimate: Calle, Anna, Jelena, Alex, Fredrik, Kristina, Simon, David, Jim, Filip, Frank och Josef. Indrek, thank you for clever ideas and for the chair! Nathan and Jacinda, thank you for the great journeys together. Filippo, for the great Bud-Spencer evenings and for hosting me in Italy twice. Nicolas, for being an awesome flatmate and a great friend. Thanks to James, Jessica, and the others of the crime reading group for giving me a new perspective on writing and murder. Marie for all your support during the writing of this thesis. Thank you Juri for the friendship and for bringing a piece of home to Uppsala. Thank you Half-CPS, again and again in fifteen minutes. Danke Sabse, Berni, Marek, Thisus, Sarah, Charly, Jul und Henrik, ihr wisst wieso. Thank you Nico, Minh, Caro, Peter, Elke, Anna, Papa, Rebecca, Daniel, Julian, Marta, Adrian, Helene, Anna, Mama, Irene, Markus, Wiebke, Leif, Vanja, Kasia, Alex, Max, Tati, Anna, Florian, Maria, Achim, Konrad, Lukas, Anna, Julian, Steffi, Mama, Tina, Marie-Sophie and Erik for visiting me here in Uppsala! Nicht zuletzt, danke an meine ganze Familie für die unglaubliche Unterstützung in all den Jahren!

Thank you, who read through all these names only to find out that I forgot to mention you. I owe you a beer.

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