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Grid integration and a power quality assessment of a wave-energy park

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Arvind Parwal[1] ✉, Martin Fregelius[1], Jennifer Leijon[1], Maria Chatzigiannakou[1], Olle Svensson[1], Erland Strömstedt[1], Irina Temiz[1], Janaina Goncalves de Oliveira[1,2], Cecilia Boström[1], Mats Leijon[1,3]

[1]*Department of Engineering Sciences, Division of Electricity, Box 534, Uppsala 75121, Sweden*
[2]*Department of Electrical Energy, Universidade Federal de Juiz de Fora, Juiz de Fora, Brazil*
[3]*Department of Electrical Engineering, Chalmers University of Technology, Gothenburg 41296, Sweden*
✉ *E-mail: arvind.parwal@angstrom.uu.se*

Abstract: This study presents a step toward the grid connection of a wave-energy park through an electric power conversion system (EPCS) developed and installed for the wave-energy harvesting in Lysekil, Sweden. The EPCS comprises a rectifier, a DC bus, and an inverter followed by a harmonic filter (HF). The higher- and lower-order harmonics injected by the inverter in a power quality context are investigated. The lower-order voltage harmonics partially distort the voltage-source inverter output grid current. A phase-locked loop-based (PLL) grid-phase tracking is used to attenuate the lower-order harmonics by reflecting the grid harmonics in the inverter output. An expression for the grid-current harmonics as a function of the grid-voltage harmonics has been derived and implemented. A mathematical model is derived to obtain a transfer function for the PLL, and finally, proportional–integral gains are tuned for stable system operation. An HF for mitigating the higher-order harmonics has been implemented. The total harmonic distortion is evaluated experimentally, and the results fulfil the grid-code requirements at various frequencies and harmonic orders.

1 Introduction

The global energy demand is rising every decade and is expected to increase up to 25% by 2040 [1]. Energy sectors around the globe are pursuing renewable energy sources (RESs) to meet this growing demand [2]. The increased integration of RES into the existing power grid is gaining attention [3]. Wave power as a potential RES is attaining increased consideration as it takes advantage of the high-energy density of the ocean waves.

Furthermore, wave power is available day and night [4]. There are various ways to harvest the energy from the ocean waves through different wave-energy converters (WECs). The reviews of the most prominent technologies and projects are reported in [5–14]. Previsic *et al.* [15] described how to categorise WEC devices. They can be categorised according to three popular methods of absorbing the energy: the overtopping device, the oscillating water column, and the oscillating body. The latter can be divided into three sub-categories based on the direction of the radiation force. These are the attenuators, the terminators, and the point absorbers. The point absorber is defined as having an absorbing device width significantly smaller than the wavelength of the incoming waves. Among these topologies, heaving point absorbers are perhaps the simplest in terms of the overall design, besides having the ability to convert absorbed energy directly into electricity [16]. The power take-off unit with an all-electric conversion using a linear generator (LG) has been studied extensively at the Lysekil research site (LRS) on the Swedish West Coast in [13, 17–21]. The main components of the park are described in more detail in [13, 22]. The WEC has the advantage of having less mechanical components, which, potentially, means reduced maintenance [23]. The annual reports present the overview of the oceanic projects and the research sites in Europe [24, 25].

It is recommended to attenuate the harmonics for the RES-connected inverter to meet standards such as IEEE 519-1992; details are specified in the Appendix. The literature shows a notable research work carried out to attenuate the harmonics in the distributed power systems. In [26, 27], methods based on multiresonant controller (MRC) are used for selective harmonics elimination. The simple implementation is the advantage of these methods. However, variations in the grid-frequency affect the performance of these controllers and increase the complexity to be frequency adaptive [27]. Also, the MRC reduces the system phase margin and requires extra compensation for stable operation. The harmonics elimination based on repetitive controller uses complex design and analysis [28, 29]. Also, the performance of these controllers is highly sensitive to frequency variations, which leads to an instability operation. In [30], a method for an adaptive-filter-based harmonic elimination is used with a dead-time compensation in a rotating reference frame. The second-order harmonic limits and the causes are discussed in [31]. A single-phase phase-locked-loop-based (PLL) harmonic elimination is used in [32]. A comparison between two methods PLL and the zero-crossing detection is presented for the current harmonics in [33].

This paper focuses on the grid integration of RES by mitigating the orders of the harmonics using a PLL grid-phase-tracking method. The PLL coefficients are tuned, which in result either superimposed or cancelled the grid-current harmonics. The performance of the PLL is evaluated experimentally and compared with the theory. Furthermore, the work presented here is a step toward the grid connection of the WECs and aims to present the system for improved grid quality. For safety reasons, an autonomous grid-connection control topology is implemented in a way to connect and disconnect the WECs in various conditions. In this work, the low-order harmonics of the grid voltage and the currents, as well as the high-order harmonics of the grid currents are analysed, to improve the power quality in the grid-connected system. The results from the experimental verification meet the grid-code requirements and provide an impact in a grid-connected system for wave-energy-harvesting applications.

The remaining sections of this paper are organised as follows: in Section 2, we present the brief introduction of the LRS, the research done, and the crucial components equipped at the site are discussed. Section 3 discusses the control of the system in detail. In Section 4, a mathematical model is derived and presented with the transfer function (TF). Grid synchronisation and the analysis of grid-current harmonics are presented in Section 5. Section 6

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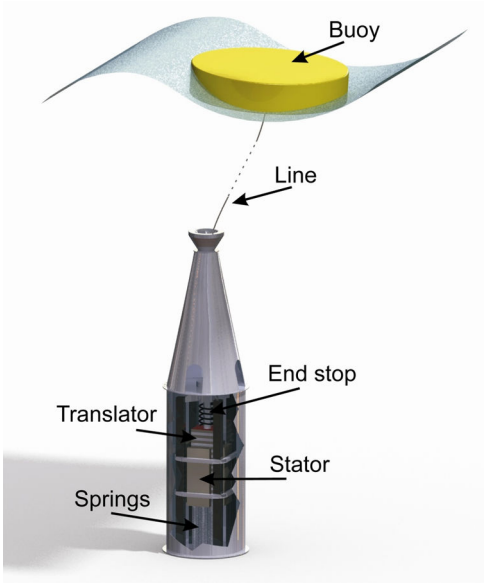

Fig. 1 *WEC developed at UU shown with essential parts; however, various WECs follow different experimental designs [39]*

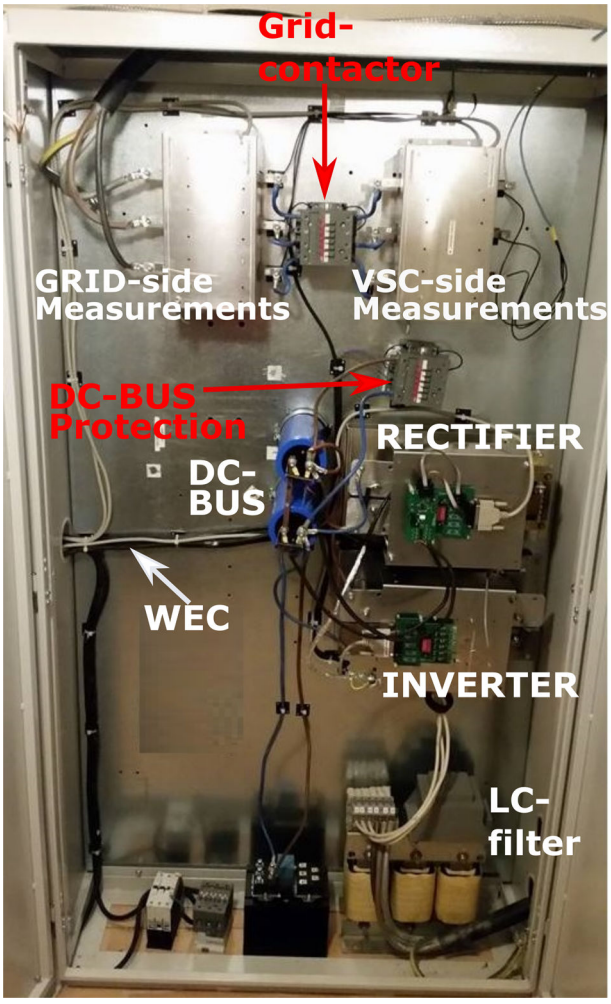

Fig. 2 *Overview of the grid-connected experimental setup*

presents the results and the discussion of the findings. Finally, this paper is concluded in Section 7.

2 Lysekil research: wave-energy harvesting

Ocean wave energy can deliver a power that could alter by a huge factor in a split minute. The wave power plants must be able to manage these extreme forces. Therefore, the survivability of the plant has raised a critical issue in wave-energy harvesting [34]. It has previously been recommended that to protect the wave power plant from the power of the ocean, the plant should be positioned below the sea surface [35, 36]. Owing to this, the generator, one of the most sensitive subsystems, is installed on the seabed. A robust and insensitive component, the buoy, is connected to the generator via a buoy line. The buoy line is guided into a vertical motion at the top of the generator structure. The piston rod is sealed off by a flexible sealing system, which prevents water from entering the generator capsule [37]. To convert the energy from the waves into electric energy, the translator is equipped with magnets, which induce a current in the stator windings of the generator as the translator moves in a vertical direction [20, 38]. To convert the power from the WECs and connect them, marine substations are used (see Fig. 1). The first marine substation, installed in 2009, was able to connect only three WECs [40]. The new marine substation is developed at Uppsala University (UU), which is capable of connecting up to seven WECs and explained in detail in [41, 42]. Three types of buoy shapes were tested: cylindrical shaped buoys, toroidal shaped buoys, and onion-shaped buoys [37].

The research on the design developments – through performance monitoring of the mechanical lead through and its sealing and guiding components – is inherently long term due to the expected lifetime of these components.

2.1 Measuring station

The measuring station (MS) is located onshore and enables testing of different subsystems and loads. The MS is equipped with a fully automated power conversion system to operate and connect to the local AC grid in a safe mode. The MS uses a DC chopper for active control of the DC link. The WEC power or power from the substation is transmitted to the MS through a subsea power cable and then to the grid-connected system. The MS is upgraded continuously since 2005, which handles the data from the WEC and the marine substation. The developed and implemented grid-connected system at the MS is shown in Fig. 2. The system is equipped with secured protections and relays.

3 Control system

During the design of a system for grid connection, there are three main aspects taken into consideration [36]. The first is the ability to keep the system in safe mode by controlling the WEC's connection and disconnection from the grid in an extreme wave climate or a generator failure. The second is the ability to control the DC-link voltage of the power converters. The last is controlling the power injected into the grid. Fig. 3 presents an overview of the control scheme. The reactive power injected into the grid is set to zero. In the setup, the grid-side converter is used to control the reactive power injected into the grid and the DC-link voltage.

The array of several WECs is defined as a WEC park. The rectified voltage of the WEC park is connected to the DC bus. Each WEC is rectified and connects to a DC bus, acting as a power smoothening energy buffer. A control system has been implemented to maintain a reliable transition. The control system is designed to execute the following tasks: (a) the LG control and (b) the grid control. In this paper, the grid-side control is discussed. The control at the grid-side system is presented, which is distributed in three different layers. The first layer includes the voltage and current sensors based hardware and the analogue-to-digital converters (ADC). The data acquisitions, the grid converter control, and the extra assignments are set to a 16 bit resolution. A voltage divider circuit is used to measure the grid voltage and an ADC with a measuring span of ±10 V. The grid current is measured using Hall sensors of ±5 V span. An agile estimating device to control loops, check faults, and transfer the data is used and defined as the second layer of the control system.

3.1 Measurement system and communication

It consists of field-programmable gate arrays (FPGAs) for the swift processing, and a real-time (RT) control for the data logging and maintaining the link to the local PC. An overview of the control

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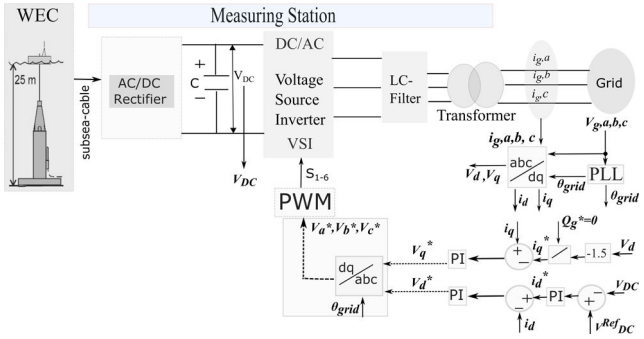

Fig. 3 *Control scheme overview for the grid-connection system*

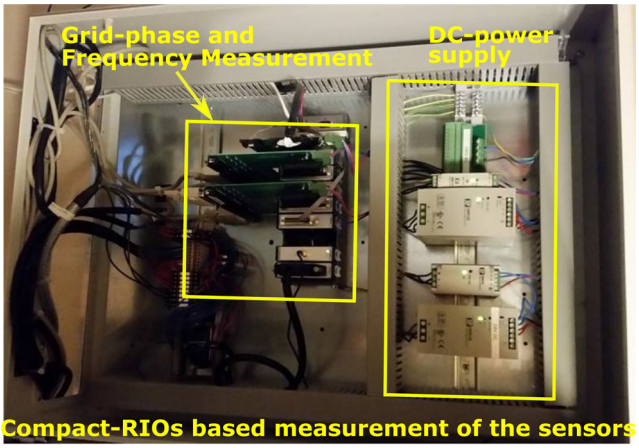

Fig. 4 *Developed PCBs for grid-phase and frequency measurement*

and data propagation is discussed in detail in [36], and the printed circuit boards (PCBs) developed for measuring the grid parameter (e.g. phase and frequency) are shown in Fig. 4. The third layer is defined as the top layer of the control system. This layer provides a graphical user interface (a standard PC) and is required to enable a direct control, the system monitoring, and data streaming. The complete measuring system design is updated regularly for a secure and robust control.

3.2 Grid-side control and the experimental setup

To connect or disconnect the system, an automated grid-connection control system is designed. The control system is able to operate in a lost-communication situation from the energy park and keeps the system in safe mode. The system is capable of connecting and disconnecting the WEC smoothly and is able to deliver instantaneous power to the grid. A grid control and synchronisation system are developed and realised to maintain a reliable power transmission, which is discussed later.

A current control (CC) is used to protect the inverter for overcurrent, whereas a voltage control lacks this dynamic behaviour. Different current-referenced frames are suggested in the literature such as the stationary-reference frame, the natural-reference frame, or the synchronous-reference frame [43]. Fig. 2 shows the experimental setup installed with autonomous protections at the MS. The grid voltages $V_{g,\,a,\,b,\,c}$ are measured and fed into the PLL block. The PLL tracks the grid-voltage vector and generates the grid-voltage angle θ_{grid} used for the transformation from the stationary abc reference frame to the synchronous dq frame. These components can, therefore, be analysed as DC values; the power feedback control is based on standard proportional–integral (PI) controllers. The grid angle θ_{grid} is used to convert the stationary-reference frame for both the voltages V_{ga}, V_{gb}, V_{gc} and the currents i_{ga}, i_{gb}, i_{gc} to the synchronous-reference frame v_d, v_q and i_d, i_q, respectively, as shown in Fig. 3. To control the power flow, two PI regulators are used to control the i_d and i_q currents, and one PI regulator is used in the outer loop to control the DC-link voltage V_{DC}. The d-axis voltage v_d is assumed and set equivalent to the magnitude of the grid-voltage vector V_g. The q-axis voltage is equal to zero $v_q = 0$. Hence, the active and reactive powers injected into the grid can be estimated in the equation below:

$$\left.\begin{aligned} P_g &= \frac{3}{2}(v_d i_d + v_q i_q) \\ Q_g &= \frac{3}{2}(v_q i_d - v_d i_q) \end{aligned}\right\} \tag{1}$$

To achieve a unity power factor in steady state, the reference reactive power component Q_g^* is set to zero, and the reference q-axis current can be obtained in the equation below:

$$i_q^* = \frac{Q_g^*}{-1.5 v_d} \tag{2}$$

The d-axis reference current i_d^* is generated by the PI regulator, which is used to maintain the DC-link voltage at a steady level to a reference DC-link voltage V_{DC}^{Ref} during the active power injection into the grid by the inverter. In Fig. 4, i_d and i_q are compared with the referenced values i_d^* and i_q^* and the resulting error is fed to the respective PI regulator to generate the reference dq voltages V_d^* and V_q^* to control the inverter. The synchronous frame reference voltages V_d^* and V_q^* are converted to the stationary frame sinusoidal voltages V_a^*, V_b^*, and V_c^*. A carrier-based sinusoidal-pulse-width modulation (SPWM) is used to generate the pulses to control the inverter with the stationary frame voltages.

3.2.1 DC bus: The DC bus, an interfacing point of the WECs to the grid-side converter, serves as a short-term buffer for the voltage-source inverter (VSI) and the rectified WEC output, which reduces the grid flickers in the grid current. Capacitors are suitable for this application due to their ability to store energy and to release the stored energy swiftly. Since the capacitor will be charged during a certain sequence, and therefore store energy, it will also get discharged during another sequence. This behaviour is called a ripple, and the ripple is depending on the value of the capacitor, i.e. a large capacitor gives more stored energy, which results in a smaller ripple. The ripple can be calculated as a 'ripple factor', which depends on the lowest-voltage amplitude, the maximum voltage amplitude, and the root-mean-square (RMS) value of the voltage. The relation between the three is called 'ripple factor', see formula (3). A less harmonic waveform of the current can be achieved by setting the lowest voltage of the DC bus. The theoretical value of the minimum voltage of the DC bus for a diode rectifier is the peak value of the line-to-line RMS voltage V_{LL}^{RMS} and is obtained in (4). The voltage at the DC bus is kept above the diode's peak DC voltage

$$\text{Ripple}_{\%\,V} = \left(\frac{V_{peak} - V_{min}}{V_{rms}}\right)100 \tag{3}$$

$$\left.\begin{aligned} \frac{1}{2}C\left(V_{DC,\,max}^2 - V_{DC,\,min}^2\right) &= \int_{t1}^{t2}\left(\left(P_{WEC}(t) - P_g(t)\right)\mathrm{d}t\right) \\ V_{DC\,min} &> \sqrt{2}\,V_{LL}^{RMS} \\ V_{DC\,min} &> \sqrt{2}\,\sqrt{3}\,V_{LN}^{RMS} \end{aligned}\right\} \tag{4}$$

where C is the capacitance of the capacitor; $P_{WEC}(t)$ is the WEC power as an input; and $P_g(t)$ is the grid power. To regularise the steady power flow, the required voltage at the DC bus is set 15–20% of $\sqrt{2}\,V_{LL}^{RMS}$.

3.2.2 Two-level (2L) VSI: The VSI, commonly called as voltage-source converter, connected with the filter and the grid is shown in Fig. 5. Three insulated gate-bipolar transistors (IGBTs) modules with 1200 V and 100 A rating are used. The IGBTs are the dual-package SKM-100GB12T4 units. The circuits of the gate driver are

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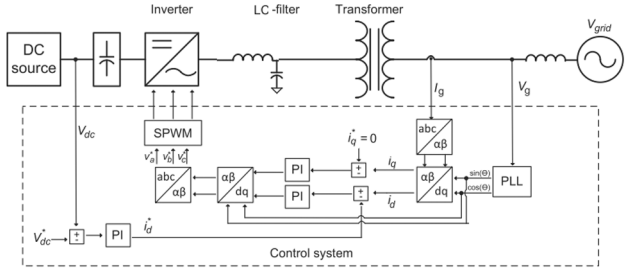

Fig. 5 *Voltage and CC scheme for the VSI*

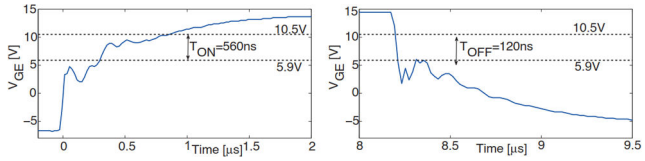

Fig. 6 *Turn-on and turn-off timings of the IGBT*

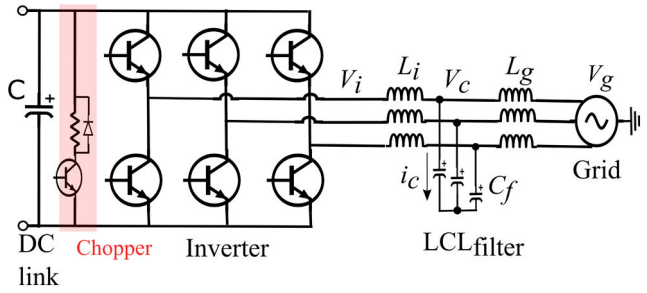

Fig. 7 *Grid-connected three-phase VSI with LCL filter*

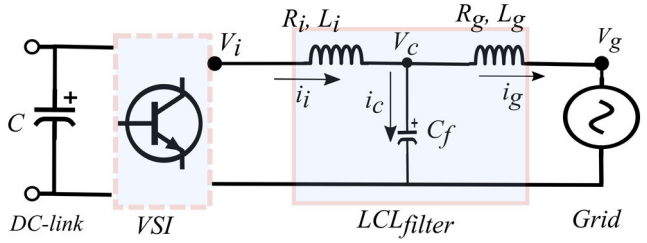

Fig. 8 *Single-phase equivalent of an LCL filter*

installed on the top of the shielded boxes for the safety reasons. The stray inductance is kept low at ∼5 nH/cm. The fast switching of the IGBTs is disciplined by modulating a signal (50 Hz) with a carrier wave (higher frequency). A balance between the switching losses and filter losses is maintained by setting the switching frequency (f_s). The fluctuations at the switching frequencies in the VSI output are removed by a harmonic filter (HF). An SPWM technique is used to control the 2L-VSI with $f_s = 5$ kHz.

Also, a chopper is implemented as safety protection and to obtain a smooth power transition. A secure interface of the control system with the logic circuits and the IGBTs is used. ACPL-337J Optocouplers are used as gate drivers. Dynamic aspects are unified for the IGBTs protection including IGBT-desat exposure, assessment during a fault, and under-voltage lockout, more details can be found in [36]. The transition of the gate signal from the FPGA to the IGBT is achieved by a NAND-Schmitt trigger (74HC132D) – as an amplifier and protection circuit – which enables the use of current limiting resistors to interface inputs to voltages over the supply voltage V_{cc}. A bidirectional digital module, NI-9401, provides a transistor–transistor-logic signal at 5 V/2 mA, which is further boosted to 15 V/20 mA. IGBTs are voltage-controlled devices, and to switch the IGBT quickly, a gate charge must be supplied. It should turn the IGBT from the off state to the on state as fast as possible, to minimise the time spent in the linear semiconductor region, and thus minimise the switching losses. A pulse is used to trigger the IGBT. The on-state gate voltage is 15 V and the off state is −8 V. By applying a negative gate voltage in the off state, one avoids false triggering (Miller effects). The gate-emitter voltage V_{GE} characteristics during turn-on and turn-off for one of the IGBTs are shown in Fig. 6. The switching time is defined as the time in the IGBT active region, here between 5.9 and 10.5 V. The turn-on time is $T_{ON} = 560$ ns and the turn-off time is $T_{OFF} = 120$ ns. The grid-side inductor–capacitor (LC) filter together with the transformer inductance forms an LCL filter. The LCL filter is an efficient and cost-effective solution to meet the grid demands.

3.2.3 LCL-filter HF: To attenuate the current ripple from the VSI, an HF is connected at the point-of-common coupling (PCC). The HF is implemented to attenuate the switching ripples [44]. In Fig. 7, the VSI is interfaced to the HF, and an isolated transformer is shown. The inductance L_T and resistance R_T of the transformer are considered in the design of the HF. The HF consists of the following components: (a) the VSI-side resistance R_i and the inductance L_i, (b) the grid-side resistance R_g and the inductance L_g and the capacitors C_f. The L_g is the combination of L_T and the grid-side inductance L_2 which yields $L_g = L_T + L_2$. To reduce the switching ripples, the LC-filter used has already been used for LC-filter configuration [45]. Fig. 8 presents the equivalent of one phase of the HF. The analysis of the stability of HF is carried out by deriving a TF of HF and compared with different conditions such as damped and undamped HF.

The implemented filter parameters are reported in Table 1, and the Bode plot results are presented in detail in [36]. The power quality in a strong AC grid is characterised by the quality of the current. The limits of the power quality are sanctioned by IEEE 519-1992. The allowed restraints are set to 20% of the maximum current. The C_f are in a star-mode configuration, and the neutral is kept floating for avoiding the zero-sequence current. The expression of HF is defined in (5) and a resonance peak occurring at the resonant frequency ω_{res} is given in the equation below:

$$H(s) = \frac{i_g(s)}{V_i(s)} = \frac{1 + C_f s}{(L_i L_g C_f)s^3 + ((L_i + L_g)C_f)s^2 + (L_i + L_g)s} \quad (5)$$

$$\omega_{res} = 2\pi f_{res} = \sqrt{\frac{L_i + L_g}{L_i L_g C_f}} \quad (6)$$

During the design of the LC filter, the inverter-side inductance L_i is selected to optimise the efficiency. A small value of L_i causes large ripple currents Δi, hence the VSI presents higher switching and conduction losses. Therefore, 10% of the attenuation rate is chosen to achieve power quality improvement. The value L_i can be obtained as presented in the equation below [46]:

$$L_i = \frac{V_{DC}}{8(\Delta i)\, f_s} \quad (7)$$

A large value for the shunt capacitor will cause an increment of the VSI rating and the reactive power flow. It is, therefore, crucial to choose an appropriate value for the shunt capacitor. During the design process, the estimated values of filter components for optimising the system for a power quality improvement and the estimated values are used in (5) and (6).

4 Grid-side CC and mathematical modelling for the TF

A CC is used due to the prevailing need for a compelling control and implicit safety measures for the VSI, as shown in Fig. 5. A voltage angle control (VAC) demands an extended control and is unreliable to deal with system resonances. The VAC lacks compelling and implicit control for the safety measures [47]. Hence, VAC is not endorsed for a grid-interfaced VSI system, whereas the CC fulfils these requirements. The complex power injected into the PCC is defined as

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$$\bar{S} = P + \mathrm{j}Q = 3\bar{V}_{\mathrm{grid}}\bar{I}^{*}_{\mathrm{grid}} \tag{8}$$

where $\bar{V}_{\mathrm{grid}}$ is the grid-phase voltage and $\bar{I}_{\mathrm{grid}}$ is the grid current. If the power is injected by the VSI through an LCL filter, the grid current $\bar{I}_{\mathrm{grid}}$ is obtained in the equation below:

$$\bar{I}_{\mathrm{grid}} = \frac{V_{\mathrm{i}}\angle\delta - V_{\mathrm{g}}\angle 0\left(1-\omega^2 L_{\mathrm{i}}C_{\mathrm{f}}\right)}{J\omega\left(L_{\mathrm{i}} + L_{\mathrm{g}} - \omega^2 L_{\mathrm{i}}L_{\mathrm{g}}C_{\mathrm{f}}\right)} \tag{9}$$

where $V_{\mathrm{i}}\angle\delta$ is the VSI output voltage and ω is the fundamental grid frequency. This presents a correlation for the variable pairs P/δ and $Q/|V_{\mathrm{i}}|$. Considering a basic case, they can be decoupled into two separate control loops. This is referred to as voltage-angle control. Despite its simplicity, VAC is not recommended for grid-connected VSIs [47]. In this work, a synchronous-reference frame is implemented and the grid-connection control system is shown in Fig. 5. The dq-axis currents i_d and i_q are used to control P and Q, respectively. The outer loop regulates the DC-link voltage to manage the power balancing, and the inner loop regulates the currents to manage the power quality. Primarily, the active and reactive powers are controlled by the grid-current-reference frame. Second, all the phases are checked, synchronised, and the grid-phase sequences are determined. Independent PI controllers are used for regulating the i_d and i_q varying parameters and an SPWM technique is used for a disciplined switching of the IGBTs of the VSI. A Park/Clarke transformation is used for the stationary frames to the dq-frame conversion for the grid voltages and the currents. The grid-phase tracking is done using PLL and discussed in detail in a later section. A numerical expression of the equivalent model is derived to determine the PI regulators gains. The derivation is presented for one phase and can be derived in the same way for the other two phases [48]

$$L\frac{\mathrm{d}i_{\mathrm{a}}}{\mathrm{d}t} = -R_{\mathrm{eq}}i_{\mathrm{a}} + V_{\mathrm{t,\,a}} - V_{\mathrm{g,\,a}} \tag{10}$$

where $L = L_{\mathrm{i}} + L_{\mathrm{T}} + L_2$ and $R_{\mathrm{eq}} = R_{\mathrm{i}} + R_{\mathrm{T}} + R_{\mathrm{g}}$.

In formula (10), i_{a} is the phase current, $V_{\mathrm{t,\,a}}(t)$ is the equivalent inverter output phase voltage, which is valid for an SPWM and used in this paper. The filter capacitor C_{f} is neglected. The amplitude modulation index is $m_{\mathrm{a}} = \sqrt{\left(V_d^*\right)^2 + \left(V_q^*\right)^2}$, where V_d^* and V_q^* are the CC feedback variables. These variables are used to control the active and reactive power flows. $V_{\mathrm{g,\,a}}$ is the voltage source in phase a that simulates the grid with a low impedance. When $m_{\mathrm{a}} < 1$ the inverter fundamental output phase voltage is $V_{\mathrm{t,\,1}}(t) = m_{\mathrm{a}}(V_{\mathrm{DC}}/2\sqrt{2})$. The rotating three-phase vectors are transformed into an $\alpha\beta$ frame with the Park/Clarke transformation by using the matrix $\boldsymbol{T}_{\alpha\beta}$ in the equation below:

$$\boldsymbol{T}_{\alpha\beta} = \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{11}$$

Substituting matrix $\boldsymbol{T}_{\alpha\beta}$ in (10) and using the current and voltage space vectors for all three phases result in the equation below:

$$\begin{aligned}[L]\frac{\mathrm{d}\left(\boldsymbol{T}^{-1}_{\alpha\beta}\boldsymbol{T}_{\alpha\beta}\right)\boldsymbol{i}(t)}{\mathrm{d}t} = &-\left[R_{eq}\right]\boldsymbol{i}(t) + \left(\boldsymbol{T}^{-1}_{\alpha\beta}\boldsymbol{T}_{\alpha\beta}\right)\boldsymbol{v}_t(t) \\ &-\left(\boldsymbol{T}^{-1}_{\alpha\beta}\boldsymbol{T}_{\alpha\beta}\right)\boldsymbol{v}_g(t)\end{aligned} \tag{12}$$

which is further simplified in the equation below:

$$\left[L_{\alpha\beta 0}\right]\frac{\mathrm{d}\boldsymbol{i}_{\alpha\beta}(t)}{\mathrm{d}t} = -\left[R_{\mathrm{eq},\,\alpha\beta 0}\right]\boldsymbol{i}_{\alpha\beta}(t) + \boldsymbol{v}_{\mathrm{t},\,\alpha\beta}(t) - \boldsymbol{v}_{\mathrm{g},\,\alpha\beta}(t) \tag{13}$$

Transforming the system parameter from the $\alpha\beta$ frame to the stationary dq frame by using matrix $\boldsymbol{T}_{\theta}$ is as below:

$$\boldsymbol{T}_{\theta} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \tag{14}$$

Then (13) can be written in (15) for the dq frame

$$\begin{aligned}&\left[L_{dq}\right]\frac{\mathrm{d}\boldsymbol{i}_{dq}(t)}{\mathrm{d}t} + \boldsymbol{T}_{\theta}\left[L_{\alpha\beta}\right]\frac{\mathrm{d}\left(\boldsymbol{T}^{-1}_{\theta}\right)\boldsymbol{i}_{dq}(t)}{\mathrm{d}t} \\ &= \left[R_{\mathrm{eq},\,dq}\right]\boldsymbol{i}_{dq}(t) + \boldsymbol{v}_{\mathrm{t},\,dq}(t) - \boldsymbol{v}_{\mathrm{g},\,dq}(t)\end{aligned} \tag{15}$$

Since $\mathrm{d}\theta/\mathrm{d}t = \omega$ angular speed can be zero. The PLL phase φ is locked to the grid phase θ if the following condition is satisfied: $\theta = \omega t + \varphi$, which is valid if the PLL has locked the grid:

$$\begin{cases} v_d(t) = V_m\cos(\omega t + \varphi - \theta) \\ v_q(t) = V_m\sin(\omega t + \varphi - \theta) \end{cases} \tag{16}$$

where V_{m} is the maximum grid voltage. The result can be seen in (17) and is then used to calculate the PI gains and to decouple between the d and q parameters. The TF for (17) is derived in (18) for the stability analysis [43]. Since the TF is obtained, the parametric values are easily obtained for the regulators. It is achieved by assessing the poles zeros position from the TF, as presented in (18)

$$\begin{cases} \frac{\mathrm{d}i_d}{\mathrm{d}t} = -\frac{R_{\mathrm{eq}}}{L}i_d + \omega i_q + \frac{1}{L}\boldsymbol{v}_{\mathrm{t},\,d} - \frac{1}{L}v_d \\ \frac{\mathrm{d}i_q}{\mathrm{d}t} = -\frac{R_{\mathrm{eq}}}{L}i_q + \omega i_d + \frac{1}{L}\boldsymbol{v}_{\mathrm{t},\,q} \end{cases} \tag{17}$$

Table 1 Generator and system parameters

Units	Specification of the parameters and values	
	Electrical parameters	Value
LG parameters	stator inductance	21.2 mH
	stator resistance	1.0 ± 1.5% Ω
	maximum current	40 A
	maximum power	20 kW
	voltage-line line (maximum)	450 V
	maximum translator speed	0.7 m/s
parameters system and HF	VSI-rated power S	10 kVA
	grid frequency f_{g}	50 Hz
	grid voltage v_{g} (line neutral)	230 V_{rms}
	switching frequency f_{sw}	5 kHz
	DC link V_{DC}	400 V
	VSI-side inductance L_{i}	0.75 mH
	VSI-side resistance R_{i}	20 mΩ
	grid-side inductance L_{g}	0.502 mH
	grid-side resistance R_{g}	80 mΩ
	HF, *cap. C*	30 μF
	rated power, S	80 kVA
	impedance, Z_{pu}	0.086 pu
PI controller	PLL gains, K_{p}, K_{i}	0.52, 126

5 Grid synchronisation

5.1 Phase-locked loop

A three-phase synchronous reference frame (SRF)-PLL is used for grid-phase tracking, as shown in Fig. 9. To minimise the errors, the strategy utilises a conversion of the stationary abc reference frame to the synchronous dq-frame components using Parke and Clarke

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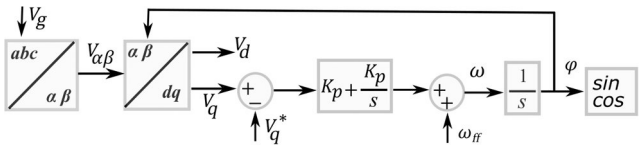

Fig. 9 *PLL structure for the grid-phase tracking*

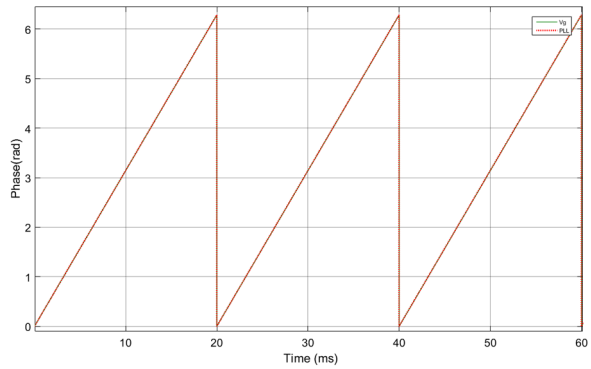

Fig. 10 *PLL performance during grid-phase tracking*

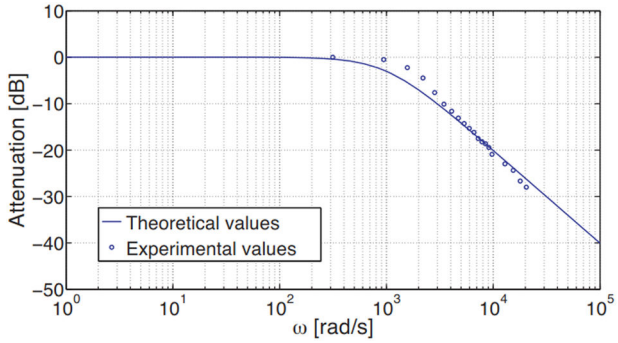

Fig. 11 *Measured and theoretical Bode plot of PLL TF*

transformation. The error is minimised by using (16) when $\theta = \omega t + \varphi$. This results in $v_q = 0$ and $v_d = \hat{V}$. By using a PI regulator on the v_q and setting $v_q^* = 0$, the error is minimised and inserting a feedforward in the loop makes the loop converge faster. Fig. 10 presents the performance of the implemented PLL. The PI-control block is tuned to minimise the PLL phase error, and also has the effect of a low-pass filter to reduce measurement noise. The TF of PI control is defined in the second-order form in (18). The PLL design is a trade-off between fast phase tracking and appropriate noise rejection. The derived closed-loop TF of the PLL in the general second-order form is given in (19) [49]

$$H_{\mathrm{PI}}(s) = K_{\mathrm{p}} + (K_{\mathrm{I}}/s) \tag{18}$$

where K_{p} and $K_{\mathrm{I}} = 1/\tau$, are the proportional and integrator controller parametric-gain values and τ is the integral time constant which is set to 0.2712

$$H_{\mathrm{PLL}}(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{19}$$

where $\omega_n = \sqrt{K/\tau}$ is the closed-loop bandwidth of the PLL and $\zeta = \sqrt{\tau K/2}$ is the damping ratio, where K is the normalised factor to scale the phase error into integer on the FPGA, which is defined as $K = K_{\mathrm{p}}K_{\mathrm{m}}$ and set value of K_{m} is 3000. The theoretical Bode plot of the PLL is presented in Fig. 11 along with the measured attenuation for the different frequencies. The tuned PLL coefficients are presented in the Appendix. The sampling frequency is usually set to the f_{sw} or $f_{\mathrm{sw}}/2$ built on the controlling strategy utilised [49]. Auxiliary voltage supply of 24 V is used for the control system, sensors, and contactors. The control is done by using a compact-real-time input outputs (RIOs) design for a robust PLL to track the grid phase and to establish a stable grid synchronisation. The PLL was chosen because of its simple implementation compared with other available options. The output voltage of the VSI and HF is synchronised to the grid voltage after fulfilling the grid-code requirements [50]. At the grid side, a grid synchronisation control system is implemented. The voltage transducers are used to measure the voltage and the frequency of the grid and logged the data in the data logger. The analogue-to-digital converters (ADCs) is used to sample the data and the FPGAs process the data, whereas the RT control logs the data in local memory and communicates between FPGAs and the PC. To measure the voltage in three phases, individual PCBs are certified after testing and calibration, and the developed PCBs are shown earlier in Fig. 4.

5.2 Grid-current harmonics

To meet the grid codes and improve the grid power quality, it is recommended to maintain the harmonics in the grid currents lower than 5%. The IEEE 519-1992 [50] defines the maximum allowable harmonics for the medium- and high-voltage grids. The IEEE 519-1992 current distortion standards are presented in the Appendix. The standard states the limits for total harmonic distortion (THD) and the peak limits of the individual currents and is calculated in the equation below:

$$\mathrm{THD} = \frac{\sqrt{\sum_{h=2}^{N}(I_h)^2}}{I_1} \tag{20}$$

where h is the order of the harmonic and I_1 is the component of the grid current at the fundamental. The respective Fourier components of the grid voltage $\bar{V}_{\mathrm{g}}$ and the inverter voltage $\bar{V}_{\mathrm{i}}$ are computed in the equation below:

$$\left.\begin{aligned} V_{\mathrm{g}}(t) &= \sum_{h=1}^{n} V_{\mathrm{g}h}\sin(h\omega t + \varphi_{\mathrm{g}h}) \\ V_{\mathrm{i}}(t) &= \sum_{h=1}^{n} V_{\mathrm{i}h}\sin(h\omega t + \varphi_{\mathrm{i}h}) \end{aligned}\right\} \tag{21}$$

The complex power $S_{1\varphi}$ (VA) into the grid at the fundamental frequency is defined in the equation below:

$$S_{1\varphi} = \frac{V_{\mathrm{g}}V_{\mathrm{i}}\sin(\delta) + \mathrm{j}\left(V_{\mathrm{g}}V_{\mathrm{i}}\cos(\delta - V_{\mathrm{g}}^2)\right)}{\omega_1 X} \tag{22}$$

where X is the inductive reactance between V_{g} and V_{i}, $\delta = \varphi_{\mathrm{i}1} - \varphi_{\mathrm{g}1}$ is the load angle, the reactive power flow is controlled to zero by setting the amplitude of the inverter voltage to $|V_{\mathrm{i}}| = |V_{\mathrm{g}}|/\cos(\delta)$. The hth grid-current harmonic $\bar{i}_{gh}$ is obtained in the equation below:

$$\bar{i}_{gh} = \frac{V_{\mathrm{i}h}\angle\varphi_{\mathrm{i}h} - V_{gh}\angle\varphi_{gh}\left(1 - \omega_h^2 L_{\mathrm{i}}C_{\mathrm{f}}\right)}{J\omega_h\left(L_{\mathrm{i}} + L_{\mathrm{g}} - \omega_h^2 L_{\mathrm{i}}L_{\mathrm{g}}C_{\mathrm{f}}\right)} \tag{23}$$

where $V_{\mathrm{i}h}\angle\varphi_{\mathrm{i}h}$ is the inverter voltage harmonic and $V_{gh}\angle\varphi_{gh}$ is the grid-voltage harmonic. Complete harmonic cancellation occurs, when $V_{\mathrm{i}h}\angle\varphi_{\mathrm{i}h} = V_{gh}\angle\varphi_{\mathrm{g}h}\left(1 - \omega_h^2 L_{\mathrm{i}}C_{\mathrm{f}}\right)$.

6 Result analysis and discussion

This section contains the experimental results validating the procedure to reduce the harmonics contents at switching frequencies and lower-order harmonics of the grid current. Additionally, lower-order harmonics of the grid voltage are experimentally studied and presented with the results at low-power injection into the grid. The inverter is connected to the primary side of the YY 345/1 kV, 80 kVA three-phase transformer via the filter. To prevent the flow of zero-sequence currents, the neutrals of the transformer are left floating, and the transformer is considered

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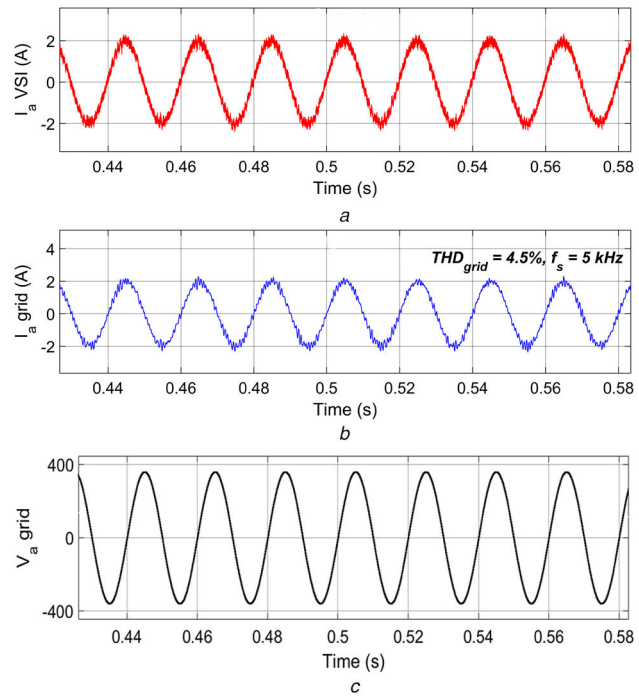

Fig. 12 *Measured current of VSI and the grid showing their THDs*
(a) VSI-current waveform in phase a with THD = 18%, ***(b)*** Grid-current waveform in phase a with THD = 4.5%, ***(c)*** Grid voltage in phase a

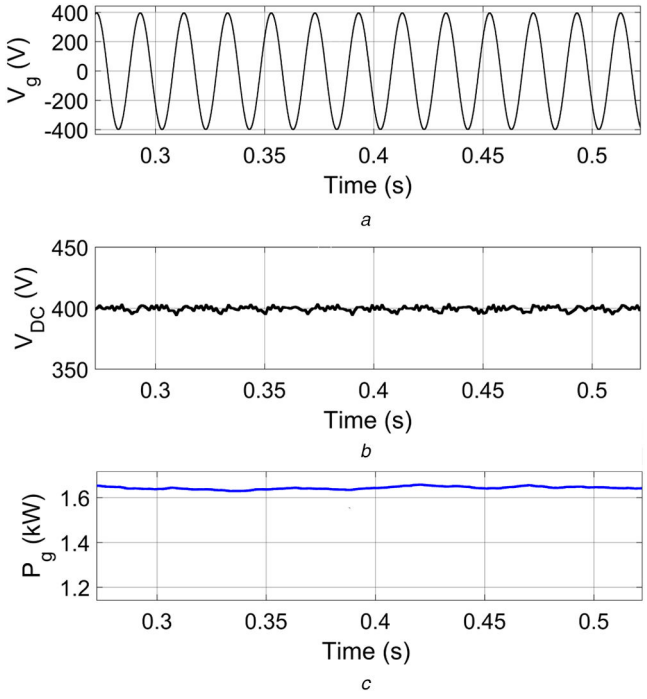

Fig. 13 *Measured parameters*
(a) Grid voltage, ***(b)*** DC-link voltage, ***(c)*** Active power into the grid

balanced. The transformer only operates at 40% of its rating, which is far from any magnetic saturation of the core. The local grid with a fundamental frequency of 50 Hz and a voltage of 400 V was used at the PCC. Three-phase voltages and currents are measured at the PCC, and the voltage and current harmonics contents are obtained. We used the fast-Fourier transform (FFT) with a Blackman window to calculate the harmonic contents with a measurement rate of 200 kHz.

6.1 Analysis of the switching-frequency harmonics in the grid currents

The high-frequency harmonics of the VSI currents are reduced notably using an HF to meet the grid-code requirements, which also meets the demanded attenuation rate of 10% for a power quality improvement as shown in Fig. 12. The control has a fixed switching frequency of 5 kHz and a referenced DC voltage V^*_{DC} of 400 V. The reactive power flow in the PCC is kept zero throughout the experiments. It is worth mentioning that the experimental results were obtained without a damping resistor in LCL filter. Moreover, the actual grid inductance L_g, which includes the transformer inductance, is used in the experiments as depicted in Fig. 8. Figs. 12*a* and *b* show the waveforms and respective THDs of the VSI current i_1 and the grid current i_{ga} for $L_g = 0.502$ mH, respectively. Fig. 12*c* shows that the grid voltage V_{ga}, where it can be noted that the grid current i_{ga} and the grid voltage are in phase as presented for phase a. Almost a unity power factor is maintained throughout the tests to control the reactive power flow close to zero into the grid.

The obtained THD of VSI current is 18%, whereas the THD of the grid current is below 4.5%. As shown in Fig. 12, the THD values are effectively reduced by using the LCL filter at the switching frequency. The obtained THD results comply the THD limits as per recommendation for the THD. Moreover, the total demand distortion (TDD) in the obtained grid current is below 15% which satisfies the requirements for low-voltage grids. If the TDD limits are followed, the standards become more generous. In this work, the operating grid is a low-voltage grid (in our case, <69 kV), and the TDD limits are specified in the Appendix.

6.2 Analysis of the grid-voltage harmonics

Three-phase voltages are measured at the PCC, and the grid voltage V_{ga}. The DC-link voltage and the active power injected into the grid are shown in Fig. 13. The frequency spectra of the grid voltage in phase a present the grid-voltage harmonics with the fundamental voltage as a reference, as shown in Fig. 14. Since the grid-voltage harmonics vary in phase and the resulting grid-current harmonics may vary as well. The THD of the grid voltage is measured to 0.69% and satisfies the standards well within limits. Fig. 13*a* shows the full-scale grid-voltage waveform in phase a, measured at the PCC. Fig. 13*b* shows that the DC-link voltage is kept steady at the reference level $V^*_{DC} = 400$ V with a small amount of DC ripples. The injected active power into the grid is shown in Fig. 13*c*. A constant active power of 1.65 kW is injected into the grid, and the system is well-capable of keeping a null reactive power injection into the grid.

The harmonic contents for the grid voltage in phase a are presented in Fig. 14. It shows that the presence of even-order harmonics may be due to local unbalanced loading in the nearby grid. These harmonics are well-attenuated along with the odd-order harmonics, and a desired level of the THD is achieved. Using the PLL coefficients, the experimental and theoretical results of the TF of the PLL for a grid voltage are presented in Fig. 11. The results show that both curves have a first-order roll-off of −20 dB/decade with a minor descent at the cut-off frequency. The results also show that the stability agreement is met at different frequencies. The THD of the grid voltage is well-below the maximum THD limits (5%). Fig. 15 presents the magnitude of the harmonic spectra of the grid voltage.

Fig. 15 presents the individual spectra components at different frequencies. It is evident that the third-order harmonic $V_{g3}/V_1 = 0.051$ is far below the fundamental component at 50 Hz. Moreover, the fifth (V_{g5}/V_1) and the seventh (V_{g7}/V_1) order harmonics are significantly attenuated and meet the grid-code requirements for the individual voltage harmonics as defined by the IEEE 519-1992. However, the fifth harmonic in Fig. 14 showed a slight discrepancy in its magnitude. The source of this error could be the slight discrepancy during the FFT with a Blackman window. Moreover, the individual component of the fifth harmonic fairly met the limit (5%) assigned by the IEEE 519-1992 standard. A

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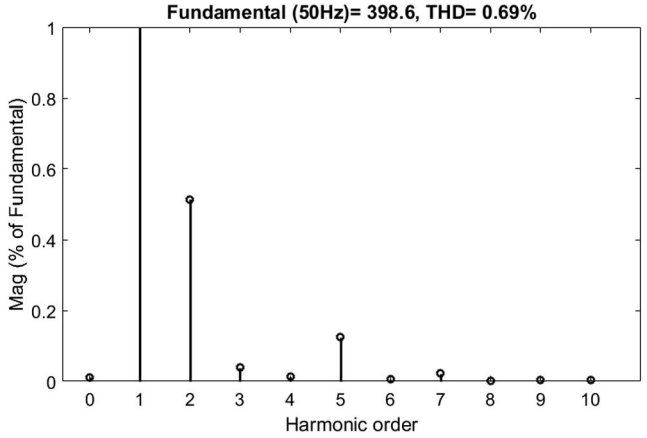

Fig. 14 *Magnitude of the grid-voltage harmonics*

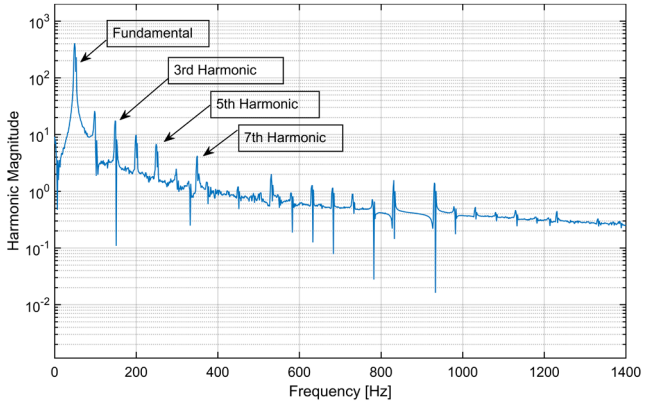

Fig. 15 *Magnitude of harmonic spectra of the grid voltage*

Table 2 Current distortion limits regulated by standard IEEE 519-1992

Current distortion limits for general distribution system [50] (120 V through 69 kV)						
	Individual harmonic order (odd harmonics)					
I_{SC}/I_L	<11	11≤*h* < 17	17≤*h* < 23	23≤*h* < 35	35≤*h*	TDD
<20[a]	4.0	2.0	1.5	0.6	0.3	5.0
20–50	7.0	3.5	2.5	1.0	0.5	8.0
50–100	10.0	4.5	4.0	1.5	0.7	12.0
100–1000	**12.0**	**5.5**	**5.0**	**2.0**	**1.0**	**15.0**
>1000	15.0	7.0	6.0	2.5	1.4	20.0

The bold values indicates the range for the ratio ISC/IL where this level is 180 for the Lysekil research site (LRS).

IEEE 519-1992 current distortion limit at the PCC of LRS, $I_{SC}/I_L = 180$. Maximum harmonic current distortion in per cent of I_L.

[a]Even harmonics are limited to 25% of the odd harmonics limits above.

possible solution for mitigating this error could be the implementation of the method combining least square and optimisation technique, which could provide more accurate results; however, in our application, the obtained individual harmonics and THD are well-satisfying the grid-code requirements.

6.3 Analysis of the lower-order harmonics in the grid currents

The grid-current harmonics are computed by using (23). The grid-current waveform is shown in Fig. 12*b* and analysed for the lower-order harmonics. The results presented in Figs. 16 and 17 show that the third-order harmonic i_{g3}/i_1 is well-below the fundamental and the limits sanctioned by IEEE standard for individual harmonic components. This harmonic falls under the category of zero-sequence current and is effectively eliminated by keeping the neutral of the transformer floating.

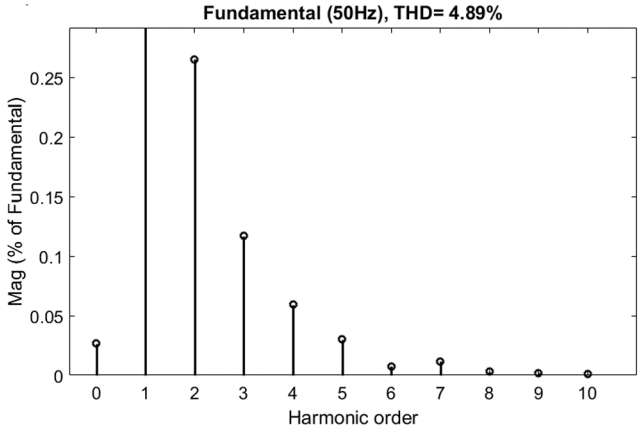

Fig. 16 *Magnitude of the low-order harmonics of the grid current*

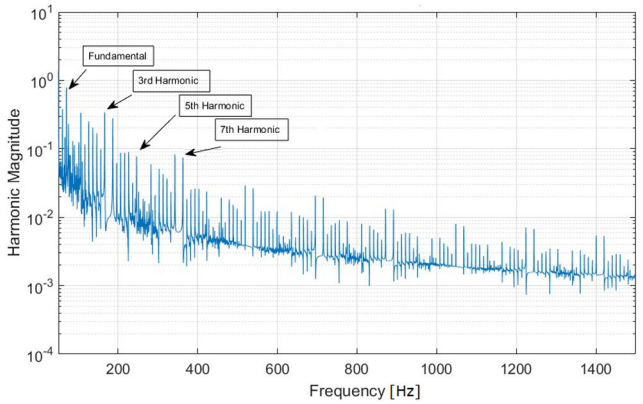

Fig. 17 *Magnitude of harmonic spectra of the grid current caused by the voltage harmonics*

If this prevention is not taken into consideration, the vector component of the third harmonic may vary three times to its vector value in each phase and will only heat the system. The harmonic magnitude of the zero-sequence components is almost eliminated from the current harmonics, as shown in Fig. 17. Also, the fifth harmonic i_{g5}/i_1 and the seventh harmonic i_{g7}/i_1 components are well-attenuated even at low-power flow into the grid. The individual distortion in odd harmonics is significantly reduced and well-below the limits allowed. From the results, it can be noted that the individual distortion of the even harmonics is <25% of the odd harmonics from Table 2 in Appendix 1. However, the second-order harmonic is visible, but this harmonic has a significantly reduced harmonic distortion almost 0.26% of the fundamental, which is well-acceptable as per the IEEE standard. If the power flow is increased, the relative effect of the harmonics reduces as the fundamental frequency component increases. It is interesting to note that the grid-code requirement – for a grid below 69 kV, the THD recommendation is $\text{THD}_{\max} < 5\%$ for both voltage and current – is met reasonably well and can be improved extensively with higher-power flows. If the TDD is used, the grid-code standards are met more generously.

6.4 Performance of the controller in a variable power flow

The behaviour of the controller is presented in Fig. 18 during a variable power flow case. To demonstrate the stability and the performance of the controller, the control of *dq*-axis currents is shown in Fig. 18*a*, where the current controller kept the *q*-axis current to zero to maintain a zero reactive power (Q_g) flow and the *d*-axis current is followed by the generated referenced *d*-axis current to inject the active power (P_g) into the grid, as shown in Fig. 18*b*. The DC-link fluctuation occurred due to the WEC varying power as shown in Fig. 18*c*, where the referenced DC-link voltage V_{DC}^* is maintained around 400 V. The result presented the stable behaviour of the DC-voltage controller during the test. The

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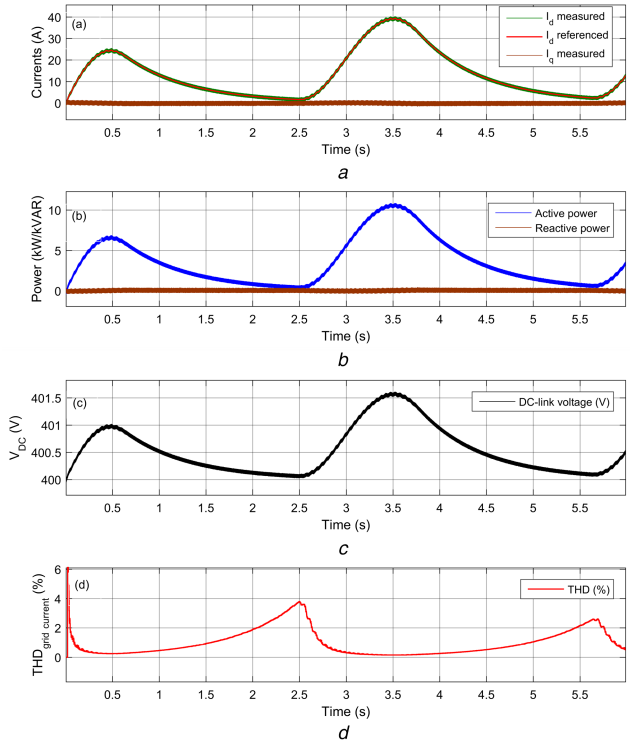

Fig. 18 *Measured parameters in variable power flow showing the performance of the controller*

(a) *d* and *q* Axis measured and referenced currents, ***(b)*** Active power injected into the grid and the reactive power controlled to zero, ***(c)*** DC-link voltage varying according to the rectified power fed by the WEC, ***(d)*** THD of the grid current

THD obtained, as shown in Fig. 18*d*, throughout the test, is well-below the maximum limit allowed by the IEEE 519-1992 standard. It can be noted that the grid-current THD reported in Fig. 18*d* from a varying power flow was increasing when the power flow was reduced to a minimum, at time instant $t = 2.5$ s and around 5.6 s, whereas the value of the percentage value of THD was significantly reduced in a high-power flow, kindly note at $t = 0.5$ s (THD $\simeq 4\%$) and at $t = 3.5$ s (THD $\simeq 3\%$) in Fig. 18*d*. The observed THD analysis depicted that the THD limit is satisfied for $\text{THD}_{\max} < 5\%$ in improved power quality context.

7 Conclusion

In this paper, we presented an experimental validation for the power quality improvement by analysing the harmonics content of the grid voltage and current. A grid connection has been established for connecting an array of several full-scale WECs. A fully automatised control system has been developed and validated experimentally. The results presented analyse the work, which validate that the higher-order and the lower-order grid-current harmonics are reduced and satisfied the grid-code requirements. The lower-order harmonics are analysed in steady and varying power flow, and the results presented met the criteria of the IEEE standard. The higher-order harmonics, caused by the switching in the grid current are attenuated by the LCL filter and kept below the allowed limits. The inductance of the grid is considered throughout the experiments to present control stability. The voltage and the current harmonics are analysed and presented with results which meet the required THD limits in a low-power flow application. The voltage and the grid-current harmonics have been controlled according to the grid codes set by the IEEE 519-1992 standard. A PLL-based grid-phase tracking is implemented to reduce the 5th and 7th harmonics components. A significant reduction in the odd and even harmonics is achieved at low-power injection into the grid at unity power factor. The THD of the current in a varying power flow is assessed and controlled by the control under the allowed limit. The objective of assessing and improving the power quality in a smart grid context is achieved by meeting the allowed THD limits regulated by the standards such as IEEE 519-1992 and IEEE 1547-2003 for the grid voltage and current. The results presented show a good agreement for improved power quality in the grid. From the results, the system performance indicated a safe operation and an improvement in the power quality for an energy-harvesting application from the ocean waves.

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10 Appendix

10.1 Appendix 1

The recommended limits are also dependent on the grid-voltage level, and its stiffness, defined as I_{SC}/I_L , where I_{SC} is the short-circuit current and I_L is the rated load demand current. The grid-connected system at the MS is rated according to the current rating of 81 A. The grid-connected onshore transformer has a short-circuit current capacity of $I_{SC} = 2450$ A on the primary side and 1318 A on the secondary side. This condition yields the I_{SC}/I_L ratios of 30.2 and 180, respectively. For a grid below 69 kV, the THD limit for both currents and voltages is set to a maximum 5%. The TDD limits set for the Uppsala University research site is 15% from Table 2. The standard is specified in detail in [50].

The value of short-circuit current (I_{SC}) and the value of maximum load current (I_L) is calculated using

$$I_{SC} = \mathrm{kVA_{tf}}/\left(\sqrt{3}\,\mathrm{kV_{\varnothing-\varnothing}} Z_{pu}\right)$$

$$I_L = \mathrm{kW_{max_demand}}/\left(\mathrm{PF}\,\sqrt{3}\,\mathrm{kV_{\varnothing-\varnothing}}\right)$$

where $\mathrm{kVA_{tf}}$ is the rated transformer power kVA; Z_{pu} is the per-unit impedance of the transformer (0.086 pu) at rated kVA; and $\mathrm{kV_{\varnothing-\varnothing}}$ is the nominal voltage, i.e. 0.4 kV.

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