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High Power Radio Frequency Solid-State Amplifiers and Combiners for Particle Accelerators

From module to system design approach

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Abstract

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The rise of Big Science projects brings issues related to the energy consumption and the associated environmental impacts of such large-scale facilities. Therefore, environmentally-sustainable developments are undertaken towards the adoption of energy savings and improved energy-efficient approaches. The advent of the superconducting (SC) radio frequency (RF) accelerating cavity is bringing answers to these issues. Such superconducting RF (SRF) cavity is made of niobium that allows much higher accelerating gradients with a minimization of the energy consumption. The SC RF technology is increasingly used in many modern particle accelerators, including: the European Spallation Source (ESS), the X-ray Free Electron Laser (XFEL), the Linac Coherent Light Source (LCLS)-II and the proposed International Linear Collider (ILC).

The innovation of solid state PA technology pushes limits regarding packaging, efficiency, frequency capability, thermal stability, making them more attractive than other well-established alternative technologies, such as vacuum tube technology in mid-range power applications. Through the investigations of designs and techniques, this research goal of the thesis allows to improve solid-state based power generation systems from module to the overall system design. This thesis introduces the single-ended PA design approach in planar technology and at kilowatt level. The design solution unlocks different possibilities including: improved integration, layout flexibility for tuning, and suitably for mass productions that are demanded in future high peak power generation systems. The novel amplifier design is followed by time domain characterization to fully evaluate the pulse profiles of such amplifiers when delivering kilowatt output power level for operation in conjunction with SRF accelerating cavities. Amplitude and phase stability of those amplifiers are also investigated in time-domain. The extracted data can then be used as measurement-based model for predicting factors which could degrade the overall stability of the associated PA.

Future RF power generation systems built around solid state PAs need also efficient combining strategies. Two engineering design solutions are investigated in this thesis aiming for mid- and high- range power combination. One solution is based on a combination of the Gysel structure using suspended strip-line technology for improved power handling capability. Another solution is implementing a radial combiner, which uses re-entrant cavity resonator at 352 MHz and door-nob geometry for coupling at inputs and at the output. These solutions facilitate the scaling up 400 kW for powering ESS spoke cavities while maintaining a high degree of efficiency in RF power generation. This thesis gives insights of system integration and tuning procedures with a demonstration of combining 8 modules, delivering a total of 10 kW output power. Along with the proposed combining solutions at higher power levels, the nominal power block of 10 kW is used as an elementary block to propose scaling up in power till the 400 kW nominal power required by ESS.

Finally, this thesis focuses on implementing an optimal charging scheme for SRF cavities, which helps reducing the wasted energy and improves the overall efficiency operation at future accelerating facilities. Therefore, these results contribute further to the larger adoption of solid state technologies in the future power generation systems for particle accelerators.

Keywords: solid state technology, power amplifier, superconducting cavities, optimal charging, high efficiency, particle accelerators

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Dành cho bố mẹ, và vợ Dương Ngọc Hương
Dedicated to my parents, and my wife Duong Ngoc Huong

"Move fast, and break things" Mark Zuckerberg

List of papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I   Linus Haapala, Aleksander Eriksson, Long Hoang Duc and Dragos Dancila, **"Kilowatt-level power amplifier in a single-ended architecture at 352 MHz,"** in *Electronics Letters*, vol. 52, no. 18, pp. 1552-1554, 2016.

II   Long Hoang Duc, Anirban Bhattacharyya, Vitaliy Goryasko, Roger Ruber, Anders Rydberg, Jorgen Olsson, and Dragos Dancila, **"Time domain characterization of high power solid state amplifiers for the next generation linear accelerators,"** in *Microwave and Optical Technology Letters*, vol. 60, no. 1, pp. 163–171, 2018.

III   Long Hoang Duc, Anh Nguyen Dinh The, Duong Bach Gia, Magnus Jobs, Roger Ruber and Dragos Dancila, **"High-power low-loss air-dielectric stripline Gysel divider/combiner for particle accelerator applications at 352 MHz,"** in *The Journal of Engineering*, vol. 2018, no. 5, pp. 264-267, 2018.

IV   Vitaliy Goryashko, Magnus Jobs, Long Hoang Duc, Johan Ericsson and Roger Ruber, **"12-Way 100 kW Reentrant Cavity-Based Power Combiner With Doorknob Couplers,"** in *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 2, pp. 111-113, Feb. 2018.

V   Long Hoang Duc, Magnus Jobs, Tor Lofnes, R. Ruber, Jorgen Olsson, and Dragos Dancila, **"Feedback compensated 10 kW solid-state pulsed power amplifier at 352 MHz for particle accelerators,"** in *Review of Scientific Instruments* , vol. 90, no. 10, p. 104707, 2019.

VI   Long Hoang Duc, Tran Van Nghia, Arniban Bhattacharya, Tor Lofnes, Roger Ruber, Jorgen Olsson, and Dragos Dancila, **"A Highly Efficient Solid State RF Power Source for Optimal Power Consumption during the Charging of Superconducting Cavities,"** Manuscript.

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Other publications

The following papers were not included in this thesis.

VII   Long Hoang Duc, Mans Holmberg, Adam Hjort, Roger Ruber, Anders Rydberg, and Dragos Dancila, **"Monitoring of RF high power SSA with Arduino,"** in Swedish Microwave Days, March 15-16, Linköping, Sweden, 2016.

VIII   Long Hoang Duc, Anders Rydberg, Jorgen Olsson, Vitaliy Goryashko, Roger Ruber, and Dragos Dancila, **"Time domain characterization of high power RF pulsed solid state amplifiers for linear accelerators,"** in Ninth CW and High Average Power RF Workshop, June 20-24, Grenoble, France, 2016.

IX   Dragos Dancila, Long Hoang Duc, Magnus Jobs, Mans Holmberg, Adam Hjort, Anders Rydberg, and Roger Ruber, **"A compact 10 kW solid-state RF power amplifier at 352 MHz,"** in Journal of Physics: Conference Series, vol. 874, p. 012093, July 2017.

X   Stefan Book, Long Hoang Duc, Dragos Dancila, **"Design, fabrication and measurement of 1 kW class-E amplifier at 100 MHz,"** in Swedish Microwave Days, May 24-25, Lund, Sweden, 2018.

XI   Long Hoang Duc, Anirban Bhattacharyya, Jorgen Olsson and Dragos Dancila, **"Optimal Power Consumption during the Charging of Superconducting Cavities using Drain Voltage Modulation of Solid State Power Amplifiers,"** in Swedish Microwave Days, May 24-25, Lund, Sweden, 2018.

XII   Long Hoang Duc, Anirban Bhattacharyya, Jorgen Olsson and Dragos Dancila, **"Implementation of a Highly Efficient Solid State RF Power Source for Superconducting Cavities,"** in Swedish Microwave Days, May 24-25, Lund, Sweden, 2018.

Contents

1. Introduction

"As the saying goes, the Stone Age did not end because we ran out of stones; we transitioned to better solutions. The same opportunity lies before us with energy efficiency and clean energy." – Steven Chu - Nobel laureate 1997.

The emergence of Big Science

The term "Big Science" was first introduced by Alvin Weinberg from Oak Ridge National Laboratory in 1961 to characterize Mega-projects with large-scale instruments and facilities i.e. huge rockets, high-energy accelerators, high-flux research reactors, in which research is carried out by large teams of scientists and technicians working in collaboration [1]. Originally, "Big Science" prospects began from the collaboration between the US government, US army, and academia in the Manhattan project during the Second World War [2]. For such large-scale projects labeled Big Science projects, a common character emerges, a model of 5 M's: money, manpower, machines, media and military [3]. During the era of Big Science, several of the best-known projects were developed also for high-energy physics, allowing i.e. the exploration of the matter at nuclear and sub-nuclear length scales i.e. Stanford Linear Accelerator Center (SLAC) and FermiLab in US, KEK in Japan, and the high-energy large Hardron Collider (LHC) CERN [4].

The trend of Big Science

Research in large-scale projects has been shifted away from high-energy physics to material science at materials-science facilities (i.e. synchrotron light sources and neutron-scattering facilities) allowing for probing matter at atomic, molecular, and also at larger scales. Such facilities are considered emblematic of the new Big Science era. The "new" means that the character of new facilities are expanding in new scales of physical footprints and costs, in the scope and complexity of multidisciplinary networks, in providing opportunities for new users coming from industry and multi-disciplinary research such as: archaeology, geology, and medicine, in providing state-of-the-art materials knowledge to address the grand challenges related to climate change, energy security, health and well-being, food preservation, etc [5, 6].

Two major examples of such new experimental facilities in Sweden include: the MAX IV and the European Spallation Source (ESS) Big Science projects. The MAX IV is a synchrotron radiation facility where X-rays are used to investigate properties of materials. The construction was completed in 2015 with a linear accelerator (linac), two storage rings in which one has an energy of

1.5 GeV and the other one, 3 GeV, and there are 30 beamlines for user experiments [7]. The neutron scattering method is an essential tool to explore materials properties and relies on the scattering behaviour when neutrons pass through materials. Thus, the method allows researchers to get insightful understanding of the structure, composition, or dynamics of samples at atomic scale. ESS is a neutron source [8], which is under construction in Lund Sweden. ESS consists of a 500-m long linear proton accelerator with an average beam of 5 MW, the world's most powerful neutron source. It is expected that the first experiments at the ESS will begin in 2023, with a full capacity of 40 instruments for users.

The trend of big machines at new Big Science facilities
"Following Paris agreement, it will be imperative to have a climate-neutral Europe by 2050. It is therefore vital that new big-science initiatives lead the way in greening their technologies and facilities." – from the open symposium of the European Strategy for Particle Physics (ESPP) in May 2019.

The rise of new Big Science projects brings issues related to energy consumption and the associated environmental impacts at large-scale facilities. Since such facilities require extremely high demands of energy quality and consumption levels during their operation i.e. the target goal for ESS's power consumption is under 270 GWh per year. Therefore, the adoption of energy savings and efficiency improvement approaches is imperative allowing for environmentally-sustainable development at large-scale research facilities i.e. ESS wants to be the world's first green facility. These approaches are used towards achieving the renewable goal, the recyclable goal, and the responsible goal of the United Nations (UN) sustainable development goals (SDGs) [10] in order to build a sustainable ESS facility. For ESS, the renewable goal is implemented using renewable resources that allows for providing the facility's annual power consumption at a stable, competitive and predictable cost. This goal results in the savings of 135000 tones of CO_2 emissions. For the recyclable goal, the facility features no cooling towers as compared to traditional

Subsystems of facility	Annual electricity use [GWh]	Annual cooling need [GWh]
Accelerator	167	138
Target	31	57
Conventional facilities	4	-6
Neutron scattering system	32	32
Heat Pumps	44	44
Total	278	265

**Table 1.1.** *Energy inventory at ESS facility [9].*

designs. Instead, the generated waste heat is recycled and transported to the nearby district heating networks. Unique features of the cooling system can help reducing 15000 tones in CO_2 emissions annually. Energy efficiency is a valuable figure-of-merit for a sustainable research facility design to meet the responsible goal i.e. 270 GWh per year in energy consumption at ESS facility. For the responsible goal, energy-savings enhancement can result in a reduction of 40000 tones of CO_2 as compared to the original design, with 350 GWh of the energy consumption, without preventing the availability and intensity of the ESS neutron facility. To fulfill the responsible goal, there is a need for enabling energy-savings innovations, including: regular energy inventories, energy culture and energy management and systems [9]. The energy inventory (EnI) method is a measure of the progress towards the responsible goal, providing support to identify the areas with high energy consumption and design rooms for improvement of the energy performance which is then focused on the top energy consumers of the facility. An energy culture is combined with EnI method as supporting tools for a systematic energy management. Energy management system adopts energy management plan which is based on an energy inventory of energy flows, see Table 1.1. Energy flow mapping is implemented by the energy management system enabling more insights in the energy flow towards executing proper actions for improvement of energy performance. Energy efficiency approaches is part of the energy management system aiming for major consumers of the facility i.e. linac's energy consumption accounts for 70% of energy supplied to ESS facility [9]. Any increase in efficiency has therefore a significant contributor in reducing the overall CO_2 emissions. For the future circular collider [11], an enhancement of 10% i.e. from 70% to 80% in the efficiency of Klystron-based power generation systems would represent a reduction in the energy consumption up to 1 TGWh during a time span of 10 years. Energy efficiency approaches will be driven by addressing the methods and innovative technologies for RF systems of the linac, the cryogenic system, and the RF test stands. These are related to the use of superconducting cavities i.e. in the spoke sections (352.21 MHz) and elliptical sections (704.42 MHz) of ESS linac [8], the use of stacked multi-level topology in Klystron modulators [12], the use of permanent magnets, the use of Klystron, Gridded tubes, and Solid State Amplifiers at RF power generation systems, the use of optimal filling scheme [13] as implemented in Chapter 4, the optimized design and energy management of cryogenic and conventional systems [14].

## 1.1 An overview of Microwave Power Generation Systems

Microwave power generation systems include at least one power supply, one or more power amplifiers (PAs) for the amplification of a received signal, and

a system controller. An amplifier is a circuit allowing the conversion of DC-input power into RF output power [15]. The input RF power, which can be generated by a RF synthesizer [16], is distributed to each of power amplifiers. At ESS facility, a low level radio frequency (LLRF) module creates a high-quality RF signal for the power generation systems. Power amplifiers are the work-horse to carry the RF power in transmitters for radar applications [17, 18], for existing and next-generation telecommunications [19], for broadcasting communications [20–22], for satellite communications [23, 24], for heating applications [15], and for powering accelerating sections in linear accelerators [8]. For the amplifier design, there are many considerations of interest including: output power, efficiency, gain, bandwidth, frequency, reliability, stability, cost, etc. Depending on applications, trade-offs among parameters have to be made. For future wireless communication systems care should be taken in power amplifier (PA) design for linearity, large peak to average power ratio (PAPR), large signal bandwidth up to 100 MHz, carrier aggregation, beamforming and multi-input multi-output (MIMO) architectures. Future particle accelerators requires stringent requirements of high energy efficiency, beam availability and intensity. The future power generation systems for particle accelerators therefore impose challenges for their PA designs i.e. improved energy efficiency, higher output power, better stability and reliability, smaller footprint. Energy efficiency is a critical factor in a PA design and in power generation system design. For a PA design, efficiency is defined as two common terms consisting of power added efficiency (PAE) and drain efficiency (DE). PAE is a measure of efficiency in which the gain of the amplifier is taken into account allowing for the evaluation the conversion efficiency between the direct current (DC) input power and the produced output power i.e. $\eta = (P_{out} - P_{in})/P_{DC}$. PAE is widely used factor of merit as industry standards for power amplifiers [25], especially the ones for wireless communications and radar systems. DE is regarded as the ratio of RF output power to DC input power, i.e. $\eta = P_{out}/P_{DC}$. For power generation systems incorporating a number of amplifier modules and passive combining stages, the overall efficiency is then calculated as a combined efficiency of the sub-systems, see [**Paper V**]. At particle facilities, definition of energy efficiency of the power generation system is expanded in the form of the grid-to-beam efficiency which is a product of efficiency of the modulator, efficiency of power generation system, and efficiency of RF power to accelerated beam power [26].

To power the accelerating cavities, the output power is required in the range from 10 kW to MW that is realizable by employing either vacuum tube or solid state technology. Vacuum-tube power sources use extremely high voltage supplies on the order of few kV to hundreds kVs to generate RF power up to MW per tube, whereas solid-state RF power transistors are operated at low voltage i.e. tens of V with output power up to a few kW per transistor, thus the power combination needs to be also considered.
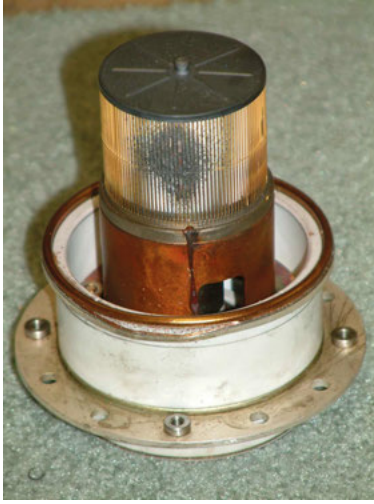
(a)
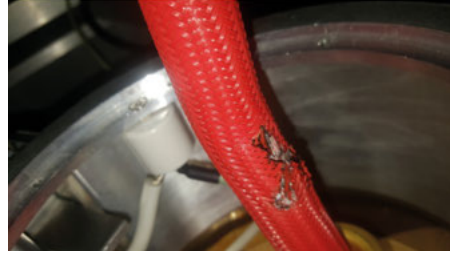
(b)

Figure 1.1. Pictures of damages found at a vacuum tube. (a) Damage found in the tube due to arcing happening at high voltage grid, (b) Arcing caused burn-out at the cooling hose connected to a tetrode-based tube.

The footprint of power generation system is determined by the size of amplifiers, which is dependent on the DC voltage and the operating frequency. To reduce the footprint of a power generation system with a given requirement of output power and efficiency, a designer should address challenges related to the increase of energy density within the amplifier. The increase causes higher operating temperature of amplifier, thus reducing the output handling capabilities of the amplifier. Also, a reduction of size of amplifier leads to an increased complexity, and higher cost for its maintenance.

For a power generation system, a power distribution system includes passive waveguide-based transmission lines or coaxial-based transmission lines depending on the power levels. The system distributes power to the target (antennas in communications, cavities in heating applications or in accelerator applications) with minimized loss i.e. 5% of total loss in [27]. Attention should be given in the design phase of power generation system for the power distribution system to save space and facilitate the installation i.e. in the ESS gallery [8].

1.2 Solid state power amplifiers (SSPAs) for particle accelerators.

The rapid and continuous improvement of solid-state technology allows foreseeing a replacement of high power vacuum tubes in the frequency range from 100 to 3000 MHz. The main driver for the adoption of the solid-state technol-
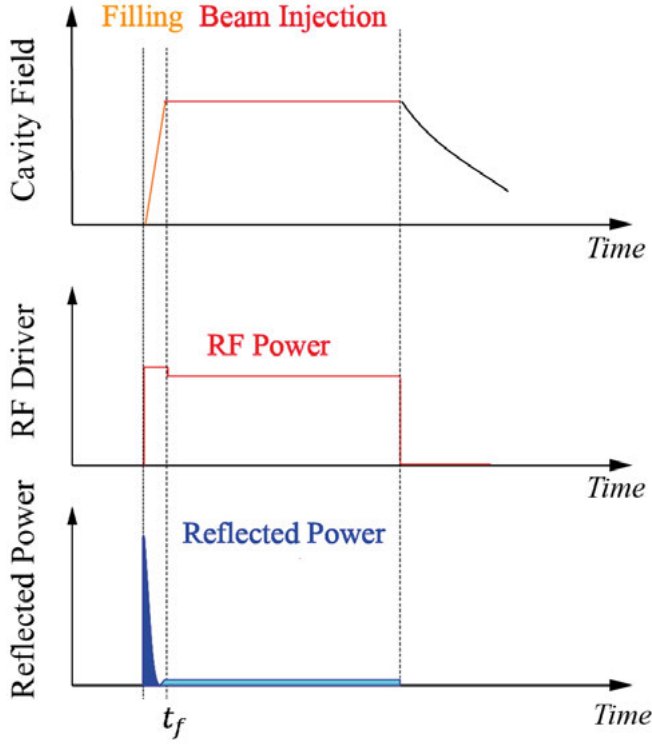
Figure 1.2. A profile of ESS operation of spoke cavities in time domain for cavity voltage, RF power source, and reflection power. During the filling time, the RF power generation suffers from a large amount of reflected power caused by mismatch of the cavitiy.

ogy is that the vacuum tubes with their extremely high voltage power supplies, typically in multi-kV, have lower reliability as compared to solid-state based amplifiers operating at a decreased voltage, two or three orders of magnitude lower. In addition and as we will demonstrate in this thesis, the use of SSPA allows for a drastic reduction of the energy used in driving SRF cavities, when adopting an optimal feeding profile in pulsed operation. Using SSPA technology, there are no multiple and strict constraints on the DC power supplies i.e. fast switching protection, cooling and space requirements of multi-kV power supplies for the vacuum tube amplifiers are not necessary. SSPA-based power sources show an extreme modularity, high efficiency, low phase noise, low harmonics, lower maintenance and operating cost, redundant design, no warm-up time, cost effectiveness and simple start-up procedures. Klystron [8, 28–34] and multi-beam inductive output tube (MB-IOT) [35, 36] remain strong candidates for mega-watt level projects, while SSPAs have already been a mainstream technology for mid-range power level projects in the range from a few kW to several hundreds kWs.

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The development of SSPA technology was pioneered at SOLEIL synchrotron to replace vacuum tube amplifiers for powering its booster (35 kW) and four storage rings (180 kW each). These amplifiers were based on metal–oxide–semiconductor field-effect (MOSFET) transistors, each delivering 330 W output power [37]. After a long operation of 11 years, these amplifiers have demonstrated an excellent operational availability and mean time between failures (MTBF $\approx$ 32000 hours) [38]. The successful development and demonstration at SOLEIL is then followed by ever-growing adoptions of SSPA technology at other facilities around the world, resultng in energy savings, cost reduction, compactness, improved reliability, ease for mass production and lifetime along with extending the technology to other frequencies ranging from the FM to the L band. Based on the scientific collaborations and technology transfer to industry from SOLEIL, a large number of projects among particle laboratories and industries have been realized, including: 50 kW SSPAs (476 MHz) for the storage rings at LNLS [39], 50 kW SSPAs (500 MHz) for driving SIRIUS boosters [40], 75 kW amplifier towers (352.2 MHz) with efficiency of 59% for booster ring at ESRF, [41], 50 kW SSPAs (500 MHz) with optimized efficiency of 56% for X-ray source ThomX [42], 4x80 kW SSPAs for SEASAME storage rings [43]. At conventional accelerator facilities, more issues are caused by mid-range power vacuum tubes during high power operation i.e. high voltage arcing, tube arcing, grid emission, increased price, and shortage of supply from broadcasting manufacturers [44, 45]. This leads to the need of collaborations with major industry actors using their expertise and experience in high power broadcasting applications to implement improved SSPA designs with superior performances to fully replace mid-range power vacuum tubes. Such projects include: 40 kW and 4x75 kW (500 MHz) delivered by Cryoelectra GmbH for synchrotron radiation source BESSY II with a reduction of the mains power in the order of 30% as compared to the use of Klystron amplifiers [46], 100 kW (500 MHz) SSPAs designed by Cryoelectra for CLS booster with extremely high redundancy i.e. no interruption if up to 14 transistors fail [45], 50 kW SSPAs (500 MHz) provided by BTesa for replacing IOTs of ALBA booster with hot-swap replacement capability even when operating at full power [47], 192 kW amplifiers (176 MHz) for radio frequency quadrupoles (RFQs) at MYRRHA injector produced by IBA [48], Rhode & Schwarz supplied 60 kW liquid-cooled SSPAs (100 MHz) to be used at MAX IV facility [49] with an option of using broadband amplifiers in a feedback loop to reduce the size and energy distribution of particle beam within the ring, SSPA technology is planned for the first time to reach MW-level i.e. 1.6 MW for powering RF cavities at CERN Super Proton Synchrotron (SPS) RF acceleration system [50]. Thanks to the emergence of Gallium Nitride (GaN) semiconductor technology, more projects are carried out using this disruptive technology at higher frequency up to L-band, such as: 20 kW CW GaN-based SSPAs (1.3 GHz) developed by SPE in LUCRECE project [51], 8 kW CW (1497 MHz) at JLAB as an replacement of

its Klystron [33], 5.2 kW (1.3 GHz) SSPAs for superconducting (SC) linear accelerator at SHINE [52]. Advances in solid-state amplifier technology also open new approaches for MeV-energy accelerators to be used for other applications i.e. aurora mapping, magnetic resonance imaging (MRI), radiation therapy [53]. Moreover, such advances in high breakdown voltage allows for addressing new concepts and new architectures (switched-mode matching networks in combination with coupling loop of cavity input) with the aim of improving efficiency and reduced footprint [54, 55]. Though GaN technology shows excellent performance in efficiency for accelerator applications, there still lacks of insightful reports regarding its reliability during a long run of operation as compared to LDMOS technology. Therefore, LDMOS technology is still a strong contender for applications in the frequency range below 600 MHz.

ESS aims at being the first carbon-neutral research facility [8]. Therefore challenges are taken to reduce the energy consumption, and improve the energy efficiency of next-generation power sources. An increase of 10% in efficiency of RF power sources results not only in a large reduction of the operational costs. Efficiency enhancement is a challenging topic in the RF/microwave community. Improved efficiency design comes at the cost of degrading other properties, such an increased complexity and cost, see [55]. A higher complexity makes it more challenging to implement PAs. Higher complexity of PA also leads to difficulties of tuning SSPA modules in a system due to amplitude and phase spread otherwise. For next-generation RF power sources, there is a growing demand of approaches towards improved efficiency, compactness, ease of productions and low-cost. Another issue of RF power sources when powering accelerating cavities is the capability of handling full power reflection due to mismatch during the cavity filling period [13], see Fig. 1.2. For high peak power amplifiers required in high intensity accelerator facilities, full reflection can cause damage if the die temperature is over even though high power solid state transistors demonstrate its ruggedness [56]. The reflection power is wasted and thus we should improve the overall energy savings of the RF power sources. Few solutions are carried out, however, remain theoretical studies [13, 57]. To our best knowledge, no practical study has been demonstrated for solving the reflection problem for SC linac, especially in case of ESS with requirements (RF pulsed 352 MHz, 14 Hz of repetition rate).

From module to system design of RF power sources, all SSPA modules and sub-systems (dividers, combiners) properties are correlated, i.e. as stated in [58]. For designers, prioritizing those different properties is challenging, especially regarding three key factors: the efficiency, cost and complexity. A good design is not only achieving the best DC-to-RF conversion but also offering a low cost and reduced complexity.

1.3 Thesis contributions and outline.

The research goal of this thesis is to develop the core technologies for addressing the needs of the next-generation RF power sources to be used for large-scale projects for particle accelerators i.e. ESS. The first part of the thesis gives some insightful perspectives on the design of SSPA modules, system design and use with ESS superconducting (SC) cavities [8]. These elements are required for the conceptual of a 400 kW peak power station, fulfilling ESS specifications (352 MHz and 14 Hz repetition period). In this thesis, the challenge of implementing an efficient design, which is a compromise of high efficiency, low complexity, and low cost, is undertaken in [**Paper I, III, IV, V**]. The efficiency improvement consists of innovative engineering solutions and is continued with high power combiners for the scaling up in power.

In chapter 2, the basic knowledge of linear accelerators is given through the architecture of the ESS linac [8], consisting of a normal conducting (NC) section and a superconducting (SC) section. This thesis presents a brief overview of the established vacuum tube technology in particle accelerator facilities. Such conventional technologies are a crucial core of RF power generation systems allowing for powering the accelerating structures and the linac. Some comments regarding the advantages and disadvantages of vacuum tubes-based systems are provided.

Chapter 3 focuses on the core corporate-combining architecture: a kW-level single-ended amplifier module, combining solutions from dozens Watts up to 200 kW power handling capabilities are demonstrated in [**Paper I, II, III, IV**]. A demonstration of a 10 kW SSPAs block is presented with an excellent performance in DC-to-RF conversion on the order of 71% in efficiency under ESS specifications in [**Paper V**]. Design considerations of the system level are presented from the tuning procedure to the evaluation of the stability in amplitude and phase. The unitary 10 kW sub-block uses a bank of capacitors to eliminate the extend of the associated power supply, however, this results in a drop of the drain voltage waveform, thus a drop of the output power within the pulse. A low-level RF controller realized in-house implements a feedback loop to facilitate solving the issue that may cause instabilities. Chapter 4 is a follow-up discussion based on the sub-block 10 kW SSPAs established by combining 8 individual modules. In the first part of the chapter, a few possibilities of architectures are discussed aiming for scaling up 400 kW to fulfill the requirements of the ESS spoke cavities. In the second part, the challenge of the full reflection happening during the filling period of the first 300 μs is addressed. For the first time, this thesis experimentally investigates experimentally the feasibility of adopting an optimal charging scheme, theoretically developed [13], to a high power generation system for powering the accelerating cavities. A demonstration of the feasibility using an amplifier module developed in [**Paper I**] is given in [**Paper VI**]. This demonstration is realized using envelope tracking techniques at kW level. This allows for realizing the
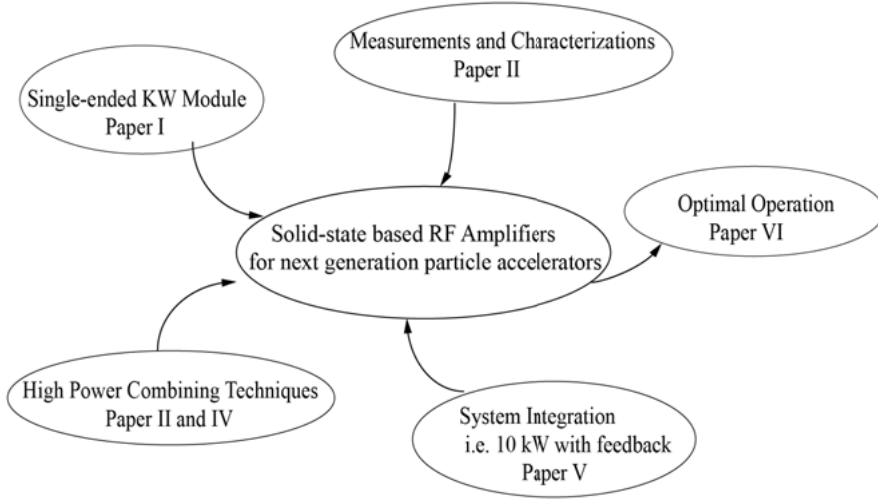
Figure 1.3. A structure of the works in this thesis.

optimal filling scheme towards minimizing the reflection power for high efficiency operation. The 400 kW power generation system based on 10 kW SSPAs sub-block is realised in chapter 3. The implementation of the optimal charging scheme is presented in [**Paper VI**] and results in an excellent reduction of about 24% the overall consumed energy as compared to the conventional scheme. The result of this, is corresponding to an increase in the overall efficiency of the whole ESS linac.

Chapter 5 concludes the thesis and discusses future work for the next-generation RF power sources not only for particle accelerators but also for other applications requiring high RF power levels.

2. Accelerators system

2.1 Particle Accelerators Basics

There are two kinds of radio frequency (RF) particle accelerators mostly in large-scale facilities: synchrotrons and linear accelerators. Several large-scale accelerator facilities are introduced in Table 2.1. For the synchrotron, the principle is based on the physical phenomenon that a moving electron emits energy when it changes direction. An electron gun produces the electrons by applying high voltage through a heated cathode, which is similar to the operating principle of cathode ray tube in standard televisions [59]. The produced electrons are guided to the linear accelerator (linac) in the form of pulses. The linac accelerates the electrons to an energy level which is required for injection into a storage ring. The high energy electrons are transferred from the booster ring to the storage ring, moving in the circumference at nearly the speed of light. As electrons move around the storage ring, they pass a number of magnet sections inside the accelerator ring allowing for the generation of X-rays (the synchrotron light). The X-ray beams tangent to the storage ring are conveyed into beamlines where experiments are performed.

Linear accelerator is another type of accelerators where acceleration of the beam is linear by RF electromagnetic fields and the beam passes the accelerating sections only once [60]. The concept of RF linear accelerator was first demonstrated experimentally in 1927 [61]. In this paper, an RF voltage with a peak of 25 kV was applied to a single metal tube between two ground electrodes, producing time-alternating electric field in each gap. A beam of charged sodium ions, emitted from the cathode, was then accelerated and gained with maximum energy when travelling through the gap. The beam energy was measured on the order of 50 keV, twice of the gap voltage of 25 kV. The experiment established the principle that the voltage gain of an RF accelerator could exceed the maximum applied voltage [62], since the particles arrive in gap at the right time to be accelerated. Therefore, the principle could be repeated on several drift-tube sections, allowing to achieve higher energies i.e. [8, 63, 64]. Fig. 2.1 shows a block diagram of a conventional linac structure. Beam of particles is generated by a DC injector system [65, 66]. Beam is then accelerated along a waveguide towards the target. The waveguide structure contains a series of accelerating resonant cavities, which are excited by E-fields created by an external RF power system, see Fig. 2.1. The RF system primarily converts DC power provided by a DC power system into RF power. The accelerating structures transfer the electromagnetic energy to the beam,
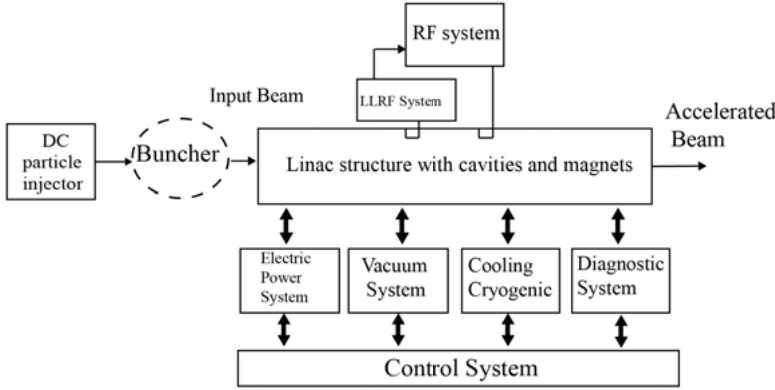
Figure 2.1. A simplified block diagram of a linear structure.

	SNS [67]	J-PARC [68]	ESS	ISIS [69]	LHC [70]
Particle Type	H^-	H^-	p	H^-	p
Beam Current	35 mA	15 μA	62.5 mA	0.25 mA	580 mA
Beam Energy	1 GeV	30 GeV	2 GeV	800 MeV	7 TeV
Beam Power	1 MW	0.75 MW	5 MW	200 kW	200 MW

Table 2.1. *A table of existing large accelerator facilities across the world.*

allowing for the particles to travel along the linac and help to focus the beam with support of focusing/steering magnets. Note that the shunt impedance is a valuable figure-of-merit for characterizing the accelerating efficiency of a given cavity geometry. A vacuum system is provided to make sure that the beam is not impeded by other particles during the acceleration. The entire system is cooled by water i.e. in a normal conducting accelerator, or by liquid helium i.e. in a superconducting accelerator. The continuous beam coming out of the DC injector system must be grouped into bunches when it enters the sequence of accelerating structures. In order to achieve maximum acceleration, the time period between bunches must be a multiple of one or more RF wavelengths.

The linear accelerator offers the capability for reaching high-intensity particle beams and for operating with high repetition pulses or continuous wave (CW), which allows for the acceleration of beams with high average current [62]. For the linear accelerator, the energy loss is minimized as compared to the circular accelerator since the beam is accelerated along the straight line. However, the advantage of the high energy comes at the cost of adding accelerating segments to the length of the linear accelerator, thus increasing its cost and maintenance.

RF superconductivity [71] is generating an increasing interest in technology of choice for future accelerators such as: ESS [8], the X-ray Free Electron
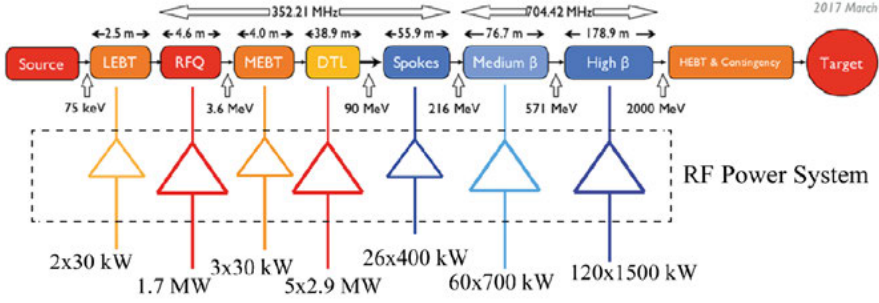
Figure 2.2. A layout of ESS linear accelerator.

Laser (XFEL) [72], the Linac Coherent Light Soucre (LCLS) - II [73] , and the proposed International Linear Collider (ILC) [74]. The use of superconductivity in accelerating cavities brings superior performances for applications requiring CW or long-pulse accelerating fields. This is due to the low Ohmic losses allowing for a high-field gradient and low power dissipation. This following section describes the ESS linac including the linac's components and some basic knowledge related to the operation of the linear accelerator with its superconducting spokes and elliptical cavities.

2.1.1 The European Spallation Source (ESS) Linac

As can be seen in Fig. 2.2, the ESS linac consists of a proton source, warm conducting sections, cold conducting sections, and a tungsten-based target. In the first step, the ion source generates hydrogen ions from heating hydrogen gas, which are later stripped of electrons in order to collect the protons. The formed protons are then guided and accelerated into a 48-meter-long normal conducting (NC) sections. The NC section includes: Low energy beam transport (LEBT) section, radio frequency quadrupole (RFQ) section, medium energy beam transport (MEBT) section, and drift tube linac (DTL) section. All of these sections are operated at a frequency of 352 MHz. The normal conducting section provides an energy of 90 MeV to the proton beam. The superconducting section is followed with 26 spoke cavities operated at 352.21 MHz, 60 medium-β and 120 high-β elliptical cavities operated at 704.42 MHz. At the end of the ESS linac, a tungsten-based target is bombarded by the proton beam with an energy of 2 GeV at nearly the speed of light, resulting in the generation of neutrons. The following paragraphs cover the details of several several sub-systems and give more insight into the ion source and superconducting sections.

Microwave Discharge Ion Source (MDIS):

The microwave-discharge source (MDIS) is placed at the pulsing heart of the ESS linac. This is required to produce a proton beam with a high current of 62.5 mA. The MDIS system is based on a microwave charge ion source [75] which is widely used for proton production. It uses alternating electric fields i.e. at 2.7 GHz to generate a plasma. The ESS proton source design is composed of a plasma chamber, an RF generator and RF distribution network, magnetic system, and an extraction system. The RF energy and the hydrogen gas are injected into a water-cooled, cylindrical plasma chamber through a RF waveguide-based distribution network in which the RF energy is provided to the chamber by using an RF generator at a resonance frequency of 2.7 GHz. The magnetic system includes three solenoids providing the axial magnetic field which allows tuning for matching the injected RF signals and the hydrogen gas. The ion source, the RF generator and distribution chain, and other components are installed on the high voltage 75 kV platform. The extraction system is composed of a plasma electrode, two extraction ground electrodes, and a repeller electrode. The proton beam is expected to achieve a beam energy of 75 keV with a maximum emittance of 0.2 π.mm.mrad, during the 2.86 ms pulse length at 5% duty cycle, and 99.9% reliability defined in [76]. The extracted beam is guided toward the first focusing solenoid of the LEBT.

Low Energy Beam Transport (LEBT):

The LEBT section is the first part of the warm conducting linac, following the extraction system of the ion source. The LEBT consists of two solenoids plus two correctors, one for the horizontal direction and one for vertical direction. The two solenoids are used for transverse focusing whereas the steerers are used for trajectory corrections. Two devices including an iris and a fast chopper, allow beam shaping. The LEBT provides the beam matching between the ion source and the next section RF quadrupole (RFQ).

Radio Frequency Quadrupole (RFQ):

The RFQ section takes charge of accelerating the extracted proton beam from the ion source, transversely focusing it, and longitudinally bunching it in providing the performance of acceleration in the further stages of the linac.The RFQ is based on a 4-vane structure resonating in the TE_{210} mode at 352.21 MHz. It is divided into 5 sections for a total length of 4.6 m. The beam energies at the output of the RFQ are on the order of a few MeV (i.e. for ESS RFQ the beam energy is 3.6 MeV). More details can be found in [77].

Medium Energy Beam Transport (MEBT):

The MEBT section acts as a steering and matching section between the upstream RFQ and the adjacent section DTL. It has 11 magnets, 3 buncher cavities, 1 fast chopper, 1 beam dump, 2 beam scrappers, and a set of beam instru-

mentation for diagnostics. The length of this section is on the order of 4 m. The use of the scrappers allows to remove the pulse head/tail during the transient times of the ion source and the LEBT, improves the beam quality as well as the beam losses due to the partially-chopped bunches [78].

Drift Tube Linac (DTL):

The drift-tube section is located in the last stage of the warm conducting part of the linac. It is made by 5 tanks with 173 drift tubes, which are equipped with beam position monitor (BPM), electromagnetic dipole (EDM) , and permanent quadrupole magnet (PMQ) [79]. Each of the tanks requires a power generation of 2.2 kW to increase an energy for a proton beam current of 62.5 mA from 3.6 MeV to 90 MeV. The DTL is designed to operate at 352 MHz with a duty cycle of 4% and 2.86 ms pulse length.

Spoke cavities:

The superconducting linac starts with the spoke section, which will accelerate the proton beam extracted from the DTL section from 90 MeV up to 216 MeV. The spoke section has a total of 26 cavities for a total of 56 m in length. The spoke cavities are made of Niobium, designed to be matched at relative beam velocity of $\beta = 0.5$. Two spoke cavities are paired in a cryomodule and are immersed in helium liquid at 2K since Niobium becomes superconductor when cooled below 9K. The SRF spoke cavities require an accelerating field of 9 V/m, which is realizable by using an average power of 250 kW per cavity. Insights of design and testing can be found in [80, 81].

Medium-β and High-β sections:

The spoke section is followed by the accelerating structures, consisting of 60 medium-β and 120 high-β elliptical cavities. Those cavities occupy the longest portion of the ESS linac (about 256 m in length). In this section, acceleration is performed at the resonating frequency of 704.42 MHz with an energy transition at 571 MeV until the proton beam reaches 2 GeV at gradient of 18 MV/m, prior to the HEBT section [82]. Testing performance of the section can be found in [83].

High Energy Beam Transport (HEBT):

After acceleration up to 2 GeV, the proton beam is transported from the linac tunnel to the target which is 4 m higher at the surface level. The HEBT section inclues: a 128-m upgrade high-β (UHB) sub-section, a 69-m-long dogleg, acceleration to target with total length of 45 m, and a beam dump line sub-section [84]. The UHB sub-section provides space for extended cryomodules if upgrades in the future are made, and for contingency purposes. Then, the achromatic dogleg is to steer the proton beam 4 m up to the target level. The last sub-section is to transport the beam to the target using a set of 6 quadrupoles and 8 raster magnets. More details are given in [84].

Tungsten Target Station:

At the target section, the spallation process is performed, resulting in the production of high-intensity neutron beams. The more neutrons are produced in the collision of the spallation process, the brighter the neutron source is. ESS will be 100 times brighter than any of the existing spallation sources. The target is made of tungsten, divided into 33 sectors with 2.5 m in diameter. Proton beam pulses are synchronized with the rotation speed of the target at 25 rpm. The high-energy spallation neutrons are transformed into slow neutrons at the speed of sound by using the moderator-reflector assembly carefully surrounding the target [85]. A radiation shielding system of 7000 tons of steel is surrounded the target and allows to prevent unwanted radiation from leaking. The beam extraction system provides the neutron beams via beam guides located in arcs around the station. These slow neutron beams are accessible at the surface of the station to spectrometers, allowing scientists to carry out their experiments.

2.1.2 Some basic definitions

This section covers insightful explanations of the basic terms and definitions which are commonly used in particle accelerators.

Acceleration and focusing:

The acceleration/bending/focusing processes are described by the Lorentz force, as the total force on a charged particle moving through both an electric field and a magnetic field:

$$\frac{\mathrm{d}\vec{p}}{\mathrm{d}t} = q(\vec{E} + \vec{v}\vec{B}) \qquad (2.1)$$

in which $\vec{p}$ is the particle momentum, $\vec{v}$ is the velocity, q is the electric charge. Particles are accelerated by electric fields, whereas they are focused and bent by magnetic fields (i.e. quadrupole focusing with 4-poles magnets).

Particle velocity and energy:

Particles are divided into light particles and heavy particles. The light particles (i.e. electrons) reach a constant velocity at relatively low energy. The acceleration process occurs at constant particle velocity. Heavy particles (i.e protons and neutrons) reach a constant velocity at high energy. The velocity changes along the linac during the acceleration process. ESS proton linac has a number of accelerating structures, each optimized in geometry and energy for accelerating the proton beam to a high energy of 2 GeV.

Electrostatic acceleration:

The principle of electrostatic acceleration was used for the first time in the Cockcroft-Walton accelerator [86]. If a particle travels through an electric
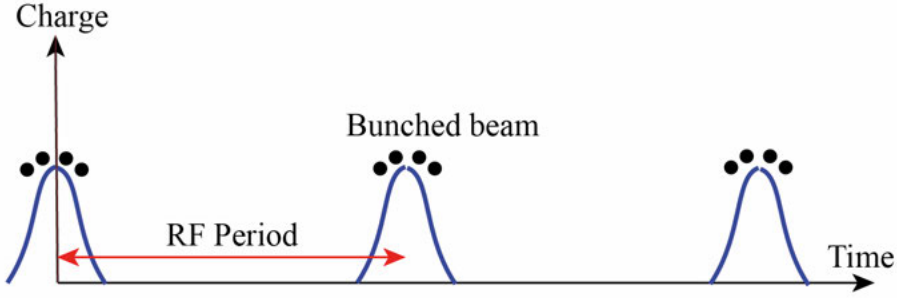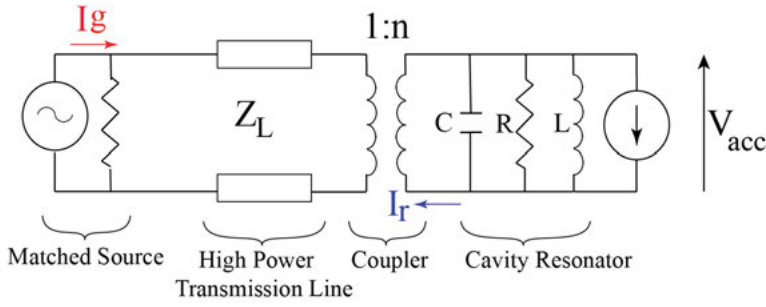
Figure 2.3. A picture of RF acceleration in time.

Figure 2.4. A schematic of resonant cavity with a RF generator, a coupler, and high power transmission lines.

field generated by a potential V, it will gain a kinetic energy:

$$\Delta E = q \times e \times V \tag{2.2}$$

in which 1 eV is the energy of an electron accelerated under a potential of 1 V. Electrostatic acceleration is often used at the sources section of accelerator.

RF acceleration:

The electrostatic accelerator is limited in accelerated energy since it requires practical potential difference. The particle is passed through an RF field which is provided by a RF generator. This concept was first used in the acceleration of particles of higher energy, with low gap voltage [61]. The accelerating electrodes must be arranged such that the accelerating field changes as the particle passes at the right point. This is also a conventional method of producing bunched beam [87], see Fig. 2.3.

RF accelerating cavities:

The acceleration technique presented in [61] requires the relativistic factor $\beta \ll 1$, thus it is unable to apply for relativistic particles. The relativistic

factor β is defined as the ratio between the velocity of a moving particle and the speed of light. As particles get high velocities, the energy gain per unit length decreases, resulting in a longer drift spaces in order to deliver higher accelerating gradient. Therefore, a design of high frequency is needed allowing a required increase in the accelerating gradient. To do so, a popular scheme in particle accelerators is to have a series of resonant cavities in which the resonant frequency matches the RF generator frequency. The RF cavity is a metallic chamber that confines an electric field in the form of the cavity modes. For almost all RF cavities, the TM_{010} accelerating mode is preferably used since it has a longitudinal electric field, therefore it accelerates particles in the direction of propagation. The modes of the cavities can be excited by RF generators coupled to cavities using waveguides, capacitive/inductive coaxial cables, etc. Resonant modes of EM waves in a cavity can be represented by a equivalent resonant R-L-C circuit, in Fig. 2.4. The equivalent circuit is used allowing for analyzing the build-up of electric fields as the result of a reflection of waves inside the cavity during the charging time, see [**Paper VI**]. Cavities can be made of normal conducting or superconducting materials depending on requirements of accelerating gradient, pulse length, duty cycle, average beam current, etc. Multi-cell structure is an array of accelerating single cavities with only one RF input coupler, thus reducing the number of RF sources [88].

Principle of phase stability:
As mentioned in previous sections, energy gain of the particles travelling along the accelerating cavities depends on the arrival time of the particles (or arrival phase ϕ_S). The accelerated particles in the linac remain to be synchronized with the accelerating fields, called synchronous particle with a synchronous phase on the positive slope of the RF voltage see Fig. 2.5. The particles that arrive earlier than the synchronous phase point (black dot) will gain less energy whereas the particles coming at late phase will experience higher energy. This provides longitudinal focusing of the beam in which a longitudinal restoring
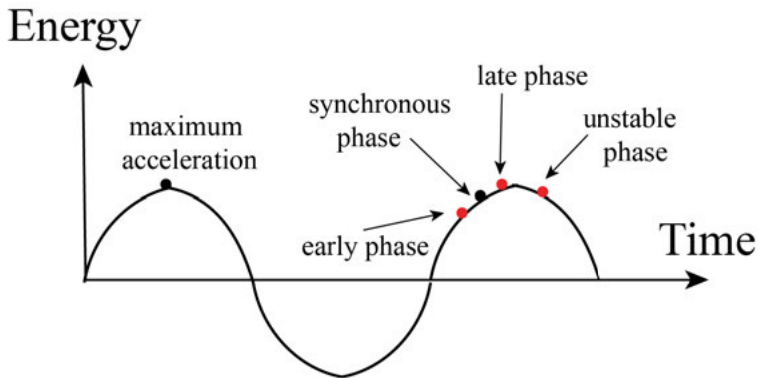

Figure 2.5. Energy gained by a particle as a function of arrival time.

force exists when the synchronous phase is chosen corresponding to a time-varying field [62]. Forces keep the beam oscillating about the synchronous phase, providing phase stability. For ESS baseline design, phase stability is one of stringent requirements. This is specified to be 0.1^o [8].

2.2 Review of power generation sources for particle accelerators

In this section, a review of technologies for power generation systems to be used in particle accelerators is introduced. The review covers a broad range of established technologies including: Tetrode amplifiers, Inductive Output Tubes (IoTs), Klystron amplifiers.

2.2.1 Tetrode-based amplifiers

Tetrode vacuum tubes are established in the frequency band ranging from 30 MHz to 400 MHz. The output power is technically dependent on the maximum current density from the cathode and the maximum power density dissipated by the anode [89]. Similar to a conventional grid tube, the Tetrode TH595 has 4 active- electrodes, including: a filament, a control grid, a screen grid and an anode plate. They are arranged in coaxial structure in which the cathode is inside and the insulated anode is outside, see Fig. 2.6. The spacings between electrodes must be small enough to allow the short transit time of electrons from cathode to anode. Each of the electrodes is connected to a single power supply. For the 400 kW tetrode-based amplifier at FREIA, two tetrode (TH595) from Thales are used, each delivering 200 kW peak power in pulsed mode. A single anode power supply from Astron Electronic AG is used to provide DC voltage of 16 kW for two tetrode amplifiers combined with a bank of capacitors, crowbar unit for protection, high voltage limiters, and filters [90]. The disadvantage of this configuration is that once arcing happens at one amplifier, this could lead to a damage to the other amplifier. The high voltage anode power supply is quite bulky and accounts for 3 racks 5U-19-inch plus room occupied by the high voltage capacitor in the system [91]. For the filament power supply, an AC voltage single phase supply is used to ramp the voltage from 0V to 8V for the filament. It takes 10 minutes for the warm-up operation. For the control grid power supply, it generates negative voltage of -173 V with respect to the cathode for a class AB operation. The screen grid is used for suppressing the Miller effect, thus avoiding instability at high frequencies. The power supply for the screen grid is maintained constant at 900 V, far below the anode voltage. Along with the water-cooled and air-cooled system, each of tetrode amplifiers accounts for 25% of the power station's space.

The available gain of the TH595 is on the order of 12 dB. Therefore, a 10 kW driver stage is required in oder to deliver an output peak power of
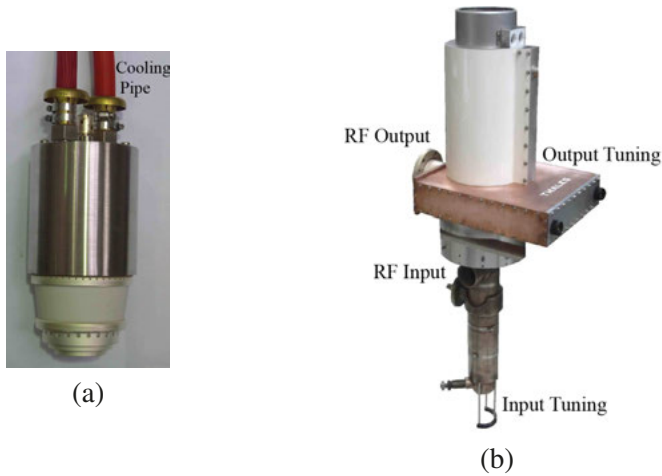
Figure 2.6. A picture of Tetrode-based amplifier in the power station installed at FREIA. (a) Tetrode TH595, (b) Tetrode cavity TH18595.

200 kW. Yet another requirement of space for the tetrode-based station when delivering higher output power is that a bulky combiner is necessary i.e. a 3-dB hybrid combiner is located on the top of the station for combining 2 outputs from tetrode amplifiers into a total of 400 kW output power. Using such hybrid combiners results in an addition of high power loads (i.e. 200 kW at the load arm of the combiner). For such configuration, the loads should be capable of handling high power if one tube fails and isolate the other one. The anode efficiency of the system is measured on the order of 60% at the nominal max output power of 200 kW [91] under ESS pulsed condition [8].

2.2.2 Inductive output tube amplifiers

For tetrode amplifiers, the output power is limited due to the power dissipation within a small volume [89]. Such constraint can be overcome by isolating the electron beam and the RF output circuit, see Fig. 2.7. This was firstly demonstrated by Haeff in his invention called "Inductive Output Tube" [92]. In an IOT amplifier, major components include: electron gun, anode, input cavity, output cavity, collector, see Fig. 2.7. An electron gun is used to emit electrons, which then are accelerated towards the collector. An RF signal is applied to the gap between the grid electrode and the cathode. The grid is based at a negative DC voltage (i.e. similar to a class-B operation). This allows the formation of electron bunches. The bunches are accelerated by the electric fields between the anode and cathode. The bunches excite resonant fields at the output re-entrant-based cavity and the magnetic field induces a current in the cavity. The output power is then extracted via an inductively coupled coaxial line.
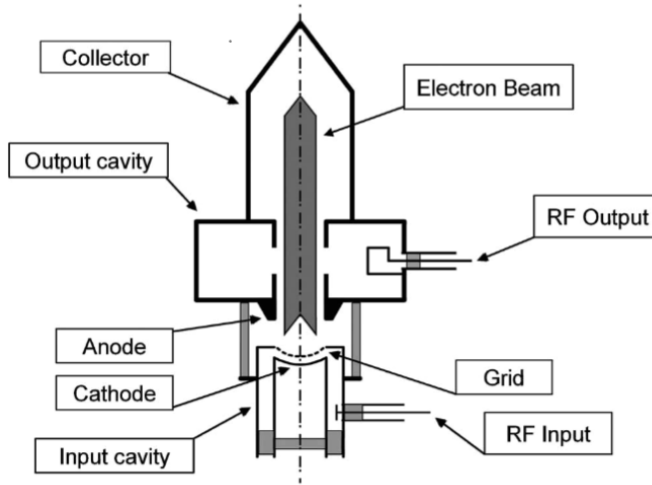
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Figure 2.7. The architecture of a conventional IOT amplifier. Reprinted with permission from [93]. Copyright IEEE 2009.

IOTs generates their output power from the modulation of the beam via the output cavity. Therefore, the output power can be increased as high as the beam voltage, resulting in a high conversion efficiency in the range from 70% to 80%. For IOTs, the output and input are completely isolated, thus the input and output are easily tuned. The lifetime of IOTs is reported to be over 40000 hours as compared to 20000 hours for tetrode amplifiers [94]. Mutli-beam IOT is demonstrated [36] with 1.2 MW output power at 704 MHz and is a potential candidate to replace the Klystron technology for ESS high-β cavities. However, this technology is still under development and some challenges should be taken into consideration. The limit of the beam voltage due to the voltage breakdown in vacuum practically results in a boundary of the output power for this technology (i.e. 100 kW output power for a single IOT). Due to a large potential between anode electrode (more than 27 kV of applied voltage) and cathode electrode, arcing might happen causing the deterioration of performance, thus reducing the lifetime of the tube.

2.2.3 Klystron amplifiers

To date, Klystron is the technology of choice in particle accelerators when requiring extremely high power (i.e. in the range of MW) and high frequency (i.e. up to GHz). Klystron amplifiers work on the principle of velocity modulation. An electron gun produces a stream of electrons travelling at same speed. The electron beam then passes through a pair of spaced grids, which is called buncher grids. The buncher grids are connected to a resonant cavity producing an electric field between them. The electric field alternately accel-
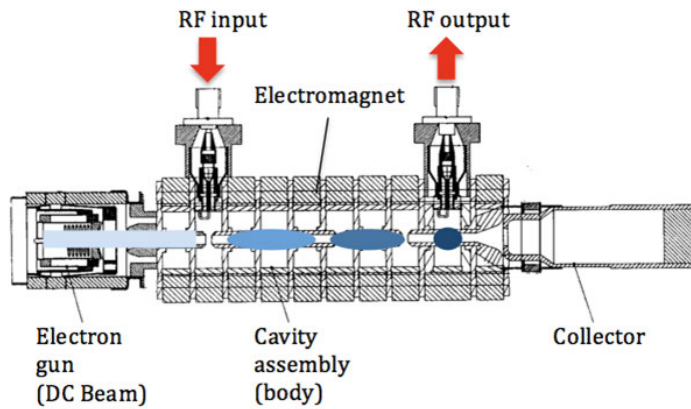
Figure 2.8. The architecture of a conventional Klystron amplifier. Reprinted with permission from [97]. Copyright Research Study Press (1994).

erates and decelerates the electron beam passing the section, forming bunches of electrons. The buncher grids are followed by the catcher grids. The RF current carried by the beam produces an RF magnetic field, which then excites by using the second catcher cavity. The position of the cavity is determined by the transit time of the bunches at the same frequency of the buncher and catcher cavities, thus allowing for maximally transferring energy to the output. The number of cavities can be more than two allowing for an increased gain or bandwidth. For ESS elliptical cavities [8], Klystron amplifiers from Toshia are used allowing for 1.5 MW peak power at 704 MHz in pulsed mode at a repetition frequency of 14 Hz. A high power modulator [95] is needed to operate the Klystron. Insights of test stand and results can be found in [96].

3. Results

The working principle of the solid-state based power system is determined by both how the individual modules are operated and how the outputs are combined. The choice of system architecture depends on the demand of output power, transistor technology, and combining method, see Fig. 3.1. This chapter gives the insights needed to understand and design the system from amplifier modules to combiners. The know-how to integrate individual components for scaling up the output power is also discussed. In this chapter, the system design approach starts with a discussion about the single-ended architecture at the kilowatt module. It is shown that the feasibility of single-ended configuration allows for high efficiency, simple architecture for mass production [**Paper I**] as compared to other major configurations i.e. the push-pull configuration [98]. Since ESS SC cavities require high peak power i.e. 400 kW for ESS spoke cavities, thus a few hundreds of kW modules are needed. The simplicity of the single-ended architecture facilitates the fabrication and the tuning procedure when combining them. The validation of the single-ended solution applied to a PA design is characterized in time domain to make sure that it meets the stringent demands for amplitude and phase at kilowatt level [**Paper II**]. This chapter shows also engineering solutions of combiners based on con-
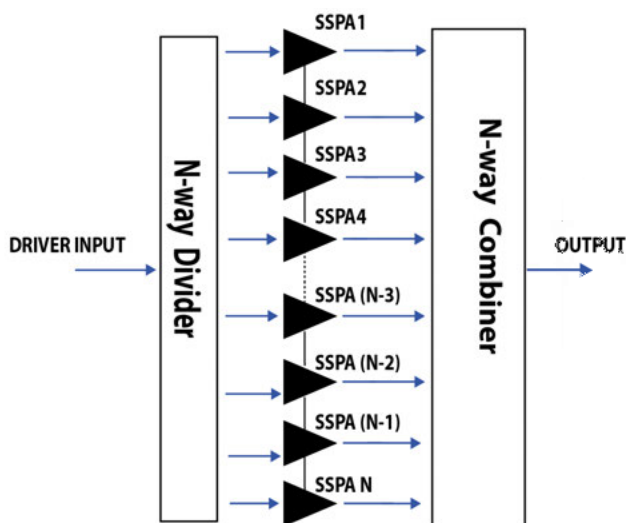

Figure 3.1. A conventional block diagram of N-way power amplifier system with N number of power amplifier modules and divider/combiner.

ventional Gysel topology [**Paper III**] and re-entrant cavity structure [**Paper IV**]. All combiners satisfy the requirements of low loss and high power. For the Gysel-based combiner, it was demonstrated to operate with low loss at 10 kW [99], 20 kW power level [*Paper III*]. The reentrant-cavity combiner is tested at a power level of few hundreds kW. This chapter provides insights of the integration process in which each of stages is designed and fine-tuned following a specific procedure to achieve the objectives of performance i.e. output power, stability, linearity, amplitude and phase imbalance, etc. Each of the single modules in the system is tuned in a systematic way to achieve the best combining efficiency regarding amplitude and phase [**Paper V**].

3.1 High efficiency LDMOS-based power amplifiers

Push-pull circuit configuration has been widely used [100, 101] since it allows for the realization of wide-band power amplifiers [102–104] usually combined with an ultra-wide-band balun [105], high output power [106–111], and enhanced even-order harmonic suppression [112, 113]. The push-pull configuration uses a pair of similar transistors, connected through a balun (balanced-unbalanced) transformer at both input and output. The two devices are biased in deep class AB mode [114–117]. The key benefits of push pull configuration are reduced common lead effects and impedance benefit for easy in/out matching [118]. However, the requirements of balance among branches in baluns is challenging, since any imbalance reflects back to the transistors, i.e. amplitude difference among input signals to each of branches or among unequal loads to the transistors. The design of power stations for particle accelerators, baluns (i.e. coaxial type) seems not to be practically suitable when a few hundreds of power amplifier modules are needed. **The push pull configuration was not chosen for the solid-state based system in this thesis.** Instead, the requirements from ESS i.e. the extremely narrow bandwidth [8] justifies the use of the single-ended configuration [**Paper I**] with the specifications for European Spallation Source (ESS) at 352 MHz in pulsed mode with a duty cycle of 5%. In addition, the distributed design approach for single-ended amplifiers brings a range of advantages, i.e. simplicity in design without a need of baluns, suitable for mass production to build up 400 kW stations [119], and represents an economical design. It was demonstrated that the single-ended amplifier [**Paper I**] can deliver output power in the kilowatt level with superior performance in efficiency thanks to the choice of transistors and harmonics suppression of the developed resonant matching technique.

3.1.1 Realization of single-ended design at kilowatt level

The solid state power amplifier (SSPA) module was built around the LDMOS BLF188XR transistor, see in Fig. 3.2. Efficiency and output power are the two most important design constraints imposed on the design approach. In the
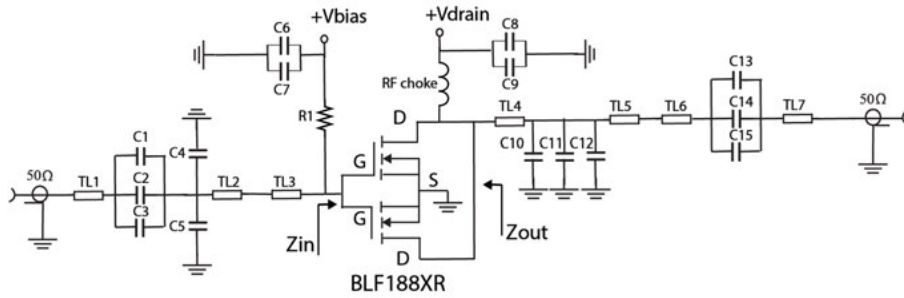
Figure 3.2. A schematic diagram of the single-ended amplifier module. Reprinted with permission from [121]. Copyright Wiley (2018).
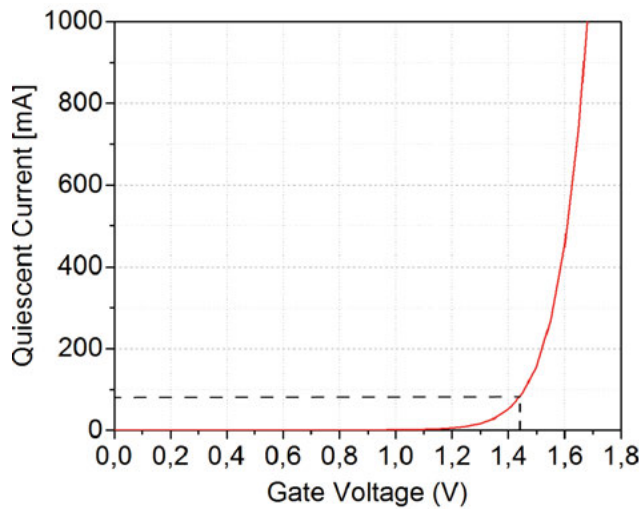

Figure 3.3. The quiescent current of BLF188XR is a function of gate voltage.

solid-state based power generation systems for the future accelerators mentioned in Chapter 1, the constraint of efficiency is firstly considered. In the first step of the design, it is important to decide on the modes of operation i.e. the class B, C, D or E, F, in order to perform a high-efficiency design [15]. Conventionally, high-efficiency amplifier configurations can be determined by adjusting bias voltages and RF input signal [118]. Depending on bias and RF input signal, the conduction angle is reduced allowing for improved efficiency i.e. class B or AB. The quiescent current is set to 80 mA for deep class AB operation at gate voltage of 1.48 V, see Fig. 3.3. Large-sinal simulations are conducted using BLF188XR's model provided by Ampleon [98]. The source and load impedances are obtained for the amplifier design, $Z_{in} = 0.36 - j0.72 \ \Omega$, $Z_{out} = 0.35 + j0.37 \ \Omega$ respectively. Next, the impedance matching using transmission line theory [120] is realized for input and output.
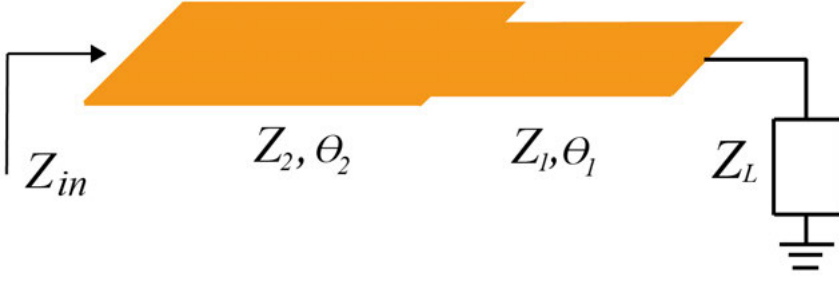
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Figure 3.4. Layout of the SIR structure with one end terminated Z_L.

Both input matching and output matching networks are based on stepped-impedance resonator (SIR) structure [122–127] at frequency of interest 352 MHz $\pm$ 2 MHz. In the design approach, SIR structures are formed by a cascade of two-stepped transmission lines with different characteristic impedance. Fig. 3.4 shows the SIR structure with one end connected to load Z_L. The input impedance seen from the open-end of the structure is denoted as Z_{in}. The input admittance can then be derived as following:

$$Y_{in} = \frac{1}{Z_{in}} = Y_2 \frac{Z_1 Z_2 + jZ_2 Z_L \tan\theta_1 + jZ_1 Z_L \tan\theta_2 - Z_1^2 \tan\theta_1 \tan\theta_2}{Z_1 Z_L + jZ_1^2 \tan\theta_1 + jZ_1 Z_2 \tan\theta_2 - Z_2 Z_L \tan\theta_1 \tan\theta_2} \quad (3.1)$$

in which θ_1 and θ_2 are the electrical length of transmission line sections. The parallel resonance occurs when $Y_{in} = 0$. The resonance condition can be written as:

$$Z_1 Z_2 + jZ_2 Z_L \tan\theta_1 + jZ_1 Z_L \tan\theta_2 - Z_1^2 \tan\theta_1 \tan\theta_2 = 0 \quad (3.2)$$

or,

$$Z_1(Z_2 - Z_1 \tan\theta_1 \tan\theta_2) + jZ_L(Z_2 \tan\theta_1 + jZ_1 \tan\theta_2) = 0 \quad (3.3)$$

K is defined as the electrical length ratio of the resonator:

$$\theta_1 = K\theta_T \quad (3.4)$$

$$\theta_2 = (1 - K)\theta_T \quad (3.5)$$

, in which θ_T is the overall electrical length of the resonator. The Eq. 3.3 can be re-written as:

$$Z_2(Z_1 + jZ_L \tan(K\theta_T)) + jZ_1(Z_L + jZ_1 \tan(K\theta_T)) \tan(1 - K)\theta_T = 0 \quad (3.6)$$

Numerical simulations are performed for the input and output resonant matching networks using Keysight Advanced Design System (ADS). For the
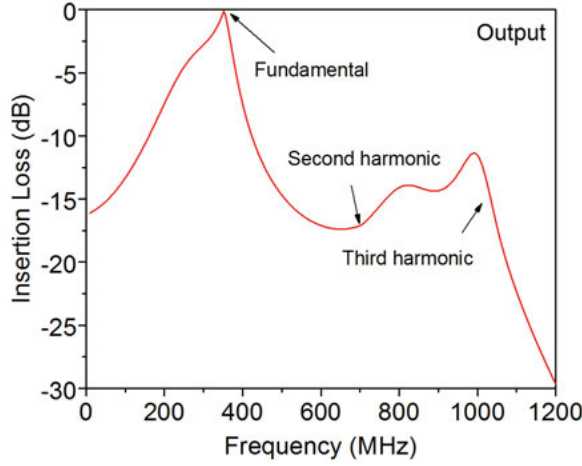
Figure 3.5. Characteristic of harmonic filtering as a function of frequency at the output matching network.

nominal power $P_L = 1250\ W$, the simulated input and output impedances are close to the short-circuit. These matching networks at input and output are based on SIR structure and act as band-pass filters at the resonant frequency of 352 MHz allowing for enhancing attenuation of the second and third harmonics. In this design approach, the harmonic filtering shapes waveforms at the drain towards i.e. class F [15]. The simulated results of harmonic filtering are shown in Fig. 3.5. At the output port of the amplifier [**Paper I**], the second harmonic and third harmonic levels are obtained -17 dB and -15 dB respectively.
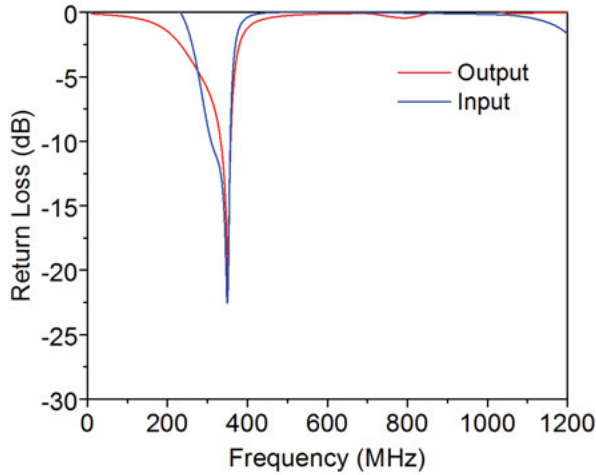

Figure 3.6. The return loss versus frequency is simulated at the input and output.
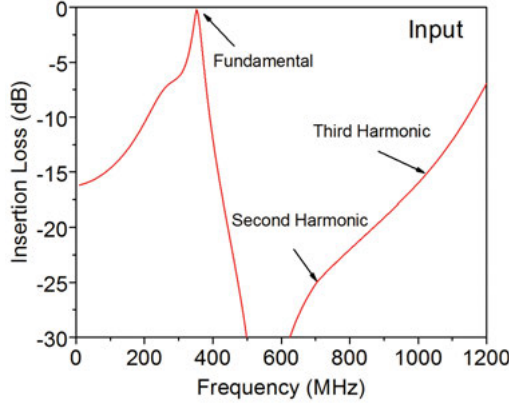
Figure 3.7. Characteristic of harmonic filtering as a function of frequency at the input matching network.

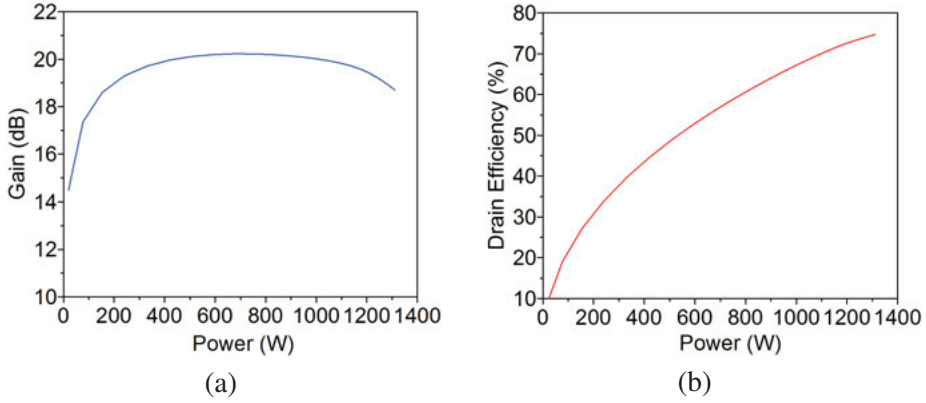
(a)   (b)

Figure 3.8. Gain and efficiency simulation results are as a function of output power. Adapted with permission from [128]. Copyright (2016) IET.

For the input matching port of the amplifier, second harmonic level is simulated as better as -25 dB, while the third harmonic level is -15 dB. Large-signal harmonic balance is then performed with BLF188XR model using ADS [129]. Harmonic balance solver allow for validating the full amplifier with input and output matching networks as simulated in Fig. 3.5 and Fig. 3.7. A capacitor is added close to the drain of the transistor for improving the matching conditions of resonance. The optimal value of the capacitor is 27 pF and was splitted into 3 smaller capacitors (C_{10}, C_{11}, C_{12}) to avoid overheating, which is caused by high current i.e. 35 A at kilowatt output power, see Fig. 3.2. Efficiency and output power can be slightly tuned by moving those capacitors further from or towards the transistor. For a large number of similar modules, this fine tuning process can be used to compensate the variation among active devices, allowing for improved combining efficiency. In this high power design,
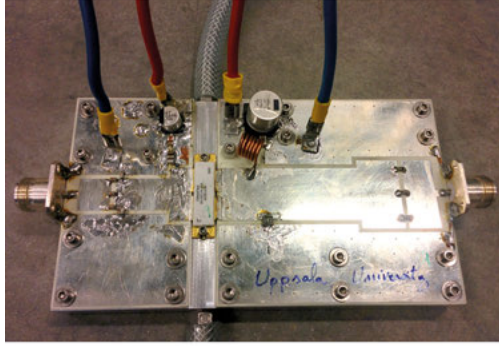
Figure 3.9. A picture of the prototype amplifier manufactured in RO3003. Adapted with permission from [128]. Copyright (2016) IET.

several coupling capacitors are used at the input (C_1, C_2, C_3) and the output (C_{13}, C_{14}, C_{15}). Details of the design considerations can be found in [**Paper I**]. The simulated characteristics of the gain and the efficiency are obtained, see in Fig. 3.8. The simulated efficiency is on the order of 73% as delivering 1.25 kW output power at 5% duty cycle.

The design is realized on RO3003 substrate with $\varepsilon_r = 3, \tan\delta = 0.001$, copper thickness = 35 μm, substrate thickness = 76 μm. All of the microwave capacitors are chosen from American Technical Ceramics 800B's series, which offer low equivalent series resistance (ESR), very good heat transfer for high power applications. The heat is dissipated through an aluminum base plate. The base plate is provided with a tube of 10 mm in diameter. Water-cooling is located 10 mm under the transistor flange, see Fig. 3.9. One should note that if there is a drop of more than 5% in power over a short period of time, it is probably due to overheating. The cooling system might be improved [130], allowing for better thermal transfer from heat sources to heat-sink.

The characterization is performed in both frequency and time domain. In the frequency domain, hot S-parameter measurements [131–133] are implemented allowing for fine-tuning matching networks at high power level, i.e. above 1 kW. Fig. 3.10 introduces a block diagram of hot S-parameter setup at kilowatt power level. Details can be found in [119] regarding the measurement setup and results. For the RF power generation systems to be used at ESS, the requirements of amplitude and phase variations are stringent i.e. 0.1% in amplitude and 0.5% in phase [8]. To validate the design in [**Paper I**], time-domain characterization is implemented with a measurement setup [**Paper II**] developed for high power level. The integration of SSPA-based system will benefit from time-domain measurements i.e. evaluating any imbalances in amplitude and phase among individual modules in order to achieve the best performance in combining efficiency. In the following sub-chapter, the time domain characterization and measurement results will be presented.
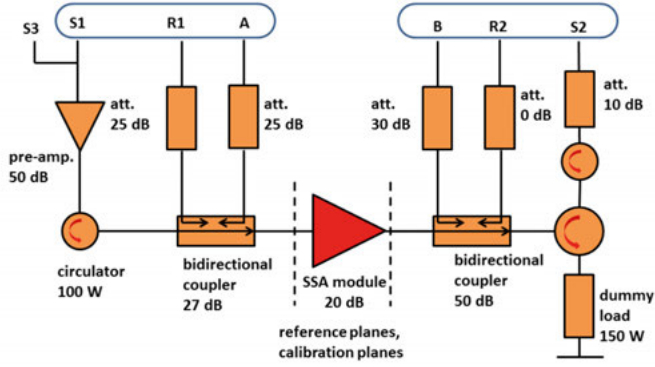
Figure 3.10. A picture of block diagram of hot S-parameter setup. Reprinted with permission from [119]. Copyright (2014) JACoW .
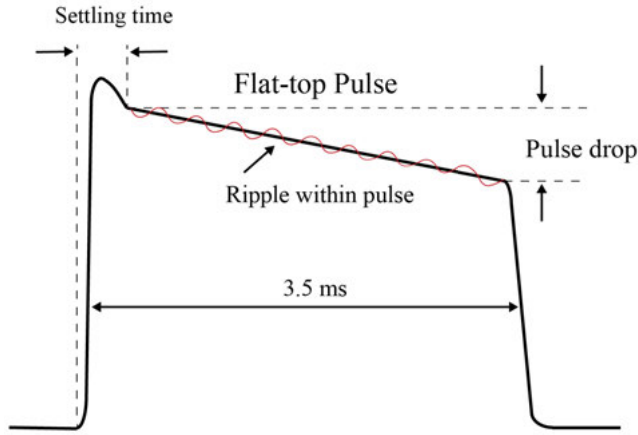

Figure 3.11. An example of pulse profile in time domain.

3.2 High power time-domain characterization

The energy use for accelerating the particles should be constant during the pulse of 3.5 ms. The particle accelerator, i.e. superconducting cavities, must establish a stable accelerating voltage to supply the same energy. The stable accelerating voltage needs from the RF power station with a stability performance in amplitude of 0.1% and phase of 0.5^o [8]. Concerns about such power generation system include pulse drop, variations during the flat-top of the pulse, pulse-to-pulse stability, rise time, fall time, see Fig. 3.11. These constraints are of paramount importance when using solid state amplifiers as a power generation system. One issue about solid-state based power amplifiers is that they exhibit pulse drop in which the amplitude of a pulse trails off over time [117, 134–138] as delivering high peak output power, i.e. kW output range. This causes instability in particle accelerators when the beam is
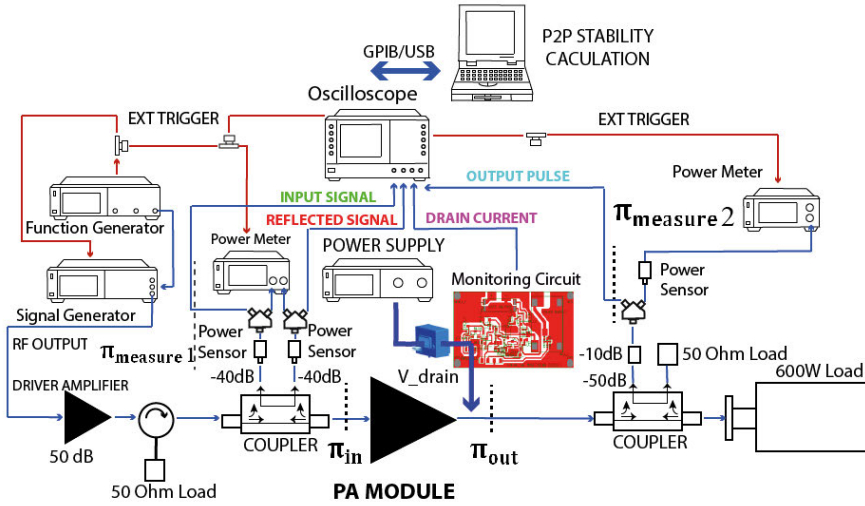
Figure 3.12. A picture of RF pulse profile measurement setup. Adapted with permission from [121]. Copyright (2018) Wiley.

injected with inconsistent experienced energy during the pulse. Another cause of instability considered is the risk of pulse-to-pulse (P2P) stability. P2P instability is characterized by variations of envelope amplitude and phase over time for successive RF pulses. For system level characterization, P2P stability is normally characterized at the very final step of the design process. This leads to insufficient knowledge on the limitations for the power amplifier module regarding amplitude and phase noise. This sub-chapter presents the development of a time-domain characterization methodology for high power SSPA module [**Paper I**] operated in pulsed mode. The non-linear time-domain simulations at the circuit level allow to gain an early insight into the design matching solutions and identify actual causes of instabilities. Such instabilities are due to over-heating or pulse-to-pulse random variations, and transistor technologies [139]. The time-domain characterized results are then be used by the low level RF (LLRF) controller [140] as priori knowledge for implementing the suitable control strategies, i.e. strategy for the compensation of the power droop compensation, see [**Paper V**].

3.2.1 Measurement setup

In [**Paper II**], the block diagram of the time domain characterization setup is presented, see Fig. 3.12. The measurement setup is well-suited for high power levels ranging from few hundreds of W to kW. Two receiver architectures are used for the realization of the time-domain measurement setup including zero-IF [141–143] and heterodyne [139, 144, 145] architecture. The

setup in [**Paper II**] is based on heterodyne architecture in which the local oscillator (LO) can be tuned to bring the input frequency range into intermediate frequency (IF) for extracting desired information. After mixing, the image frequency is suppressed by a low-pass filter, allowing to meet the image rejection requirements. An additional mixing is implemented to extract the I (In-phase) and Q (Quadrature) signals. The extracted data is captured and analyzed via a Matlab-based platform to realize the characterization of the pulse profile. The heterodyne technique offers a wide range of advantages including DC-offset cancellation, an extent relaxation of I-Q mismatch, good sensitivity. These are the main reasons why the heterodyne architecture is used for measuring time-domain performance of the SSPA module [**Paper I**]. In the heterodyne setup [**Paper II**], the RTO1024 oscilloscope is used as heterodyne receiver [146]. Details of measurement setup can be found in [**Paper II**].

For time-domain characterization, the acquisition of N pulses is realized at sample rate of 500 kS/s after the mixer stage with the support of software RTO-K11. The corresponding IQ data at 500 KS/s is then exported to Matlab to be analyzed. The transmission lines ($\pi_{measure2}$ and π_{out}; $\pi_{measure1}$,and π_{in}) are connected together by passive networks consisting of high power couplers, attenuators, power splitters, and RF cables, see Fig. 3.12. The calibration procedure is described as following:

- Step 1: To capture voltage waveforms at SSPA input and output reference planes, normalization must be performed to take into account for offset coefficients depending on the passive networks. A commercial vector network analyzer (N5221A) performs S-parameter measurements of the two-port passive networks. From these measurements, the offset coefficients are derived and used to correct values at (π_{in}, π_{out}). In this step, it is assumed that couplers offer high directivity and negligible mismatch uncertainty among individual components.
- Step 2: The phase offset between $\pi_{measure1}$ and $\pi_{measure2}$ is characterized with a through transmission between π_{in} and π_{out} from extracted IQ data.
- Step 3: Two power meters (N1912A) measure the average envelope power at the π_{in} input and π_{out} output planes as power calibration references.
- Step 4: A Matlab-based script executes the measurements of envelope amplitude and phase by extracting the IQ data and correcting with calibrated data from Step 1 to Step 3. Then, P2P stability normalization and calculations can be realized.

3.2.2 Simulation and measurement results discussion

The non-linear simulations are based on the circuit envelope (CE) method described in [147, 148]. In the CE method, the input waveforms are represented as RF carrier in frequency domain, with modulation envelopes in time do-
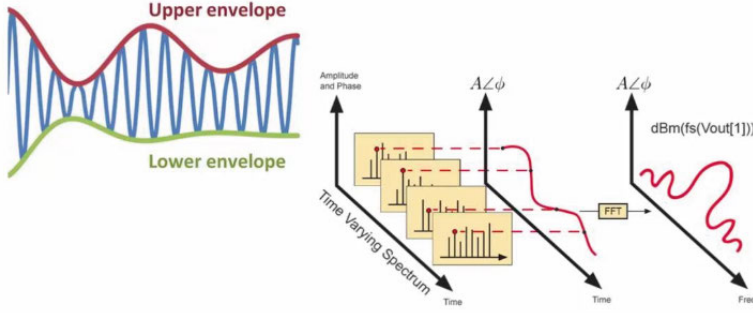
Figure 3.13. A modulated RF signal with its simulated time-varying spectrum in step-by-step simulation process. Adapted with permission from [149].

main. The CE method is a combination of harmonic balance and time-domain simulation techniques, see Fig. 3.13. First, a time-domain analysis is realized to sample the modulation envelope. Then at each time sample the circuit envelope simulator performs harmonic balance to compute a time-varying spectrum. Therefore, the method offers a greatly reduced computation for complete analysis of the modulated RF signals and P2P stability.

The simulated results are compared with the measured results in time domain for a single pulse. The design in [**Paper I**] includes an energy storage capacitor. This allows avoiding using a big power supply [138]. For the pulsed RF system in Fig. 3.1, the storage capacitors in a capacitor bank accumulate the energy during the silence of the pulse. The accumulated energy is then provided for amplification [**Paper I**] during the pulse. This leads to a very compact design solution for the system. As demonstrated in [**Paper II**], the design in [**Paper I**] exhibits a voltage droop due to the storage capacitor discharge. The voltage droop is caused by the equivalent series resistance (ESR) of the capacitor and the capacitor discharge. The energy storage capacitance is chosen as follows:

$$C = \frac{Ixdt}{dV} \qquad (3.7)$$

, where I = peak current, dt = pulse length, dV = pulse voltage drop.

Fig. 3.14 shows the measured voltage drop when the SSPA module delivers 1.25 kW output power. The drop is measured on the order of 1 V at the end of the pulse of 3.5 ms. Due to the voltage droop, it is observed that there is a droop of 0.2 dB corresponding to 4% reduction in amplitude. The measured drop agrees well with the simulation results, see Fig. 3.15. This leads also to a drop of the insertion phase, which can be found in [121]. The use of storage capacitors is unavoidable in pulsed RF power amplifiers. For pulsed particle accelerator systems, the inherent drop results in the charged particles' instabilities during acceleration. A control strategy is adopted using LLRF controller allowing for compensating the inherent drop. The details regarding the LLRF
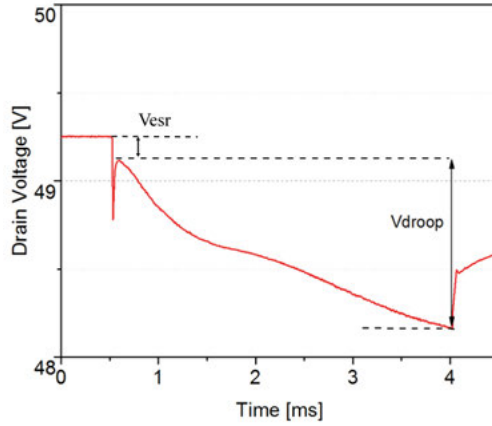
Figure 3.14. Measured result of drain voltage at 1.25 kW output power. Adapted with permission from [**Paper II**] [121].
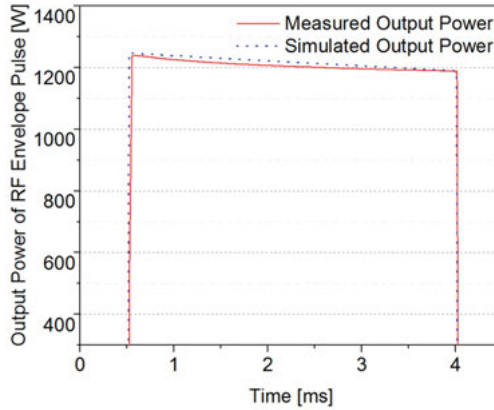

Figure 3.15. A drop of amplitude within the pulse in time domain at 1.25 kW output power. Reprinted with permission from [**Paper II**] [121]. Copyright (2018) Wiley.

controller and implementation of the control strategy will be discussed in section 3.4. The lifespan of storage capacitors is degraded due to current ripple, over-heating caused by the ESR, applied voltages beyond the rated voltage of the capacitors, etc. Therefore, it is important to consider all of the factors that can accelerate the failure rate of the storage capacitors in the pulsed power generation systems for particle accelerators. In the section 3.4, some practical considerations regarding selection of storage capacitors will be discussed.

As mentioned, P2P stability is of prime importance in power generation systems. Power amplifiers might adversely affect stability. Therefore, precise stability measurements of such amplifiers is paramount in order to maximize the overall stability of the whole system. The P2P stability is calculated by using a regular and repetitive sequence of the pulse-modulated RF carrier with iden-
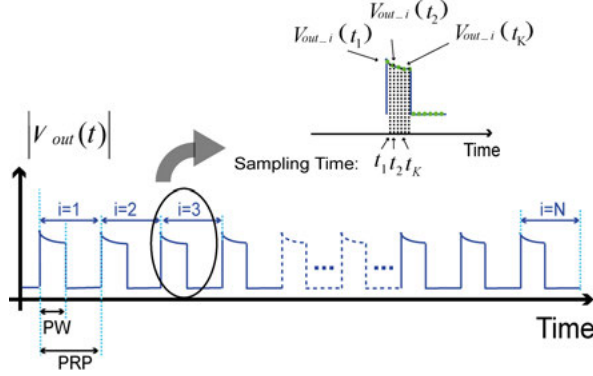
Figure 3.16. The envelope diagram of the RF pulsed signal with arbitrary pulse width (PW) and repetition rate period (PRP). Reprinted with permission from [**Paper II**] [121].Copyright (2018) Wiley.
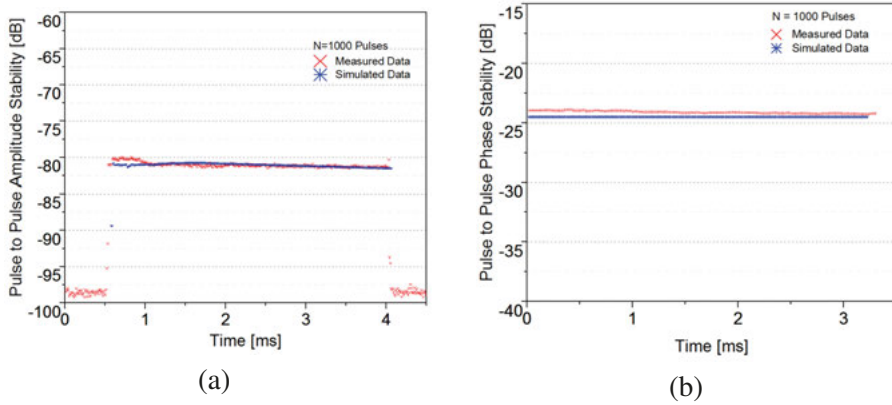

| (a) | (b) |

Figure 3.17. Measured results of amplitude and phase stability using time-domain envelope measurement [**Paper II**]. Reprinted with permission from [121]. Copyright (2018) Wiley.

tical pulse widths and identical pulse repetition periods of the envelope [139]. In this thesis, the P2P stability is characterized by using the time-domain envelope measurement setup [**Paper II**]. From envelope diagram of the RF pulsed signal in Fig. 3.16, the values for the stability can be given as follows:

$$\overline{Stab(t_k)} = 10 \times \log \left[\frac{1}{N} \sum_{i=1}^{N} \left(V_{out\_i}(t_k) - \overline{V_{out(t_k)}} \right)^2 \right] \qquad (3.8)$$

$$\overline{V_{out(t_k)}} = \frac{1}{N} \sum_{i=1}^{N} V_{out\_i}(t_k) \qquad (3.9)$$

where the index i refers to the i_{th} pulse in the sequence. The value V_{out_i} can be either amplitude or phase at sampling points of given N pulses in

case of amplitude stability or phase stability measurements. In this thesis, the time-domain envelope measurements of amplitude and phase P2P stability are performed under periodic RF pulses without silence. The P2P stability in amplitude and phase are obtained on the order of -80 dB and -24 dB. This is because non-linear distortions (thermal effects) are similar from pulse to pulse, see Fig. 3.17. In addition to stability measurements, simulations on amplitude and phase stability are performed by using circuit envelope method. To evaluate how attributable the design [**Paper I**] is on overall stability, an input signal is applied with uniform distribution of amplitude. Then the envelope simulator runs Monte Carlo analysis to obtain P2P variability in amplitude and phase at the output, see Fig. 3.17. The simulated results match well to the measured results at 1.25 kW output power. By using the envelope simulation presented in [**Paper II**], it is possible to use the non-linear model for the transistor in order to predict P2P stability performances. This allows for early insights on acceptable levels of amplitude and phase on critical components such as power amplifiers, which specifies by the tolerance of amplitude and phase of particle accelerators, i.e. for ESS requirements of 0.1% in amplitude and 0.5^o in phase. The achieved results give the upper limits for the LLRF controller, to regulate its amplitude and phase errors.

3.3 High power combiner approach

As can be seen in the combining architecture described in Fig. 3.1, the low-power amplifier modules are combined in a way to achieve the output power levels with the best efficiency performance. For solid-state based power generation systems, the system efficiency is determined by the mismatch in amplitude and phase among power amplifier modules, loss of the combiner, number of failure modules, output matching of the combiner, and number of combining modules [58, 150–152]. The mismatch among amplifier modules will be discussed in the section 3.4. This section presents several engineering solutions [**Paper III and Paper IV**] allowing for the realization of the power summation of individual PA modules with improved efficiency and high power handling capability. Power combiners are mostly based on quarter-wavelength structure such as: Wilkinson [153], Gysel [154], coupled-line [155], rat-race ring [156], etc. The combining stage might include single or multiple stages from low power to high power, see Fig. 3.18. The combiner is designed in planar technology [99, 157] or is waveguide-based structure [158–160], depending on the demand and power-handling levels. In this thesis, two engineering solutions are adopted for power summation of individual modules. The first design [**Paper III**] is based on a conventional Gysel configuration using shield strip-lines in order to improve the power handling capability. The other [**Paper IV**] combiner design uses re-entrant cavity structure, with 12 inputs.
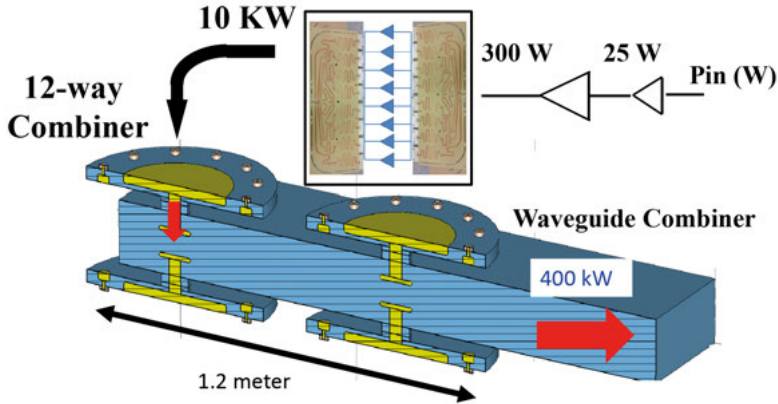
Figure 3.18. A picture of combining architecture for a conceptual design of solid-state 400-kW system. The combining stage consists of 3 stages including Gysel-type combiner for 10 kW level, cavity-based combiner for 100 kW level, and waveguide-based combiner for 400 kW level. Reprinted with permission from [**Paper VI**].

3.3.1 Low and mid range power combining solution

For high power applications, Gysel-based structure [154] has widely been used. The Gysel type structure offers the use of external isolation loads, monitoring capability of tolerances among input ports, and is an easy-to-implement geometry. The use of external high-power isolating loads makes the Gysel-based structure far better in comparison to the Wilkinson structure. A stacked arrangement, implemented on planar technology, leads to a very compact assembly at very high frequency (VHF) or ultra high frequency (UHF) range [99, 161]. However, it can be demonstrated that such Gysel combiner is not suitable for a large number of inputs, i.e. more than 10 inputs due to the floating common star point. This explains why Gysel is chosen in this thesis for combining a sub-block of 8 inputs allowing to achieve 10 kW output power [**Paper V**]. For higher power levels, the cavity and radial design approach are preferred [158, 160, 162–164] due to the availability of more inputs.

In **Paper III**, a Gysel-based combiner is adopted employing shielded strip-line techniques [165–167] with an air gap above and below the strip-line. The power handling capability of this configuration depends on the breakdown voltage of strip-lines and connectors. As can be seen in Fig. 3.19b, the spacing between copper traces (in yellow) and ground planes (lower and upper plates) are supported and held by fixed spacers. The traces are in conjunction with associated ground planes and define the suspended striplines. This allows for high power operation with inherent ventilation capability. For shielded strip-lines, the impedance can be optimized by adjusting the width of the traces and the spacing between the strip-lines and ground planes. In the assembly, spacing is 17.5 mm, the thickness of copper plates is 1.5 mm to handle the
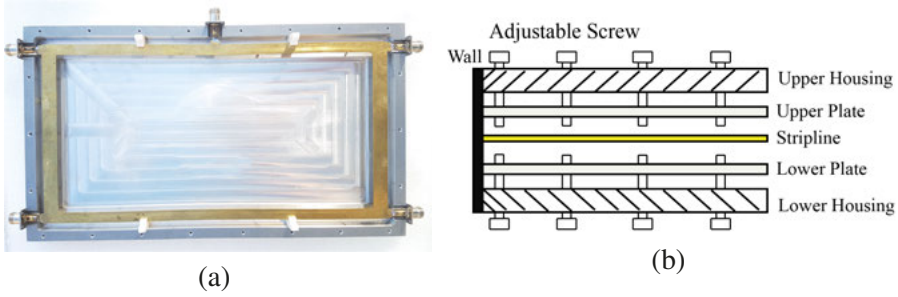
Figure 3.19. (a) The fabricated Gysel-based combiner. (b) A cross section of the strip-line structure with the mechanical tuner above and below the strip metal traces. [**Paper III**]. Reprinted with permission from [170]. Copyright (2018) IET.

temperature rise of strip conductor at high power levels [168]. The width of characteristic impedance is then deduced using Cohn's approximation [169] as following:

$$Z = \frac{94.15}{\sqrt{\varepsilon_r}\left(\frac{W/H}{1-t/H} + \frac{C'_f}{0.0885\varepsilon_r}\right)}\Omega \qquad (3.10)$$

where C'_f is the fringing capacitance in μF per centimetre, which is evaluated from one corner of the strip to the adjacent ground plane; $\varepsilon_r = 1$ is used as the relative dielectric constant of air; H is the plate spacing; W and t are the width and thickness dimensions of the transmission lines. Each of input/output ports includes a N-type connector mounted on strip plates with respective stepped matching networks. Dimension details of the combiner can be found in [**Paper III**]. It might happen that the impedance is not set to an optimal value due to imperfect balance between ground planes. A mechanical tuner is provided including upper and lower aluminum plates that are made adjustable, see Fig. 3.19b.

The design is validated and characterized at the frequency of interest i.e. 352 MHz. S-parameter measurements are performed at low power, see Fig. 3.20. The simulated results agree well with the measured results. It is shown that the combining approach offers low insertion loss of only 0.1 dB, good return loss, high isolation of more than 30 dB, and superior phase imbalance among ports. High power measurements are performed at an output power of 22 kW with 5% duty cycle, see Fig. 3.20. Several long hours of operation showed no detection of sudden heating, degradation in performance, or arcing. The temperature of the combiner stabilizes at 27.5^o C. The high power measurement results are comparable with low power results.

The Gysel combining solution using strip-line technique [**Paper III**] is implemented and validated at ESS frequency of interest. It is here demonstrated that the solution can be adopted for mid-range power combining stages up to few dozens of kilowatts. For solid-state based power generation systems, this
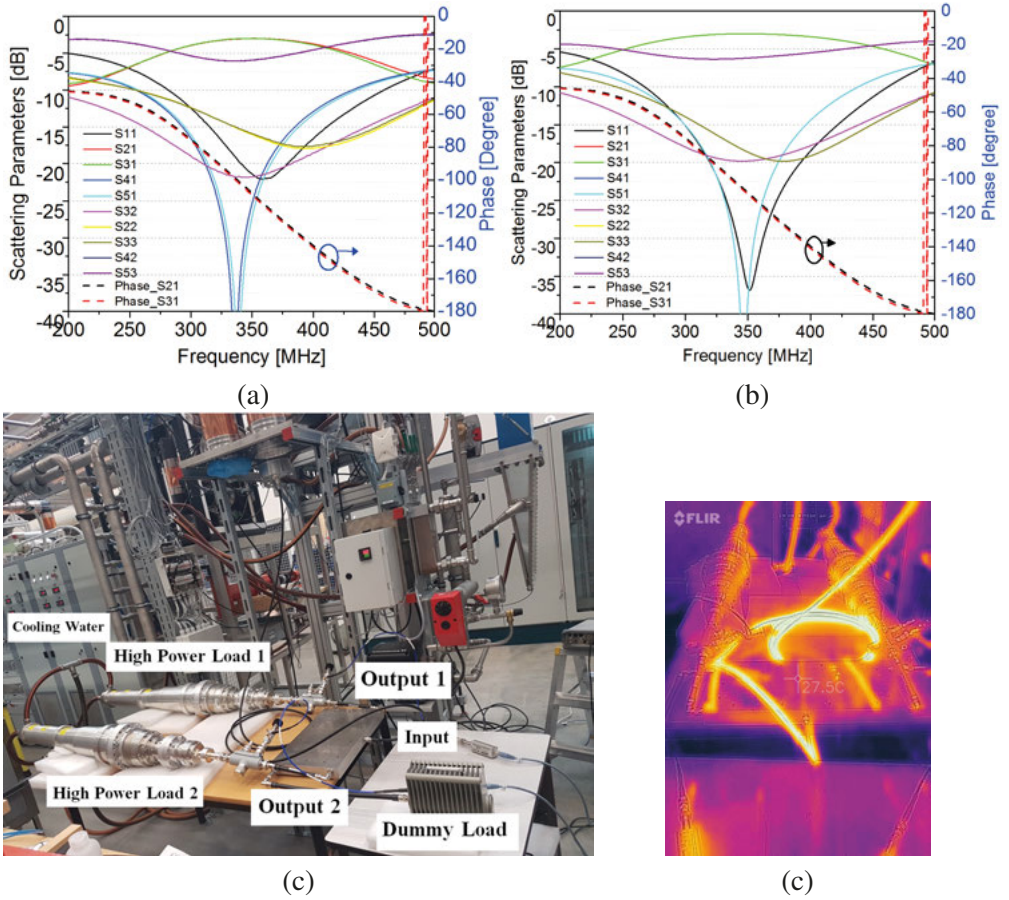
Figure 3.20. A comparison between simulated results and measured results (top). A picture of high power tests and monitoring with infrared camera (bottom). Reprinted with permission from [**Paper III**] [170]. Copyright (2018) IET.

solution unlocks a new way of designing power combiners, with improved power handling capability with good performance in insertion loss, isolation, and return loss. To reduce the footprint of the design as well as the whole system at low frequency, meander lines [171] and/or stacked arrangement [161] are adopted. The 2-way combiner at high power presented in this thesis is a very good example for facilitating Gysel multi-port combiner design, see Fig. 3.21

3.3.2 High power combiner

The use of strip-lines allows reducing the size of the design but the power handling capability is limited below 100 kW. Cavity-based approach brings advantages of a multi-port design in combination with high power handling
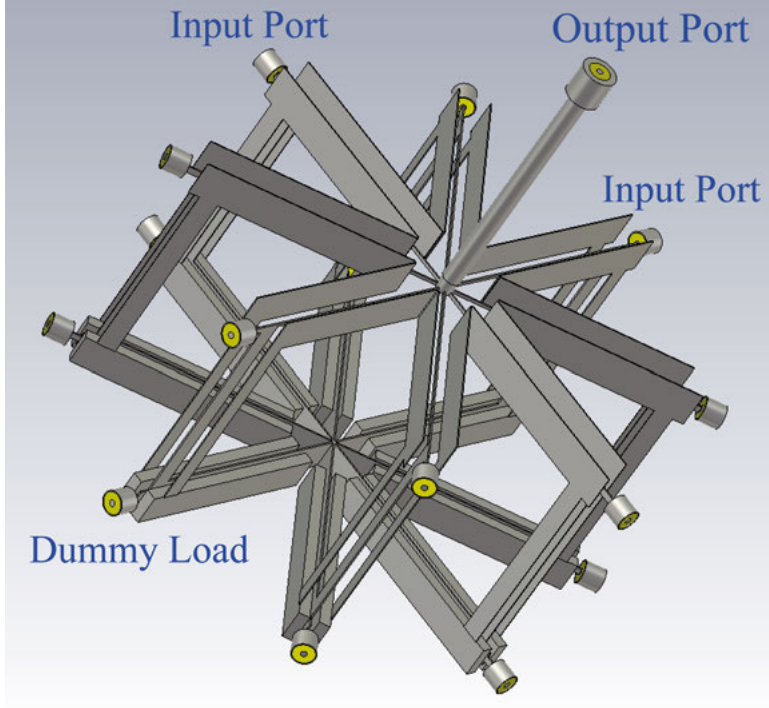
Figure 3.21. A design of 8-port Gysel combiner is realized in CST design platform.

capability up to hundreds of kilowatts. In the conceptual design Fig. 3.18, the cavity combiner [**Paper IV**] is used to combine 12 sub-blocks of 10 kW [**Paper V**]. The presented combiner consists of three sections: 1) the re-entrant cavity resonator [172, 173]; 2) the door-know type couplers [174] at inputs; 3) the output port whose post is combined with the ridge at the bottom of the re-entrant cylindrical cavity forming a doorknob geometry, see Fig. 3.22. The input ports are 7/16" flange-mount connectors screwed to input doorknob couplers, whereas the upper plate of the combiner embodies a 3-1/8" flange at the output. High-power connectors allow for an enhancement of power handling capability at inputs and output [175]. To start it off, the re-entrant cavity is equivalently treated as a shorted coaxial line terminated by a capacitor. The small spacing corresponds to the capacitor formed by parallel plates, whereas the other parts of the cavity can be modeled as a coaxial line, see Fig. 3.22. Assuming that the resonant wavelength is much greater than the dimensions of the cavity, the cavity then can be analyzed in a quasi-static approximation. The resonant condition of the cavity is given below:

$$Z_r = Z_o \frac{Z_C + jZ_o \tan \beta_o H}{Z_o + jZ_C \tan \beta_o H} = 0 \qquad (3.11)$$
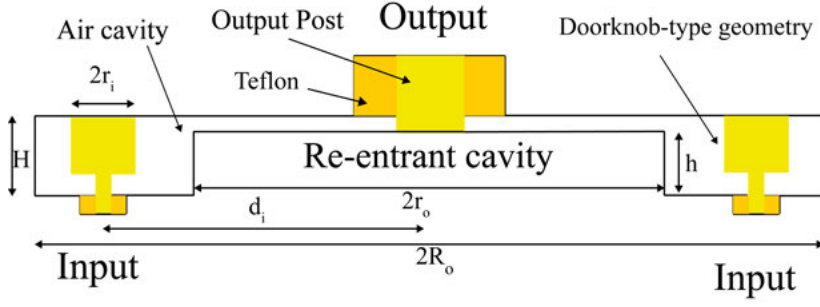
Figure 3.22. Cross section of cavity-based combiner [**Paper IV**] with doorknob-type geometry at inputs and output.
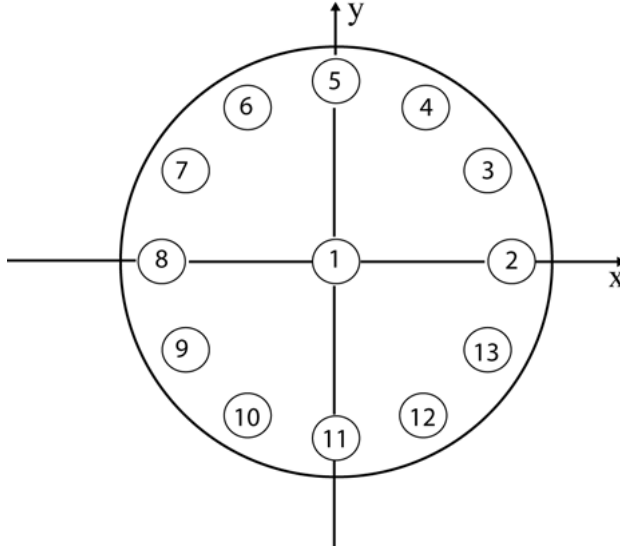
Figure 3.23. Numbering of the ports of a 12-way combiner in [**Paper IV**].

From the Eq. 3.11, the resonant condition is then given as:

$$jZ_o \tan \beta_o H + \frac{1}{j\omega_o C} = 0 \qquad (3.12)$$

in which $\beta_o = \frac{2\pi}{\lambda_o} = \omega_o \sqrt{\mu_o \varepsilon_o}$ is the propagating constant at the resonant frequency; the gap capacitance $C = \frac{\varepsilon_o \pi r^2}{(H-h)}$

The characteristic impedance of coaxial line can be represented as in [158]:

$$Z_o = \frac{1}{2\pi} \sqrt{\frac{\mu_o}{\varepsilon_o}} \ln \frac{R}{r} \qquad (3.13)$$

From Eq. 3.12, , the resonance wavelength can be derived as:

$$\lambda_r = \sqrt{\frac{4\pi^2 r^2 H}{2(H-h)} \ln\left(\frac{R}{r}\right)} = 2\pi r \sqrt{\frac{R}{2(1-\frac{h}{H})R/r} \ln\left(\frac{R}{r}\right)} \qquad (3.14)$$

Values of R, r, H, h then are chosen for resonant frequency of 352 MHz. In the next step, it is necessary to realize the critical matching for the combiner's inputs and output by employing coaxial-to-waveguide junctions. The matching junctions transform the TE10 mode transmitted by the wave-guide to the TEM mode transmitted by the coaxial line [176, 177]. Doorknob-type structure are adopted for such junctions, in which the inner conductor of the coaxial line is connected to a doorknob structure on the other side of the wave-guide, see Fig. 3.22. The doorknob type geometry allows improved high power carrying capability of the coaxial-to-wave-guide junction up to the limit breakdown point which is imposed by the breakdown voltage of the coaxial line [178]. It is found that the inductance of the output coupler is equivalent to one half of the inductance of the input coupler L_i. The inductance of input coupler L_i can be approximated by considering the input coupler in combination with the walls of the cavity and adjacent couplers as a coaxial line with inner radius r_i and outer radius (R-d). The inductance then can be written as following [179]:

$$L_i = \frac{\mu_o H}{\pi} \ln \frac{R-d_i}{r_o} \qquad (3.15)$$

The output inductance L can be given as:

$$L_o = \frac{\mu_o H}{\pi} \ln \frac{R}{r_o} \qquad (3.16)$$

From Eq. 3.15 and Eq. 3.16, one can find an approximation for the optimal distance d_i as a function of the cavity's parameters and the input coupler radius:

$$d_i = R - r_i \left(\frac{R}{r_o}\right)^2 \qquad (3.17)$$

Values of the combiner's parameters are chosen following Eq. 3.14 and Eq. 3.17. The chosen design parameters are then simulated numerically using the CST studio. The details of dimensions can be found in [Paper IV] [180].

Simulation of the electric field for an input power of 1 W is shown in Fig. 3.24. For 100 kW output signal, the peak electric field can be predicted on the order of 0.38 MV/m, which is 7 times smaller than the breakdown field strength of dry air 2.9 MV/m [181, 182]. The maximum predicted power handling capability of the proposed combiner is superior than other radial combiners i.e [158] with E-field strength of 3 kV/m at 0.05 W output signal, which would suffer electrical breakdown upon output power of 50 kW. S-parameter simulated and low-power measured results can be found in [**Paper IV**] [180].
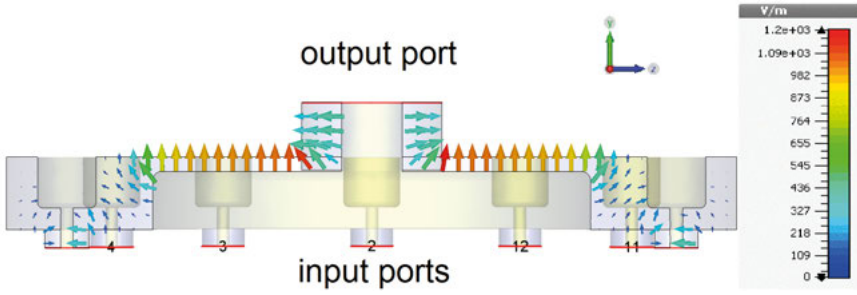
Figure 3.24. Simulated result of electric field pattern with 1 W of output power. Adapted with permission from [**Paper IV**]. Copyright (IEEE) 2018.
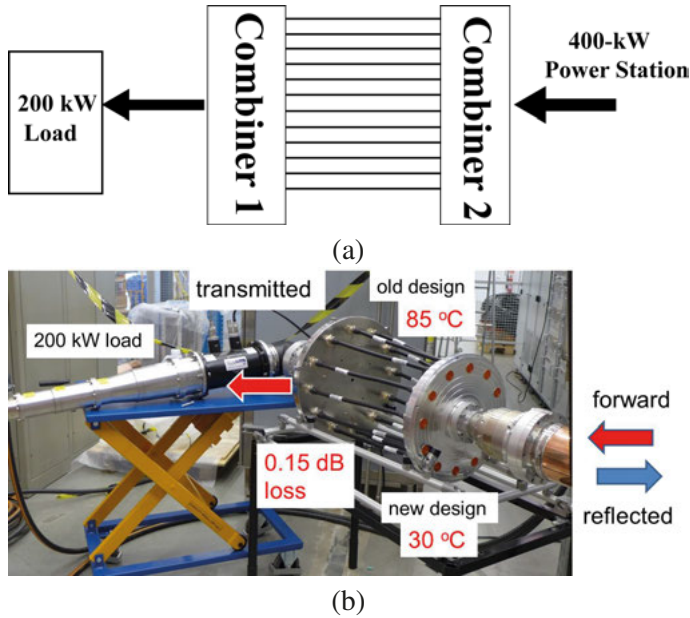

(a)

(b)

Figure 3.25. A picture of measurement setup for high power characterization of the combiner [**Paper IV**]. Combiners in [160] and [180] are referred as combiner 1 and combiner 2, respectively. Adapted with permission from [180]. Copyright (IEEE) 2018.

To validate the very power handling capabilities, a high power characterization of the combiner is performed by connecting two combiners [160, 180] in a back-to-back configuration, see Fig. 3.25. The test bench is powered by a Tetrode-based 400-kW power station from Electrosys [183] at 352 MHz with 5% duty cycle. For the output of the test bench in Fig. 3.25, a 200-kW load with water-cooled system is added. The high power characterization is limited to this power level due to the use of the 200 kW load,. The combiner exhibits an excellent performance with insertion loss of 0.15 dB, which is on the order of 0.2% as demonstrated at 200 kW level. In addition, the amplitude and phase
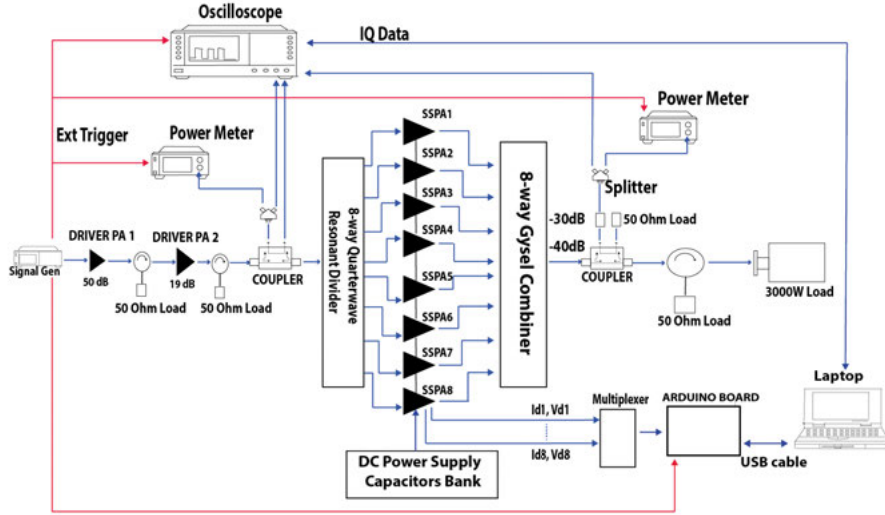
Figure 3.26. A block diagram of the sub-block 10-kW amplifiers with time-domain measurement setup. Adapted with permission from [**Paper V**].

imbalances among the ports are 0.1% and 0.036^o, respectively. It is concluded that the proposed combiner is well-suited to be used as a second combination stage (i.e. in Fig. 3.18 the combiner carries 12 sub-blocks of 10 kW to realize power combination of 120 kW.) that is required for power capability up to 400 kWs.

3.4 Integration of solid-state high power generation for particle accelerators

Integration process consists of two parts: system design and system-level characterization. In the system-level characterization procedure, the system [**Paper V**] is fully characterized under ESS specifications [8] using the time-domain setup described in [**Paper II**].

3.4.1 Integration of sub-block 10 kW amplifiers

The conceptual 400 kW system (i.e. in Fig. 3.18) is based on a number of sub-blocks of 10 kW amplifier system [**Paper V**]. Fig. 3.26 shows the block diagram of the 10-kW sub-block. Each of the modules delivers more than 1 kW output power at the frequency of interest, allowing for minimizing the number of ports to achieve 10 kW, thus, reducing the complexity of the combining topology. The 10-kW system is modular and it consists of 8 individual amplifier modules [**Paper I**]. The construction is integrated in a standardized
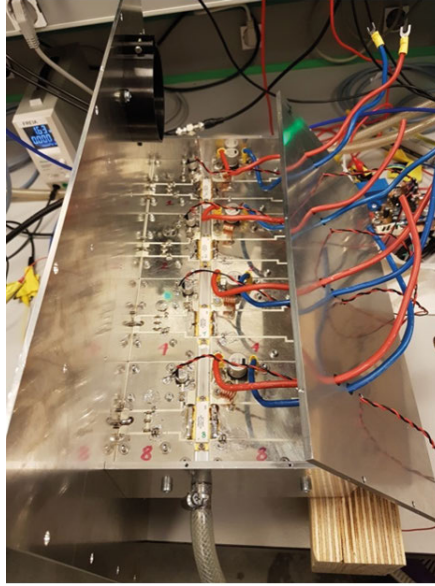
Figure 3.27. A picture of 10 kw system housed in 19-inch 3U rack with 4 modules on the top and 4 modules at the bottom. Reprinted with permission from [**Paper V**]

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19-inch 3U rack around a water-cooled heatsink in which 4 of modules are on the top and 4 of modules are at the bottom. The cooling system used for the 10-kW system includes a cold aluminum plate and a water cooling pipe inserted in the middle of the plate, for thermal dissipation. The water inlet temperature is kept around 30° C with minimum water flow of 15 l/min. A power supply (EA-PS 9063-90 from Elektro-Automatik) with high efficiency provides the DC power to the amplifiers using a capacitor bank as mentioned in section 3.2. The capacitor bank is composed of eight of 68-mF capacitors to store energy within the pulse, one capacitor for each of the associated modules [**Paper I**] [8]. In addition, current breakers are used to implement measurements of the graceful degradation [162] by switching off DC power supply applied to a certain number of associated modules. DC power consumption of the amplifier modules are monitored, as described in [**Paper II**]. All of the collected data is then analyzed for system efficiency calculations. Calibration process of voltage and current sensors is required for an improved accuracy. The test bench shown in Fig. 3.26, has a driver amplifier, a two-stage amplifier including a linear amplifier (ZHL100W-52+) from Mini-circuits. The output from the driver stage is splitted by a quarter-wavelength divider, which is required to operate at about 200 W. The 1:8 divider distributes the RF signal to each of the amplifier modules. To produce 10 kW of output power, an 8:1 combiner is used to combine the output signals from the amplifier modules. The combiner [99] is based on Gysel configuration [154]. Challenges
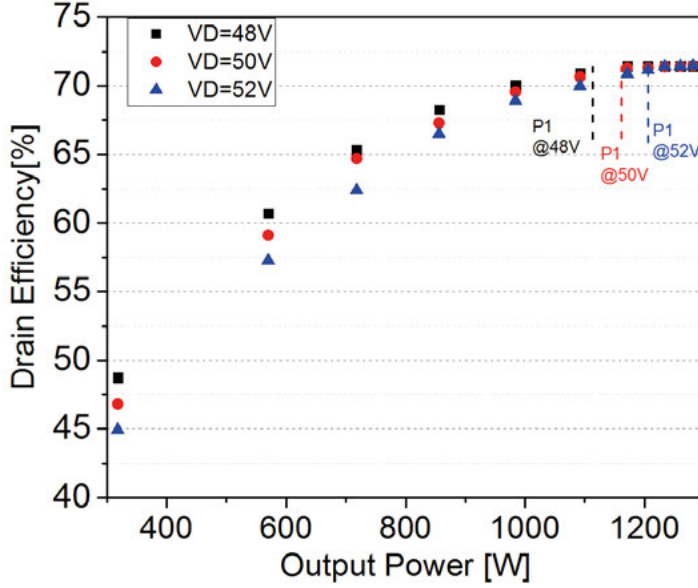
Figure 3.28. Drain efficiency of amplifier module [**Paper I**] at several drain voltages.

related to the microstrip technology integration with stack arrangement are solved with a stack arrangement, as reported in [99]. The stack arrangement results in a high degree of compactness despite the 352 MHz frequency with a quite long wavelength. In the layered approach, issues related to the ventilation capabilities are settled by using cut-out slots carried on layer-to-layer boards. Board-to-board coupling can cause a degradation of the combiner's performance, even worst in the stacked approach. To reduce the mutual coupling among boards, stubs are added in the common layer of the combiner and are located $\frac{\lambda}{8}$ from the floating common point. The full design of the divider/combiner is further described in [**Paper V**].

Integration is a sequential step-by-step process. Firstly, every single component of the system is validated to make sure that it meets key performance objectives, depending upon the stage where it is located, i.e. footprint, harmonic levels, required output power levels, noise, insertion loss, stability, etc. In this section, the integration process is realized in three stages: driver stage, dividing/combining stage, and amplifier stage.

An amplifier stage:

The first step is to realize the mechanical mounting of transistors to heat-sink. Steps should be taken to avoid any burn-out during high power operation, as follows:

- All holes are clear screw fastener with 3 mm in diameter. A lock washer should also be used.

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- It is recommended to keep mounting surface flat for the matching boards at the input and output.
- At the bottom of the active device, a thin layer of thermal compound is used with no more than a thickness of 0.03 mm.

The second step is to realize the electrical connections following the steps below:

- Applying 50 V from power supply EA-PS9063-90 to the capacitor bank. Supply cables are twisted using ferrite beads to diminish mutual interferences. All of amplifier modules can be operated between 48 V to up to 52 V, see Fig. 3.28, however, the modules are optimized for 50 V at 1250 W.
- All units are set to 40 mA quiescent current per transistor (2 transistors in each package) at drain voltage of 50 V. The monitoring boards [**Paper II**] including the bias circuitry provides the gate bias voltage to the modules. Note that the bias point of 80 mA offers the best compromise between efficiency and gain.
- By-pass capacitors should be chosen properly at DC voltages to avoid spurs and instability during the operation of the modules.

The 3rd step is to characterize the imbalance in power and phase shift among the modules followed by a tuning procedure, allowing to keep variations within reasonable limits, i.e. 0.5 dB in amplitude and 5° in phase, to reduce combining loss [58, 151]. The tuning procedure is realized at both input and output matching networks. Due to manufacturing tolerance of active devices, passive components, tuning procedure implemented at each of amplifier modules [**Paper I**] is varied, though the steps are similar. Depending upon the number of input ports, the tuning procedure can be relaxed to some degree as demonstrated in [58] i.e. $\pm 5^o$ in phase and ± 0.5 dB in amplitude among the 16 amplifier modules [184]. The use of 8 amplifier modules in the 10 kW subblock requires a more stringent tuning process with limits of amplitude and phase variations on the order of ± 0.25 dB and $\pm 2.5^o$, respectively. As mentioned at step 2, the tuning procedure is optimized for 50 V at 1250 W output power. Details of the tuning procedure at each of the amplifier modules can be found in Table 3.1. The current consumption is varied when moving the matching capacitor closer or further from the transistor. Initially, the distance between output matching capacitors and active device of all amplifier modules is in the order of 1.6 cm. During the tuning process, trade-offs are made among the return loss, output power, and efficiency. Depending on the trade-offs, the distance is adjusted, see Table 3.1. The tuning process includes:

- *Step 1:* Adjusting gate voltage bias and measuring the quiescent current.
- *Step 2:* Evaluating the performance of amplifier module regarding output power, current consumption, gain, efficiency using the time domain measurement setup [**Paper II**].
- *Step 3:* Realizing tuning procedure.
- *Step 4:* Return to step 2.

Module		Tuning procedure
1	$V_g = 1.58\ V$ $I_{dq} = 86\ mA$	Use of 10 pF + 8.2 pF + 6.8 pF for input matching at C5. Use of 27 pF and displace 1.8 cm far from transistor for output matching
2	$V_g = 1.69\ V$ $I_{dq} = 88\ mA$	Use of 33 pF + 15 pF for input matching at C5. Use of 27 pF and displace 1.68 cm far from transistor for output matching
3	$V_g = 1.57\ V$ $I_{dq} = 88\ mA$	Use of 33 pF + 10 pF + 3.7 pF for input matching at C5. Use of 27 pF and displace 1.6 cm far from transistor for output matching
4	$V_g = 1.57\ V$ $I_{dq} = 88\ mA$	Use of 33 pF + 15 pF + 1 pF for input matching at C5. Use of 27 pF and displace 1.4 cm far from transistor for output matching
5	$V_g = 1.58\ V$ $I_{dq} = 85\ mA$	Use of 33 pF + 8.2 pF + 6.8 pF for input matching at C5. Use of 27 pF and displace 1.75 cm far from transistor for output matching
6	$V_g = 1.58\ V$ $I_{dq} = 84\ mA$	Use of 33 pF + 10 pF for input matching at C5. Use of 27 pF and displace 1.95 cm far from transistor for output matching
7	$V_g = 1.59\ V$ $I_{dq} = 85\ mA$	Use of 33 pF + 10 pF for input matching at C5. Use of 27 pF and displace 1.75 cm far from transistor for output matching
8	$V_g = 1.63\ V$ $I_{dq} = 86\ mA$	Use of 33 pF + 12 pF for input matching at C5. Use of 27 pF and displace 1.55 cm far from transistor for output matching

Table 3.1. *Tuning procedure for each of the eight amplifier modules. The tuning procedure is included and consists in adjusting: gate voltage and input/output matching tuning.*
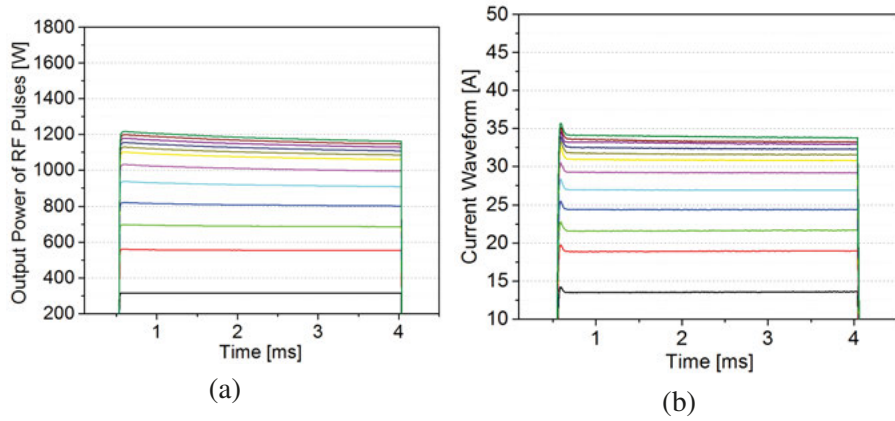
Figure 3.29. Measurement results of one amplifier module during the tuning procedure. Output envelope of the RF pulse (left) and current waveform (right).
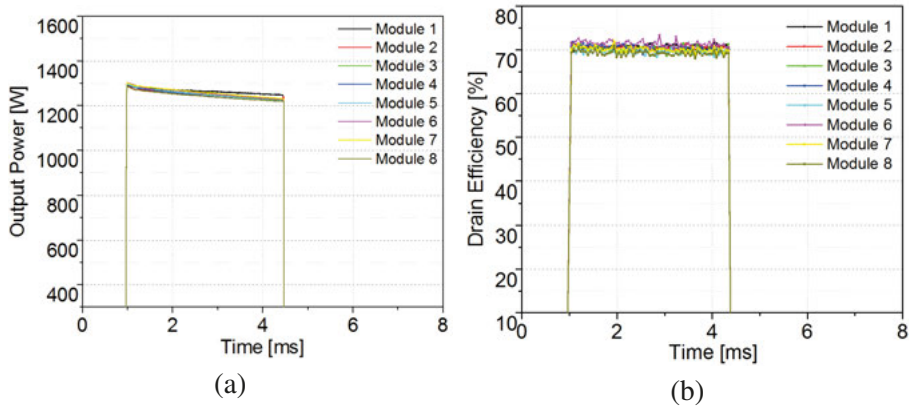

Figure 3.30. Optimal output waveform and drain efficiency waveform in time domain with different amplifier modules at 1250 W. Reprinted with permission from [**Paper V**].

- *Step 5:* Assessing the tuned performance with the requirements of input return loss, output return loss, output power and efficiency.

The tuning procedure for one module with several power levels is shown in Fig. 3.29. Insights of time domain measurement results with all of 8 amplifier modules can be seen in [**Paper V**]. All of amplifiers are optimally tuned to deliver 1.25 kW average output power along with more than 70% in efficiency within the pulse. The droop, caused by the capacitor bank, is in the order of 0.25 dB for all of modules [**Paper V**], see Fig. 3.30.

The combining stage:

The goal is to realize the power summation of the individual modules in order to achieve the targeted output power with minimum degradation in the combining efficiency. Output loss is a figure-of-merit allowing the characterization of the combining efficiency. Such loss is influenced by combiner

topology, amplifier characteristics, device failures, and S-parameters of combiner structure [58]. For the combining stage of the presented 10 kW system, some considerations must be taken, as follows:

- The combiner structure should offer low insertion loss, matching at input and output ports along with a good power handling capability.
- The failure of a module causes a reduction in the output power proportional to $(1 - \frac{k}{N})^2$ in which $\frac{k}{N}$ is the fraction of failed devices [58]. A good combining structure means a good isolation among the ports to avoid any degradation once a failure happens.
- When choosing combiner structure, reliability is an important factor to consider. The reliability at the combining stage should be far beyond as compared to the reliability at the amplifier stage and at the driver stage.
- Connectors at combiner terminations should be capable of carrying high power even in case of mismatch. Interconnection losses between connectors and transmission lines should be minimized i.e. in [**Paper II**] and [99].
- Design of the combiner should be of small footprint, cost effectiveness.

For the dividing stage of the 10 kW sub-block, the divider is required to distribute about 20 W to each amplifier modules. A quarter-wavelength coaxial configuration is chosen. The divider offers low insertion loss i.e. 0.05 dB, return loss of 25 dB, and isolation of 8.33 dB among the ports. Details can be found in [**Paper V**]. For the combining stage, the choice goes to a Gysel-based approach realized on planar technology with stack arrangement allowing for a reduced footprint. Reduced footprint results in an increase of the mutual coupling among transmission lines. This is also used to reason to degrade the balances among the ports in amplitude and phase. A tuning solution is investigated using coupling stubs in order to reduce the mutual coupling, thus, enhancing the isolation up to 20 dB and phase imbalance within 4°. The tuning procedure in the dividing/combining stage consists of the following steps:

- Choosing the topology of divider/combiner based on the targeted output power, power handling capability i.e, in the 10 kW, the number of PAs is fixed with 8 modules.
- Measuring divider/combiner's characteristics including: amplitude and phase imbalances, isolation, return loss.
- Depending on the phase variations among ports at the dividing/combining stage and the amplifier stages, each of the amplifiers is chosen to be connected to a suitable port at the combining stage to reduce any imbalances, see Table 3.2. Other solutions can be realized including: using variable-length cables or using gain/phase variable modules [185] at each of amplifier module. However, these solutions are complicated and costly and will not be covered in the scope of the thesis.

For the driving stage:

For the driving stage, it is very flexible to design the architecture of the stage. There is no restriction of how many stages it supposed to have, but it is

Divider Stage	Amplifier Stage	Combiner Stage
Port 2	Amplifier 1	Port 3
Port 3	Amplifier 2	Port 5
Port 4	Amplifier 3	Port 8
Port 5	Amplifier 4	Port 7
Port 8	Amplifier 5	Port 4
Port 7	Amplifier 6	Port 2
Port 6	Amplifier 7	Port 1
Port 1	Amplifier 8	Port 6

Table 3.2. *Inter-stage connections among components in 10 kW system for compensating imbalances.*
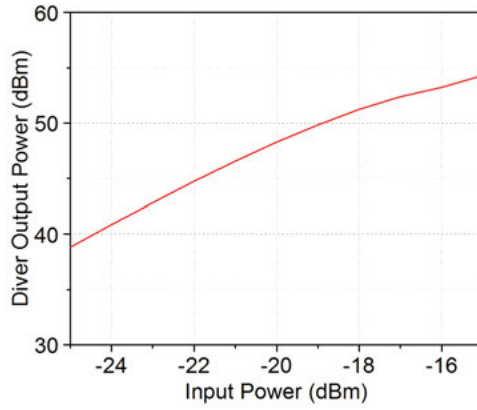
Figure 3.31. Characteristics of driver stage in the presented 10 kW system.

influenced by the input from the LLRF controller and output power needed for the dividing stage. Care should be taken for linearity at this stage. Linearity is an important factor for realizing the control loop, which will be presented in the following. The driving stage should also provide a margin of 10-15% in overhead power to compensate the losses of RF cables and circulator, as can be seen in Fig. 3.26.

3.4.2 System-level characterization

System-level characterization is realized in time domain once all of stages in the system are connected and tuned following the tuning process, previously described. Combining loss is a valuable figure-of-merit at the system-level characterization. The combining loss reflects how good the integration process could be. As can be seen in Fig. 3.32, there is a significant loss at the output of low power levels, which tends to diminish at the nominal output power delivering output power below 6 kW whereas the loss is minimized as
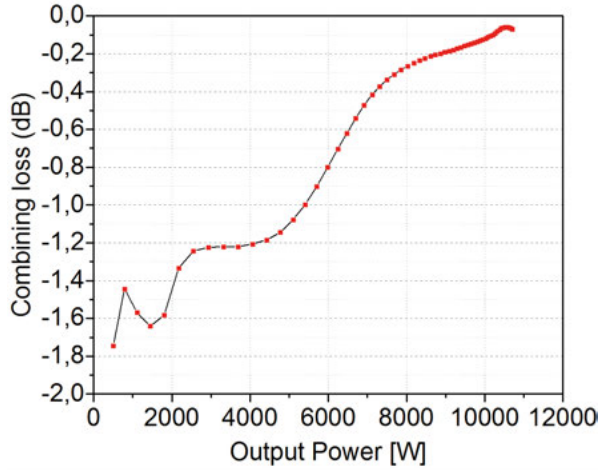
Figure 3.32. Combining loss of the 10 kW sub-block system. Reprinted with permission from [**Paper V**].

each of amplifier modules reach 1 kW.Since the imbalances in amplitude and phase among the modules are not optimized at such power levels. The overall combining loss at high power level is only on the order of 0.15 dB, equivalent to approximately a 3% loss in power. Due to the use of the storage capacitor bank, there is a drop at the output power envelope of the 10 kW sub-block, see Fig. 3.33. The drop is measured on the order of 1 kW within the pulse, which is equivalent to 0.36 dB. The drop within the pulse is due to the use of capacitor bank required in pulsed operation. The power drop causes instabilities in the linac which could lead to the acceleration of charged particles with inconsistent energies. We need to address this issue when developing solid-state amplifiers for particle accelerators operated in pulsed mode. A feedback control loop is realized allowing for stabilizing the amplitude and phase disturbances of the RF 10 kW system and compensating the drop caused by the capacitor bank. The control loop is implemented by an LLRF system developed at FREIA. Fig. 3.34 shows a block diagram of the proposed system. The control loop is based on Proportional-Integral (PI) controller implemented on the platform FlexRIO NI-5782 from National Instruments. More insights of the architecture can be found in [**Paper V**]. A reference signal is coupled to the output of 10 kW subblock system and is used as the reference signal of the control loop. The reference signal is then fed to the control loop. The implementation of the control loop includes the following procedure:

- Use LLRF to generate the RF pulsed signal at 352 MHz instead of using a vector signal generator. Calibration process is realized at this step.
- Open-loop testing with LLRF controller (no feedback) to evaluate the linearity of the system versus output power levels.
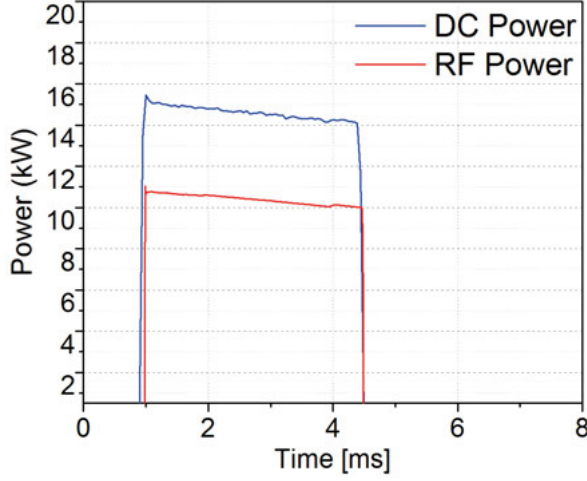
Figure 3.33. Output power and DC power waveforms at 10 kW power level. Reprinted with permission from [**Paper V**].
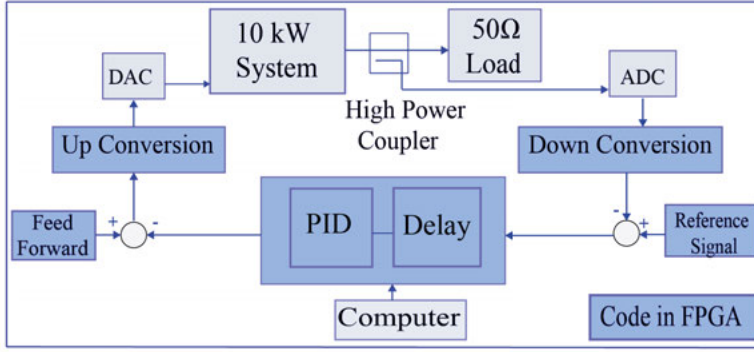

Figure 3.34. A block diagram of 10 kW system along with the feedback control loop. Reprinted with permission from [**Paper V**].

- Running the feedback loop in amplitude and phase at low power levels. Increasing power levels from low to 1 kW as to avoid any instability which could damage the amplifiers.
- Once the system works properly, the system-level is operated in several hours i.e. at least 4 hours and the RF 10 kW sub-block is characterized in operation.

3.4.3 Summary.

This thesis work developed in details the design, manufacturing and characterisation of a 10 kW solid-state amplifier starting from modules to the system integration. This work allows for a scale-up in power (i.e. targeting 400 kW)
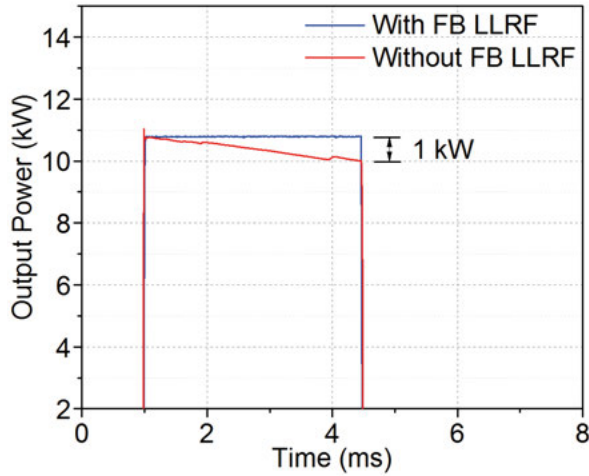
Figure 3.35. Measurement results of 10 kW system with compensated drop at the flat-top. Reprinted with permission from [**Paper V**].

to be used for next generation particle accelerators i.e. ESS superconducting cavities. Combining loss, pulse drop and stability are needed to characterize high power pulsed amplifiers using solid state technology. All of these need to be fully characterized using time-domain measurement setup in [**Paper II**]. A feedback loop [**Paper V**] addresses the pulse drop issue by using a PI-based control strategy in order to pre-distort the input signal for compensating the inherent droop caused by capacitor bank. In addition to pulse drop, the amplitude and phase stability also can be improved with the feedback loop. It is demonstrated that there is arcing, sudden heating, or degradation in performance of the 10 kW system during long hours of operation when delivering 10 kW output power. The system can be operated with 10-20% margin of output power in case of failure modules.

4. An experimental investigation of the optimal filling scheme for possible conceptual architectures of the 400 kW system.

This chapter discusses the scaling up in power of the conceptual design of 400 kW starting from the sub-block of a 10 kW power amplifier, as presented in Chapter 3. Fig.4.1 shows a system design of sub-blocks layer-over-layer assembly consisting of controller system, dividing/combining stage, capacitor bank, AC/DC power supply, and cooling system. Depending on the targeted output power, the choice of combiner topology and available power delivered by the modules are of paramount importance. The output from each of the sub-blocks is fed to a passive combining stage for realizing the power combination till 400 kW. In this chapter, several combining strategies will be discussed based on 10 kW amplifier sub-blocks. The strategies are described in [**Paper III**] and [**Paper IV**]. For all of these combining strategies, there is a demand of a distribution network which is based on a WR-2300 half-height wave-guide.
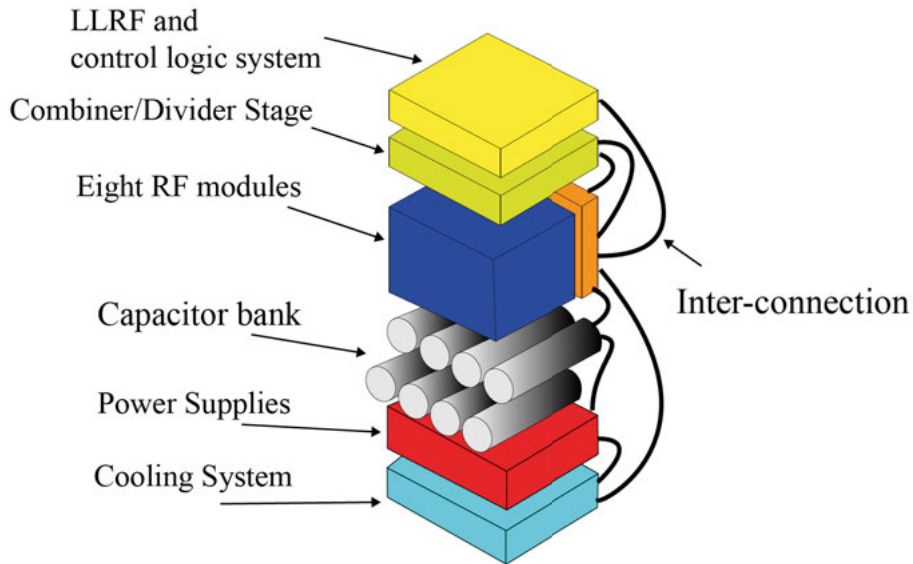

Figure 4.1. A block diagram of full sub-block design. A number of sub-blocks are used for combining 400 kW of output power.
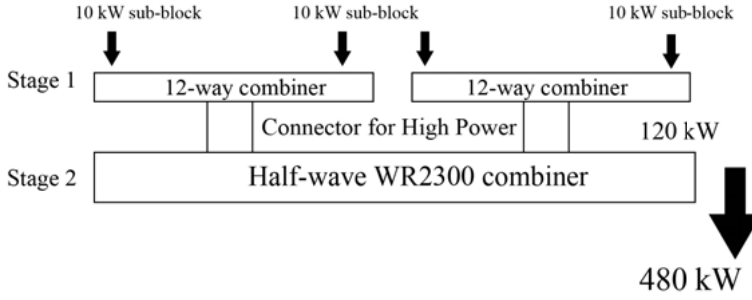
Figure 4.2. A schematic outline of the combining network I. Adapted with permission from [160].

The wave-guide-based system allows distributing high power to the cavities with low loss.

   In the second part of this chapter, we discuss the realization of an optimal charging scheme [13] using solid-state amplifiers. This scheme is demonstrated using an envelope tracking technique applied to a kW-level module. The proof-of-concept of this design is realized in [**Paper VI**]. In this paper, we demonstrate the feasibility of implementing the optimal charging scheme on solid-state amplifiers for the next generation particle accelerators using SC cavities in pulsed mode with minimized reflection, energy-saving operation up to 24% in total [**Paper VI**]. The experiment-based results shown in [**Paper VI**] unlock a new way to efficiently operate high power RF systems for next generation particle accelerators. In addition to merits of this scheme, a significant reduction of reflection power during filling time i.e. 400 kW in case of ESS superconducting cavities, is obtained. This allows for reducing the requirements of the sub-components i.e circulators for protection, the ruggedness of the PA modules, thus leads to cost-effectiveness, and reliable systems.

4.1 The possibilities of 400 kW conceptual designs using 10 kW sub-blocks and high-power combining solutions.

The core technology is the single-ended architecture and different combining strategies are demonstrated in Chapter 3. The demonstration of the power combination at 10 kW level allows foreseeing the possibility for scaling up in power of 400 kW. To realize this implementation, it is important to discuss the conceptual possibilities of the combining architectures and investigate advantages and disadvantages, thus discussing the best choice for a 400 kW solid-state based power station for the ESS accelerator facility.
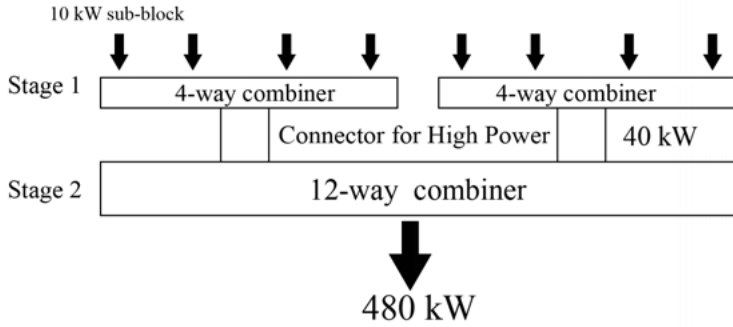
Figure 4.3. A schematic outline of the combining network II.

Combination strategy 1:

As can be seen in Fig. 4.2, 48 sub-blocks of 10 kW represent 384 kilowatt-level amplifier modules. There are four groups of amplifiers, each including 12 modules. The outputs are then fed to 12-way combiners in [**Paper IV**]. The following combining stage is based on half-wave-guide (WR2300) combiner. The high power combiner realizes power summation of 100 kW inputs allowing for delivering 400 kW output power. Coaxial 3-1/8" connectors are used for interconnecting combining stage 1 and stage 2. Details of design can be found in [**Paper VI**].

Advantages:
- Ultra high power carrying capability.
- A section of power transmission line for final power combining, i.e. WR2300 half-height wave-guide, could avoid the use of extra connectors and adapters.

Disadvantages:
- Large-size design.

Combination strategy II:

The second combining strategy makes use of two stages of combining, including: binary combiners and 12-way combiners in [**Paper IV**] for high power levels. The binary combiners adopt the strip-line technique described in [**Paper III**] for combining a group of 4 sub-blocks. The output of the binary stage is in the order of 40 kW. At the last stage, it is based on a wave-guide combiner, similar to the one introduced in the strategy 1. This configuration allows for the combination of 12 outputs from the binary stages, see Fig. 4.3. Coaxial 3-1/8" connectors are used for high power connecting stage 1 and stage 2. *Advantages:*
- Use of striplines makes the design more compact.
- Good isolation design.
- Advantages of Gysel-based configuration once mismatch happens.
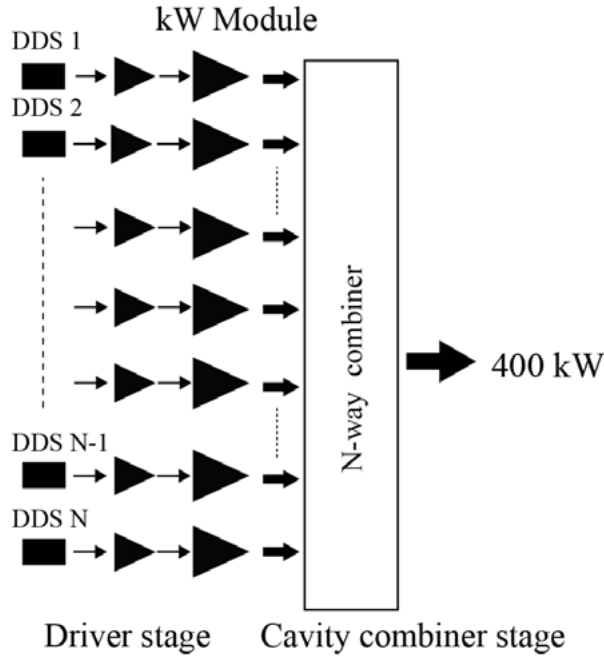- Tuning process is more accessible.

Figure 4.4. A schematic outline of the combining network 3 with resonant structures.

Disadvantages:
- External loads at the binary stages are needed. An associated cooling system for the loads should be included.
- High power transition between striplines and output connectors could cause losses and might be difficult to design.

Combination strategy III:

Cavity and radial combiners are becoming more and more available at accelerator facilities, i.e. at ESRF [111], CERN [186]. In the multi-port combiner designs, the number of the inputs can be extended up to dozens i.e. 144 inputs at CERN's cavity combiner design. In the combination strategy III, we consider the conceptual design of 400 kW using a 400:1 cavity combiner stage, 400 kW-level modules, and their associated driver amplifiers. This strategy allows to eliminate the use of the dividing stage, see in Fig. 4.4. Each of the 400 driver amplifiers is fed by a single direct digital synthesis (DDS) based module, allowing the generation of a digital signal. Each of 400 DDS-based modules is capable of adjusting amplitude, phase, and frequency. A synchronized clock interface is needed for the synchronization among i.e. the DDS-based signal generators or phase-locked loop for the synchronization of voltage-controlled oscillators. The cavity combiner in this configuration allows the capability of
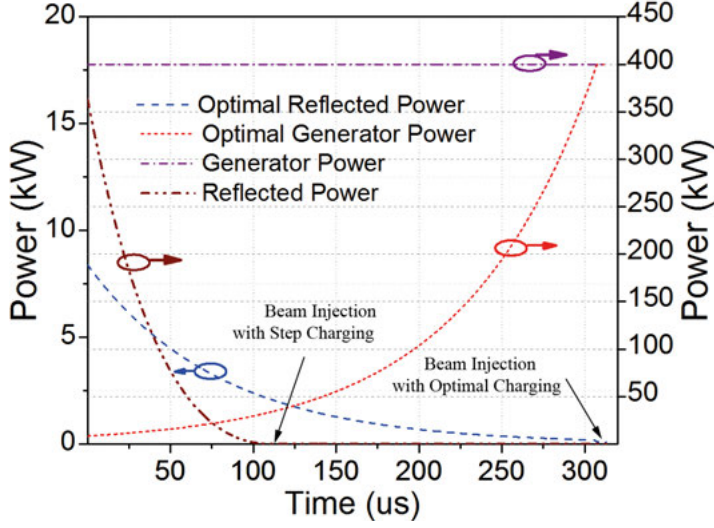
Figure 4.5. Pulse profile in time domain in case of conventional filling scheme and optimal filling scheme. Reprinted with permission from [**Paper VI**].

tuning at the input coupling ports by implementing movable coupling structures, as described in [111].

  Advantages:
  - The combination strategy allows implementing the optimized feeding power profile for operation with SC RF cavities.
  - This configuration is highly tunable and adaptive, thus it results in a highly efficient, reliable system that could self-adapt to unpredictable situations.

  Disadvantages:
  - The processor board used to control 400 DDS-based modules might be complicated.
  - The realization of the control strategies is challenging i.e. when controlling 400 modules as required at ESS facility.

4.2 Proof-of-concept kilowatt-level design system for optimal charging scheme.

The optimal charging scheme [13] allows significantly reducing power reflection when charging superconducting cavities as compared to the conventional step-filling scheme. For ESS spoke cavities [8], the wasted energy caused by full power reflection in the step filling process is estimated to be in the order of 30 MWh during long operation, i.e. 8000 hours. Estimates of the wasted energy are even worse for medium-β and high-β cavities at 150 MWhrs and
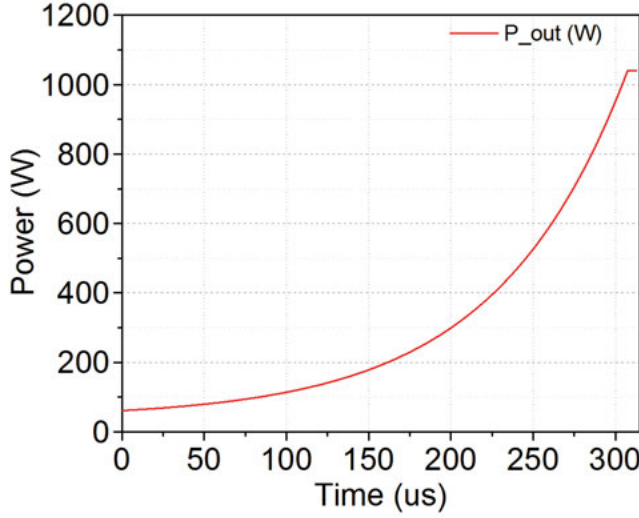
Figure 4.6. The pulse profile in time domain for one module as a function of time. Reprinted with permission from [**Paper VI**].

550 MWh, respectively [187]. Thus, the energy savings of 730 MWh in total with 684 €/MWh brings a reduction of the annual cost of 500 K€. Therefore, it is necessary to implement the optimal control scheme during the filling time of cavities allowing for accelerator designs towards sustainability and energy efficiency, as presented in Chapter 1.

The combination strategy I in section 4.1 is considered for the optimal charging scheme. The pulse profile in time domain is shown in Fig. 4.5. During a period of about 300 μ s, the RF power increases exponentially till the nominal power level. The power generation system based on SSPAs suffers of a sub-optimum efficiency i.e. at low and medium-range power level the efficiency of the amplifiers is rather low. To realize an optimal charging, the efficiency of the solid-state based generation system, using envelope tracking techniques, is highly increased. The implementation is realized on a kilowatt-level module as a proof-of-concept. This proof-of-concept design could be then scaled up in power till the nominal 400 kW using passive components, as can be seen in 4.1.

4.2.1 A proof-of-concept design for optimal charging scheme.

Envelope tracking (ET) is a well-established technique in communication systems [188–190]. In this thesis, we have adapted this technique to the single-ended kW module described in [**Paper I**] in pulse operation referring to the pulse profile in Fig. 4.6. The realization on the kilowatt-level module in [**Paper I**] consists of two parts: one is to generate an input RF signal fol-

lowing the shaping function in Fig. 4.6, the other part is to apply the generated shaping signal for the envelope tracking amplifier module.

Generating the input shaping function:

The shaping function generator makes use of a field-programmable gate array (FPGA) platform KC705 from XIlinx [191] and a quad-channel 16-bit DAC34SH84EVM from Texas Instrument [192]. The shaping function is represented by a mathematical expression as follows:

$$f(t/f) = \begin{cases} K1 * 10^{\frac{10 log_{10} \frac{e^{(X_{rise}(t/f)*K2)^2}}{K3*(sinh(2))^2} - 10}{20}} & \text{if } 0 \leq t \leq 300\mu s \\ 1 & \text{if } 300\mu s < t \leq 3.5ms \\ 0 & \text{elsewhere} \end{cases} \quad (4.1)$$

where K1, K2 and K3 are fitting parameters and f is the sampling frequency. These parameters are adjusted to fit the shaping function as provided in Fig. 4.6. A script written in Verilog Hardware Description Language (VHDL) is then used to implement the shaping function with a clock of 125 MHz. The KC705 platform transmits the data to a DAC34SH84EVM via 32-bit low-voltage differential signaling (LVDS) interface. The LVDS data goes through a multi-stage interpolation filter before feeding the digital mixing stage. A graphic user interface (GUI) provided from Texas Instruments is used to set different parameters via a serial interface i.e. frequency of built-in frequency (NCO), number of interpolation filters, gain of digital-to-converter (DAC), programmable delays, etc. A wide-band transformer [193] in combination with a matching network allows to convert the 32-bit LVDS output to a 50 Ω unbalanced output for the proof-of-concept amplifier in [**Paper VI**]. Details can be found in [**Paper VI**].

Implementation of the envelope tracking solution:

The proof-of-concept envelope tracking system consists of several components, including: a fast-switching power supply modulator (SM52-30 from Delta Elektronika), FPGA-based signal generator, driver stage, kilowatt-level single-ended amplifier module in [**Paper I**], and a measurement setup as described in [**Paper II**] in time domain. The signal generator produces an envelope control shaping function allowing to control dynamically the supply modulator . The envelope control function is tailored from Eq. 4.1 in the form of a time domain modified function M_{opt}, as follows:
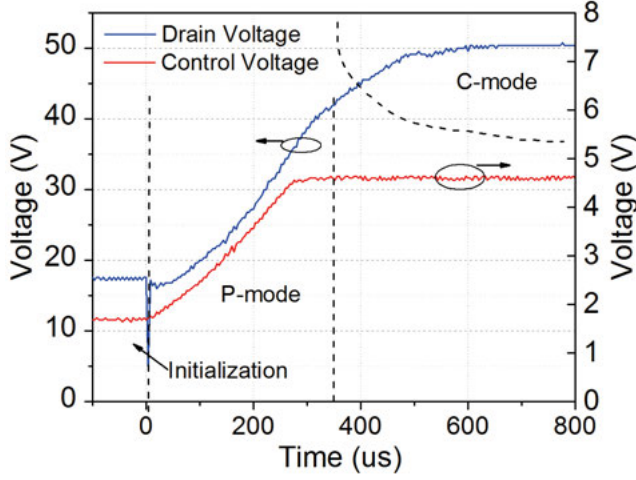
Figure 4.7. Control voltage and drain voltage of the proof-of-concept design as a function of time. Reprinted with permission from [**Paper VI**].

$$
M_{opt}(t/f) =
\begin{cases}
0.3815 & \text{if } -200\mu s < t \leq 0 \\
7.75 * 10^{\frac{10log_{10}\frac{e^{(X_{rise}(t/f))^2}}{4*(sinh(2))^2}-10}{20}} & \text{if } 0 \leq t \leq 300\mu s \\
1 & \text{if } 300\mu s < t \leq 3.5ms \\
0 & \text{elsewhere}
\end{cases}
\tag{4.2}
$$

The modification of M_{opt} depends mostly on the supply modulator's characteristics, and modes of operation of the envelope tracking amplifier [194] as described in [**Paper VI**], see Fig. 4.7. Care should be taken for the time alignment between the envelope control path and the RF pulsed signal path. The time alignment is programmable in a FPGA platform and is adapted to achieve the best performance in terms of efficiency. The capacitance at the drain of the proof-of-concept design is removed as to allow the fast supply modulation, following the recommendation in [195, 196]. This might lead to instability due to the low capacitance at the drain terminal. A measurement setup in time domain is used to characterize the performances of the proof-of-concept design regarding output power waveform, efficiency waveform, especially during the first $300\mu s$ that are particularly of interest.

As can be seen in Fig. 4.7, the supply modulator exhibits saturation when supplying the amplifier in the high power range. This inhibits the linearity of the amplifier, as described in [**Paper VI**] when full power is reached (i.e. the transition region prior to the flat-top of the pulsed RF). In this thesis, a
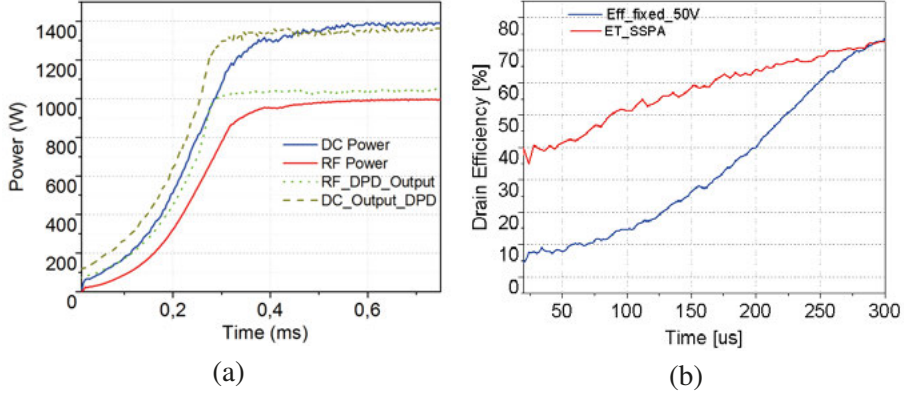
Figure 4.8. (a) Output power and DC power waveform as a function of time with and without the linearized approach. (b) Efficiency as a function of time in case of constant drain voltage and dynamic drain voltage. Reprinted with permission from [**Paper VI**].

linearized function is implemented in order to enhance the linearity for the proof-of-concept design. More insights can be found in [**Paper VI**].

4.2.2 Results and discussions

Characterization results:
Efficiency waveform is clearly an important figure-of-merit for the characterization of the envelope tracking (ET) system as described in [**Paper VI**]. The efficiency of the ET system is characterized in terms of the efficiency of the amplifier module [**Paper I**] associated with the efficiency of the supply modulator (SM52-30), as follows:

$$\eta_{ET\_system} = \eta_{SM} \times \eta_{SSPA} \tag{4.3}$$

The characterization of the supply modulator (SM52-30) is performed using a power analyzer (PCE-830) allowing for measuring the input power with a constant nominal 230 VAC. At the output load of the supply modulator, the voltage and current sensors record the measure of the output power with high accuracy. For the efficiency of the amplifier module described in [**Paper I**], a dedicated measurement setup is realized in time domain which allows to characterize the amplifier's efficiency waveform, output power waveform, current waveform, and voltage waveform. Some preliminary results shown in Fig 4.8, are compared to the obtained results with a fixed drain voltage of 50 V. A significant improvement in efficiency at low and medium-range power levels is obtained when applying the optimal shaping profile with the envelope tracking technique. The results allow to validate the energy efficiency improvement and new power amplifier design approach to practically implement optimal charg-

ing scheme for very high power system using the solid state technology [13]. The over-arching realization would allow reaching key objectives i.e. the development of greener and more sustainable Big Science infrastructures.

Discussions:

Implementing the envelope tracking modulation at 400 kW would allow a significant reduction of the energy consumption up to 24% in addition to a minimized reduction of reflection power during the charging time. For a large system, a valuable figure-of-merit R_{wall}, as defined in [13], is used allowing for analyzing the benefit of the optimal charging scheme as compared to the step filling scheme. From the theoretical analysis realized in [13], it is concluded that the particles should be injected at an optimal cavity charging time of 1.5 times the cavity step filling time for best performance of the energy consumption. The optimal charging time is then computed on the order of 312 μs. As a result, the value of the energy savings from wall plug R_{wall} can be represented as a function of charging time with respect to other established technologies in accelerator community, see Fig. 4.9.

The analysis of R_{wall} demonstrates the optimal filling scheme is most suitable to the solid-state based amplifiers in comparison with other types of amplifiers i.e. Tetrodes, and Klystrodes. The feasibility study of the optimal filling scheme is realized in this chapter and the results have the potentials to inspire the next-generation particle accelerators to adopt the solid state technology, as the technological choice for envelope-tracking energy-efficient power amplifiers.
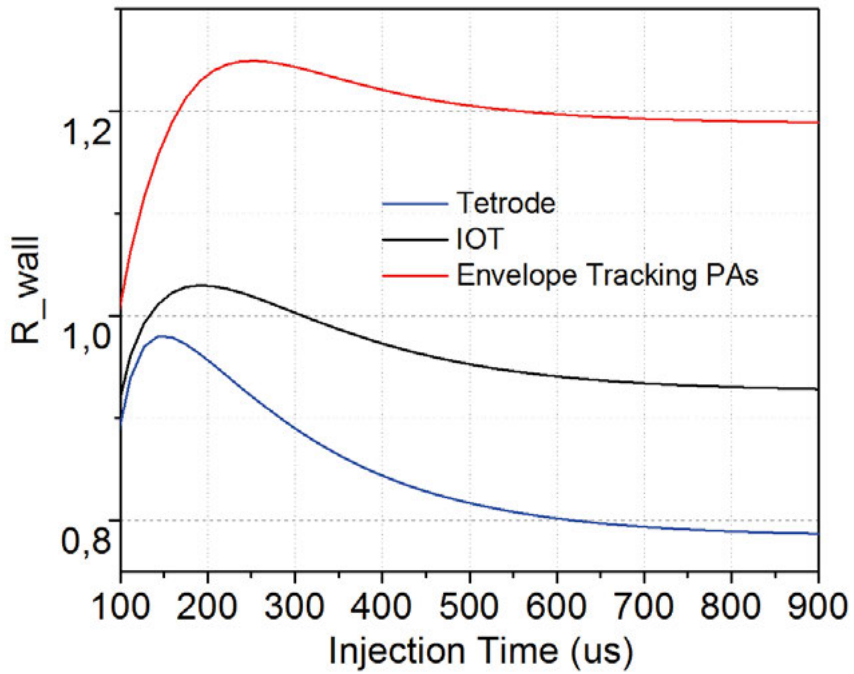
Figure 4.9. Energy efficiency R_{wall} as a function of charging time with several technologies i.e. Tetrodes, Inductive Tube Outputs (IOTs), and ET amplifiers in [**Paper VI**]. Reprinted with permission from [**Paper VI**].

5. Conclusions and future works

5.1 Conclusions

This thesis contributes to the development of the next generation RF power systems for particle accelerators in Big Science projects, implementing the latest solid-state technology (i.e. LDMOS) and high power low loss combining strategies. One new design is introduced, the single-ended architecture at kilo-watt level based on a two-stepped impedance matching network. The work is realized for the European Spallation Source (ESS) specifications i.e. 352 MHz pulsed mode operation with 5% duty cycle. The design approach in [**Paper I**] combined with advances in LDMOS technology results in a superior performance design for pulsed operation. Time-domain characterization methods are improved in [**Paper II**] and are applicable to extend for the measurements at higher frequency and higher power levels.

In this thesis, new engineering solutions for the power combination are proposed and realized [**Paper III and Paper IV**]. These solutions focus on power-handling capability, compactness, low loss and cost reduction. Suspended-stripline technology with air dielectric results in extremely low loss power combiner. The re-entrant cavity in combiner with doornob-based geometry [**Paper IV**] allows for an excellent performance of 0.2% insertion loss, 0.1% amplitude imbalance, 0.036^o in phase spread among ports and good thermal properties for high power combination. Other high power tests demonstrate the power handling capability of these solutions at 20 kW peak power level for 2-way combiner in [**Paper III**] and 100-kW peak power level for 12-way cavity combiner in [**Paper IV**]. These engineering solutions presented in this thesis are suitable for mid-range and high-range power level up to a few hundreds of kilo-watts. The demonstration of a 10 kW SSPAs [**Paper V**], which is then considered as an elementary block supporting the engineering discussion for scaling up in power till 400 kW, the nominal power per SC RF cavity at ESS linac. To the best of our knowledge, the presented system is by far improving the state-of-the-art in terms of efficiency and compactness for a system at 10 kW power level and at 352 MHz. Insights of system design presented in this thesis can be used as baseline for the integration of the next generation particle accelerators. With the LLRF controller demonstration of the compensation and stabilization of the power delivered are essential for the scale-up in power required for the accelerating structures [**Paper V**]. The demonstration of the droop compensation is realized, using a digital feedback loop and the results show 0.4 dB droop within the pulse is compensated when operating at 10 kW output power level.

This thesis investigates and gives solutions for more and more actual challenge which is of energy efficiency and reduction of the wasted energy due to mismatch during the filling period of accelerating cavities. For the first time, an optimal charging scheme is applied using a solid-state based amplifier without degrading the efficiency during operation i.e. the system is ramped-up in power to charge cavities, low reflection levels from the SC RF cavity. This is facilitated by realizing a very fast envelope tracking power supply (ETPS) operated over a charging time of 300 μs, as would be required by ESS [8]. The ETPS system is implemented on a single module and it is possible to realize the up-scaling in power till the nominal power level of 400 kW. This thesis discusses some of the possible architectures based on the demonstrated the ETPS module and gives a calculated improvement of just 24% of energy savings in comparison to the step filling scheme. The results of this thesis will facilitate the development of sustainable next generation particle accelerators in New Big Science projects and other future high power applications, all using solid state power amplifiers.

5.2 Future Works

Some of the future works that the author believes are highly relevant and interesting to be considered.

- In accelerator community, reliability is of paramount importance since the accelerator facilities require stringent demand of availability. Therefore, the reliability analysis of solid-state based power generation systems is paramount. A feasible extensive of the measurement setup in [**Paper I**] can be performed as a smart testing system with capability of harvesting sensors data and extracting the RF behavior towards the prediction and avoidance of failure i.e. stress tests, and optimizing RF amplifier's properties, and increasing its reliability.

- After successful demonstration of the proof-of-concept design presented in [**Paper IV**], a higher integration could be developed considering individual DC modulators instead of using commercial ones as in [**Paper VI**]. This will facilitate the integration that is required high power i.e. 400 kW for ESS spoke cavities. In addition to this, using individual supply modulators helps implementing corporate-combining architecture in case of using multi-inputs separately without the use of divider stage.

- The ultimate goal of this thesis is to provide a methodology allowing for implementing high power high efficiency power systems required not only in accelerator applications but also in other higher-frequency applications. For these purposes, it would be interesting to address all of this work on GaN technology at high power levels i.e. hundreds of kilowatts, or even MW, aiming to fully replace tube amplifiers in future sustainable systems.

6. Summary of the papers

Paper [I]: **Kilowatt-level power amplifier in a single-ended architecture at 352 MHz**

In this paper, a design approach of single-ended kW-level SSPA is adopted. The feasibility of single-ended architecture is demonstrated allowing for delivering more than 1.25 kW peak power in deep class AB under ESS specifications (352 MHz RF pulsed with 5% duty cycle). The design in [**Paper I**] is also tested in CW operation, however, efficiency drops to 60% due to thermal issue. To the best knowledge of authors, the design achieves a high efficiency of 71%. The adopted architecture opens up a new perspective towards kilowatt-level power amplifiers with a similar efficiency and output power, without requiring more complex circuits structures,such as baluns. This, therefore, contributes to improving the competitiveness of solid-state based power generation systems i.e. low manufacturing cost, ease for tuning and scaling in power, etc.

Paper [II]: **Time domain characterization of high power solid state amplifiers for the next generation linear accelerators**

For next-generation linacs i.e. ESS linac, the requirements of RF power sources are stringent regarding output power, efficiency, amplitude and phase stability. Characterizing SSPA modules of such power sources play an important role to validate PA design, thus reducing the design cycle. This paper presents the time domain characterization of high power pulsed solid state amplifiers in [**Paper I**] to be used for linear accelerator applications. All of PA properties are fully characterized in large-signal measurements when operating at kW level. In this paper, the time-domain measurement setup allows measuring pulse-to-pulse (P2P) stability in both amplitude and phase, then gives insights to which factors degrade the P2P stability during high power operation. Since a degraded stability in RF power sources might cause instabilities in particle accelerators when beam is injected i.e. no consistent energy is provided to the accelerated particles.

Paper [III]: **High-power low-loss air-dielectric stripline Gysel divider/combiner for particle accelerator applications at 352 MHz**

This paper focuses on an engineering solution to improve the power handling capability of a Gysel structure. The solution is based on an air-dielectric stripline which allows to handle very high radio-frequency power levels with low-loss suitable for power combination in accelerator applications. A test of 2-way combiner using the proposed structure

is performed under 22 kW peak power level. The efficiency and power handling capability of the combiner are greatly improved by choosing appropriate thickness of striplines and using air as a dielectric. This engineering solution presented in this paper allows realizing combiners in the mid-range power states of a few dozens kW level of power.

Paper [IV]: **12-Way 100 kW Reentrant Cavity-Based Power Combiner With Doorknob Couplers**

In this paper, we proposed an engineering solution of high power combiner aiming for power-combining stage at hundreds of kW to be used in 400 kW power generation system for ESS spoke cavities. The combiner is based on a re-entrant cavity with 12 input doorknob couplers and one output coupler that is integrated with the post of the cavity and forms doorknob type geometry. The presented design allows for an excellent mechanical quality and RF performance i.e. 0.2% insertion loss and a relative rms amplitude imbalance between the ports of 0.1% and phase imbalance of $0,036^o$ rms, suitably for industrial mass production, simple scalability, and good thermal characterization for high power handling. A high-power test implemented at 200 kW (352 MHz pulsed RF, 5% duty cycle) in back-to-back configuration shows good RF loss to be comparable to the low-power measurements and in the long run the combiner temperature stabilizes at 10° C above ambient.

Paper [V]: **Feedback compensated 10 kW solid-state pulsed power amplifier at 352 MHz for particle accelerators**

This paper presents insights of a modular and scalable 10 kW solid-state based RF system, which consists of 8 single-ended amplifier modules in [**Paper I**]. In the presented 10 kW system, the single-ended design approach toward compactness, high stability, high efficiency, and easy repeatability is validated at the kilowatt level, each of the power amplifier modules delivering up to about 1.3 kW output power. The 10 kW system uses a Gysel-based combiner realizing on the planar technology with a layer-by-layer approach. The layer-by-layer design approach makes the integration of 10 kW realizable in the 4U rack unit. For the 10 kW system, a combination of 8 modules is demonstrated. For ESS specifications, the SSPA-based 10 kW system exhibits 72% within the pulse in drain efficiency at 10 kW of output power. To best of our knowledge, the presented system is by far the best regarding compactness, efficiency at 10 kW of output power at this frequency of interest. In the second part, we characterize the power droop due to capacitor banks in the time domain. In open loop of compensation, it is about 1 kW within the pulse of peak value 10 kW and a duration of 3.5 ms. This may lead to the beam instability of the accelerator as particles are not provided with the same energy during the pulse. The compensation using an in-house LLRF is performed to facilitate the stringent requirements of droop within the pulse. The feedback 10 kW system is a contender

for scaling up in 400 kW power required in ESS spoke cavities' power generation systems.

Paper [VI]: **A proof-of-concept design of a highly efficiency solid state RF power source for Optimal Power Consumption during the charging of superconducting cavities**

This paper focuses on a very fast envelope tracking system (ETPS), realizing theoretical developments related to an optimal charging in pulsed modes of ESS SC cavities [13]. The ETPS is the first to demonstrate kilowatt power level envelope modulation with rising time as fast as 300 μs that would be required for ESS. This implementation is performed using an FPGA platform (KC705) along with ADC/DAC boards, controlling both a fast DC power supply (SM52-30 from Delta-Elecktronika) and generating RF signals. For 400 kW system to power ESS spoke cavities, the use of optimal charging scheme in combined with the ETPS results in an improvement of 25% in overall energy savings as compared to the conventional filling method (i.e. full power is provided to cavities in the beginning). This demonstration opens a new paradigm in accelerator facilities when considering design of RF power generation systems for accelerating cavities towards minimized wasted reflection power during charging time, optimized efficiency while in high power operation, thus reducing overall energy consumption.

7. Sammanfattning på Svenska

En lösning som uppfyller krav på effektivitet, komplexitet och kostnad är ett måste i RF-kraftsystem för acceleratordelen i nästa generations partikelacceleratorer. Denna avhandling handlar om design- och konstruktionslösningar för att nå en sådan lösning. En slutsats från avhandlingsarbetet är att utvecklingen av nästa generations RF-kraftsystem kommer att implementeras med den senaste solid-state-teknologin (dvs. LDMOS eller GaN) och kombinationsstrategier för hög effekt. En single-ended arkitektur baserad på en tvåstegs impedansmatchningsteknik används för att realisera en förstärkarkonstruktion för effektnivåer över kilo-Watt. För att möta ESS-specifikationer vid pulserat läge på 352 MHz är LDMOS den teknologi som kan erbjuda hög effekttäthet, hög effektivitet, och hög matningsspänning på 50 V. Designmetoden i [Paper I] i kombination med sådana framsteg i RF LDMOS-teknologin resulterar i överlägsen prestanda i pulserat läge för att erhålla högre effektivitet, hög uteffekt och samtidigt erbjuda enkel anpassning och massproduktion till låg kostnad. Designmetoden i [Paper I] öppnar också ett nytt paradigm för andra pulsade högeffektsystem som kräver kompakthet, effektivitet och effekt för andra tillämpningar, som t ex material-uppvärmning, kommunikation, radar, etc. En storsignals-mätmetod för högeffektmätning i tidsdomän [Paper II] presenteras för att fullständigt karakterisera förstärkarkonstruktionerna [Paper I] vilket möjliggör kortare designcykler och användandet av högre frekvenser. Kombinerare (vilka används för att blanda flera effektsignaler) är vanligtvis mycket skrymmande strukturer i ett RF-kraftproduktionssystem. I denna avhandling föreslås tekniska lösningar för nya strategier for kombinerare [Paper IV] och realiseras i [Paper III and Paper IV]. Dessa lösningar fokuserar på förmågan att hantera effekterna, kompakthet, låga förluster och kostnadsminskningar. I [Paper III] resulterar den upphängda stripline-tekniken med luft dielektrika i en extremt låg förluststruktur som implementeras på en Gyselbaserad topologi, med 0.1 dB ingångsdämpning vid 352 MHz. En annan konstruktion av kombinerare i [Paper IV] möjliggör en utmärkt prestanda på 0.2% i införingsförlust, 0.1% i amplitudobalans, 0.036 grader i fasspridning mellan portarna och god termisk prestanda vid höga effektnivåer. Högeffekttester visar effekthanteringsförmågan hos dessa lösningar vid 20 kW toppeffektnivå för 2-vägs kombinerare i [Paper III] och 100 kW toppeffektnivå för 12-vägs kavitets-kombinerare i [Paper IV]. Dessa tekniska lösningar som presenteras i avhandlingen är lämpliga för medium- till högeffektnivå. Design och integrationsmetoder som presenteras i avhandlingen kan användas för att förbättra prestanda för system som består av ett antal moduler inom kombinerande

arkitekturer. Designmetoden för [Paper I] bidrar till att framgångsrikt demonstrera en integration av 10 kW (Solid State Power Amplifier) SSPA: er [Paper V], som sedan används som byggblock, med stöd för nya tekniska lösningar, [Paper III och Paper IV] för att skala upp till 400 kW i effekt . Så vitt författaren vet är det presenterade systemet överlägset bäst när det gäller kompakthet, effektivitet vid 10 kW uteffekt. Insikter om systemdesign som presenteras i denna avhandling kan också användas som grund för att integrera och realisera högeffektiva pulssystem som ska användas för nästa generations partikelacceleratorer. Det 10 kW SSPA-baserade systemet är enkelt att integrera med LLRF-regulatorn för att kompensera och stabilisera systemegenskaperna när man utvecklar acceleratorerna. För första gången utförs droppkompensationen inom pulsen baserat på PI-regulatorn [Paper V]. Vid implementeringen resulterar den digitala återkopplingsslingan i att framgångsrikt kompensera för 0.4 dB dropp i pulsen, vilket motsvarar 1 kW i effekt, vilket är orsakat av användning av en kondensatorbank. Denna avhandling undersöker en intressant utmaning i alla acceleratoranläggningar som har låg verkningsgrad under påfyllningsperioden, vilket orsakas av missanpassnings hos accelererande kaviteten när man bygger upp det elektromagnetiska fältet inuti kaviteten. För första gången tillämpas ett optimalt laddningsschema på en SSPA som möjliggör minimering av energireflexion utan att försämra effektiviteten under dess drift, dvs systemet rampas upp för att ladda kaviteten. Detta underlättas genom att realisera ett mycket snabbt envelope tracking power supply (ETPS), dvs ett styrbart spänningsaggregat, under en laddningstid på 300 μs, som krävs av ESS [8]. ETPS-systemet implementeras på en enda modul och kan realiseras för att skala upp till 400 kW enligt proceduren som bescrivs i [Paper V]. Avhandlingen diskuterar några möjliga arkitekturer baserade på den demonstrerade ETPS och ger en beräknad förbättring med 25% i energibesparingar med ett upprampat system, jämfört med stegfyllningssystemet. Resultaten i denna avhandling kan underlätta utvecklingen av nästa generations hållbara partikelacceleratorer i nya stora vetenskapsprojekt och andra framtida applikationer med hög RF-effekt.

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Xin dành những lời biết ơn sâu sắc nhất để gửi tới bố mẹ người có công sinh thành và nuôi dưỡng con. Không có bố mẹ sẽ không bao giờ có con của ngày hôm nay. Xin dành lời tri ân sâu sắc nhất đặc biệt tới mẹ của con, người luôn luôn động viên, tin tưởng và kiên nhẫn đầu tư tài chính để con vượt qua chính mình và đạt được giấc mơ của ngày hôm nay.

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Uppsala, where my Sweden story begins

November, 2019

Long Hoang Duc

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