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Chemical Mechanical Polishing of Silicon and Silicon Dioxide in Front End Processing

BY

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Abstract
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Chemical mechanical polishing (CMP) has been used for a long time in the manufacturing of prime silicon wafers for the IC industry. Lately, other substrates, such as silicon-on-insulator has become in use which requires a greater control of the silicon CMP process. CMP is used to planarize oxide interlevel dielectric and to remove excessive tungsten after plug filling in the Al interconnection technology. In Cu interconnection technology, the plugs and wiring are filled in one step and excessive Cu is removed by CMP. In front end processing, CMP is used to realize shallow trench isolation (STI), to planarize trench capacitors in dynamic random access memories (DRAM) and in novel gate concepts.

This thesis is focused on CMP for front end processing, which is the processing on the device level and the starting material. The effects of dopants, crystal orientation and process parameters on silicon removal rate are investigated. CMP and silicon wafer bonding is investigated. Also, plasma assisted wafer bonding to form InP MOS structures is investigated.

A complexity of using STI in bipolar and BiCMOS processes is the integration of STI with deep trench isolation (DTI). A process module to realize STI/DTI, which introduces a poly CMP step to planarize the deep trench filling, is presented.

Another investigated front end application is to remove the overgrowth in selectively epitaxially grown collector for a SiGe heterojunction bipolar transistor.

CMP is also investigated for rounding, which could be beneficial for stress reduction or to create microoptical devices, using a pad softer than pads used for planarization.

An issue in CMP for planarization is glazing of the pad, which results in a decrease in removal rate. To retain a stable removal rate, the pad needs to be conditioned. This thesis introduces a geometrically defined abrasive surface for pad conditioning.

Keywords: chemical mechanical polishing, chemical mechanical planarization, silicon, silicon dioxide, front end, shallow trench isolation, deep trench isolation, bipolar transistor, BiCMOS, wafer bonding

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List of Papers

I "Effect of dopants on chemical mechanical polishing of silicon"
Markus Forsberg, Niclas Keskitalo, and Jörgen Olsson
Microelectronic Engineering, **60**, pp. 149-155, 2002.

II "Effect of Diffused Boron and Phosphorus in Si(100) on Chemical Mechanical Polishing Removal Rate"
Markus Forsberg
Submitted to *Semiconductor Science and Technology*.

III "Effect of Process Parameters on Material Removal Rate in Chemical Mechanical Polishing of Si(100)"
Markus Forsberg
Manuscript.

IV "Silicon surfaces for hydrophobic wafer bonding"
Mats Bergh, Stefan Tiensuu, Niclas Keskitalo, and Markus Forsberg
Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding: Science, Technology, and Applications, Electrochemical Society Proceedings Volume **97-36**, pp. 87-94, 1997.

V "InP and Si Metal-Oxide Semiconductor Structures Fabricated Using Oxygen Plasma Assisted Wafer Bonding"
Markus Forsberg, Donato Pasquariello, Martin Camacho, and David Bergman
Journal of Electronic Materials, **32**, pp. 111-116, 2003.

VI "Chemical Mechanical Polishing for Surface Smoothing"
Markus Forsberg and Jörgen Olsson
Physica Scripta,**T101**, pp. 200-202, 2002.

VII "A Shallow and Deep Trench Isolation Process Module for RF BiCMOS"
Markus Forsberg, Ted Johansson, Wei Liu, and Manoj Vellaikal
Submitted to *Journal of the Electrochemical Society*.

VIII "A Base-Collector Architecture for SiGe HBTs using Low-Temperature CVD Epitaxy Combined with Chemical-Mechanical Polishing"
E. Suvar, E. Haralson, M. Forsberg, H. Radamson, Y.-B. Wang, and J. V. Grahn
Physica Scripta,**T101**, pp. 64-66, 2002.

IX "Geometrically Defined All-Diamond Abrasive Surface for Pad Conditioning in Chemical Mechanical Polishing"
Markus Forsberg, Joakim Andersson, and Staffan Jacobson
Submitted to *Journal of the Electrochemical Society*.

Contribution to the papers by the author to this thesis:

I Almost everything

II Everything

III Everything

IV Part of experimental work

V Most of writing, part of measurements

VI Almost everything

VII Most of writing, part of experimental work

VIII Part of experimental work

IX Most of writing, part of experimental work

Contents

1 Introduction

Chemical mechanical polishing (CMP) is a removal process combining mechanical work and chemical etching. In CMP, the work piece slides against a pad. Onto the pad a slurry consisting of particles (size on the order 10-200 nm) in a chemical active solution is supplied. CMP has been used for a long time in manufacturing of silicon wafers, here often denoted wafer polishing.[1] After crystal growing, the crystal rod is grinded to the desired diameter and sliced into wafers using inner diameter (ID) or wire sawing. Wire sawing, which is used in the more advanced wafer manufacturing processes such as for 300 mm wafers, has a lower kerf loss. Wire sawing rate for one wafer is slower than ID sawing but, however, several wafers are sawed at the same time, and therefore, the throughput is larger. Wire sawing can result in a higher waviness compared to ID sawing. After sawing the slices are grinded and/or lapped in order to get parallel surfaces. In grinding the abrasive particles are fixed in the grinding tool. In lapping the abrasive particles are free rolling between the wafers and a metal plate. Typically the particles are about 10 μm large. The lapping, which is a simultaneous double sided process, results in a higher parallelism between the surfaces but a lower removal rate compared to grinding. Grinding, which can be fully automated, is or is anticipated to replace lapping in the manufacturing of 300 mm wafers. However, the reduction of waviness from wire sawing in the grinding is an issue. The edge is rounded and the wafers are chemically mechanical polished using colloidal silica in an alkaline solution, particle size on the order of 10-100 nm. CMP is often performed in two steps: stock removal and final polishing. CMP results in defect free surfaces in contrast to mechanically polished surfaces (diamond particles and a soft pad).[2] From the most advanced 200 mm and 300 mm wafer manufacturing processes simultaneous double side polishing is used.[3] Double side polishing gives a better parallelism compared to single side polishing and less adherence of particles since both sides are smooth. Grinding is also used to thin fully processed chips,[4] to reduce the height in order to reduce the size of the completed package and to reduce the thermal resistance.

Lately, other substrates have become in use. One is bonded SOI where at least one wafer is oxidized before bonding. Smart cut is the dominating SOI technology, where a wafer is hydrogen implanted and bonded to an oxidized wafer.[5] By exposing the bonded pair to higher temperature the implanted wafer splits at the hydrogen concentration peak, and a thin silicon device

layer bonded to an oxidized handle wafer is obtained. A short CMP step is performed to smooth the device layer. This method is very cost effective since the implanted wafer (apart from the thin device layer split of) could be reused as the oxidized handle wafer. CMP has also been used in realizing wafer bonding for several other applications and materials.[6] Paper IV investigates silicon wafer bonding and CMP. Another substrate CMP application is to create SiGe substrates.[7] To increase the electron mobility in MOS channels, it could be desirable to use strained silicon. One way of doing this is by growing silicon on relaxed SiGe. The relaxation of the SiGe causes defects, which could result in an increased surface roughness. The roughness translates into a roughness of the strained silicon surface, which degrades the mobility. This could be solved by applying CMP on the SiGe before growing the silicon. Another use for substrate CMP is in thin film transistor (TFT) technology.[8, 9] In TFT, used for instance for making flat displays, polycrystalline silicon is deposited on glass substrates. The gate oxide breakdown voltage as well as channel mobility increased by smoothing the poly surface before further processing. Investigations have also been published regarding CMP of SiC of different polytypes[10-13] and GaN[14]. These new applications motivate further investigations of the basic silicon CMP. Paper I-III review what has been done on silicon CMP and further investigates the effect of process parameters and dopants on the removal rate.

With the ever decreasing depth of focus, when decreasing minimum feature size in very large scale integration (VLSI) circuits, it was recognized that planarization was not sufficient using spin on etch back or oxide reflow.[15] Furthermore, oxide cannot be reflowed if metal is on the surface. To obtain a more global planarization in contrast to local, CMP was introduced to planarize the deposited interlevel dielectric (ILD) oxide layers in metal interconnection layers. Apart from the limited depth of focus another driver for planarization is the increasing number of metal layers. Without planarizing the nonplanarity increase for each level. Apart from degrading the resolution in the lithography, nonplanarity could cause other problems such as thinning of the metal lines when they are going over steps or remaining metal stringers. CMP for ILD planarization is used in the aluminum wiring – tungsten plug interconnection technology. The general process for one metal level, outlined in Fig. 1a, proceeds as follows: sputtering and etching Al, depositing and planarizing ILD, etching plug, barrier deposition, chemical vapor deposition (CVD) of W for good step coverage, and removal of excess W. The reason W is used for plugs, even though it has a higher resistivity than Al, is that good gap-filling CVD processes can be used. Tungsten removal could be done by etching or by employing a W CMP step. Tungsten CMP has become a standard process due to the better planarity and improved defectivity compared to etch back. Here, W CMP is a damascene process: a plug is filled by a blanket

deposition and the excess material is removed by CMP, leaving the filling material at the same level as the surrounding surface. Al wiring – W plug interconnection technology using ILD and W CMP is today a mature technology. However, oxide CMP and W still lacks some fundamental understanding.

To reduce resistive losses in the interconnection stack, Cu is favorable compared to Al since it has a lower resistivity. Lowering the resistivity becomes even more important due to the smaller dimensions to avoid increasing the RC-delay in the interconnection layers. Also, copper has higher resistance to electromigration. Today, Cu interconnection technology is standard in the most advanced VLSI processes. Here, Cu CMP is an enabling technology. Cu lacks volatile etch species at low enough temperatures. Therefore, Cu could not be etched as the Al in the Al wiring – W plug interconnection technology. To solve this the plugs and wiring are etched in one step, the Cu deposited by electrodeposition[16] and the Cu removed by Cu CMP. This type of process, outlined in Fig. 1b, is called dual damascene since the plugs and wiring are deposited in one step. The purpose of Fig. 1 is to illustrate the different concepts of Al-wiring/W plug and Cu dual damascene. Note that barriers and etch stops (for Cu dual damascene) is not included. Different schemes for the etch, such as plug (via) or wiring (trench) first, self aligned and top hard mask as well patterned buried layer are in use or have been proposed.[17, 18]

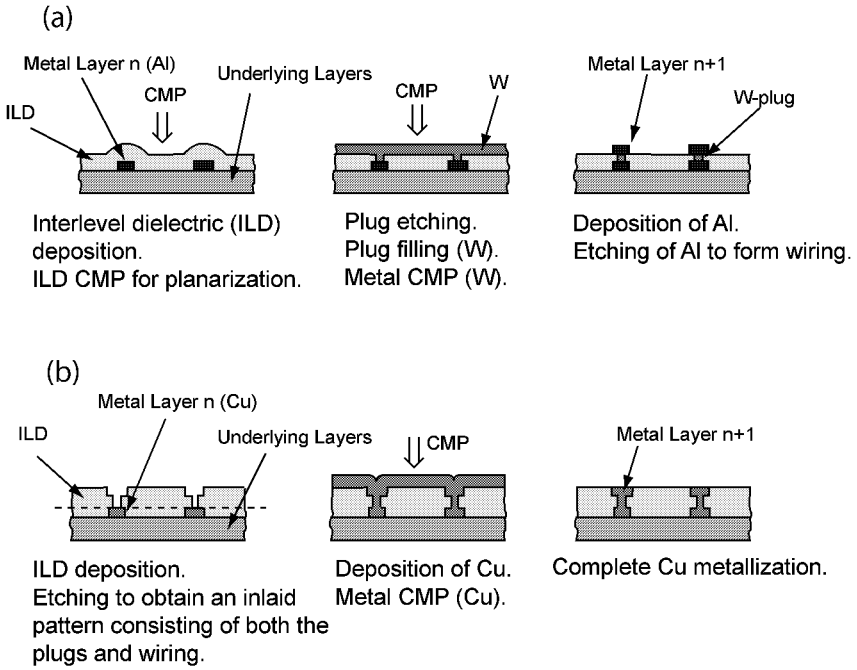

Figure 1. Schematic of Al wiring-W plug and Cu dual damascene metallization. Barriers and etch stops not included.

To reduce capacitive losses oxide could be replaced by low-κ dielectrics (decreases the capacitive coupling between the metal lines) for ILD. Some reduction, which is implemented in the more advanced processes, could be obtained by using fluorine doped silicon dioxide[19], κ about 3.7, or by having a less dense silicon dioxide with a higher hydrogen content (HSQ). To obtain further reduction in the capacitive coupling the use of polymer based materials with $\kappa < 3$ have been investigated. The Cu CMP stops on the barrier on ILD. Thereafter, the barrier is removed by a second CMP using slurry with a low selectivity between barrier and copper. The rigidity and the chemical resistance of the slurry chemical for the polymer ILD are issues in the integration for Cu/low-κ.[20] One way to ease this is to have a dielectric polish stop on top of the ILD.[21] However, some of the benefit of implementing polymer low-κ is then lost. For a more complete picture of issues in realization of Cu/polymer low-κ, consult the interconnect section in the 2003 edition of ITRS, Ref. [17]. CMP also is today employed for planarization of pre-metal dielectric, which often is phosphosilicate glass (PSG).[22]

Front-end is the processing before connecting to circuits in the metal layers as well as the starting material.[23] The most important use in front end CMP, apart from in manufacturing of the substrate, is to realize shallow trench isolation (STI).[24] STI has several advantages compared to local oxidation of silicon (LOCOS), such as better planarity, higher packing density and lower capacitances due to a non-present bird's beak, and the possibility to increase the field oxide thickness. STI-CMP was introduced by IBM, which gave much better planarity compared to etch-back only.[25] One later chapter of this thesis treats STI and Paper VII describes the implementation of STI in a BiCMOS process. Another front-end use is to planarize polyfilled trench capacitors for dynamic random access memories (DRAM).[26]

Other front-end applications include metal gate.[27] There are some issues with the use of poly gate, such as gate depletion and boron penetration.[28] Another driver for metal gate is that the gate resistance increase when decreasing gate width can be suppressed. The reason poly gates are in use is that it can withstand the high temperatures in the annealing of the source and drain implantations enabling self-alignment. To implement metal gate one scheme is to use a dummy gate for source and drain self-alignment. After source/drain implantation dielectric is deposited and planarized by CMP. The CMP is performed long enough to reach down to the dummy gate. Thereafter, the dummy gate is removed by selective etching and metal is deposited. A damascene metal CMP step is performed. In this way, a metal gate self-aligned to the source/drain implantations could be obtained. Metal ferroelectric MOS device has also been implemented in a similar way.[29] Noble metals are gaining interest to use as barrier and as electrodes in DRAM and FeRAM. Therefore, CMP of iridium and iridium oxide has been

investigated.[30] Other uses for CMP in gate engineering include in formation of a T-shaped gate[31], realization of a memory device process where the gate electrode is silicidated after formation of a lightly doped drain,[32] and planarization of gate poly before silicidation to suppress agglomeration at the LOCOS corners.[33] Applying CMP before growing oxide on polysilicon decreases leakage, result in less trapping and higher breakdown field, which will increase the data retention time for non-volatile memories.[34] CMP after polydeposition has also been found to reduce losses in polysilicon waveguides.[35] CMP has also been explored for polysilicon surface micromachining.[36] Bipolar transistors with implanted base have been processed combining selective epitaxial growth (SEG) and CMP.[37] In Paper VIII this concept is investigated with a SiGe epitaxial base. Other applications for SEG and CMP include formation of fully isolated multiple layers of silicon-on-insulator islands.[38] Paper VI describes a new use for CMP, which is for rounding and smoothing, using a soft pad.

The focus on this work is on silicon dioxide and silicon CMP for front end processes. Two direct applications are described: STI/DTI for BiCMOS (Paper VII) and planarization of selectively grown collector in processing of a SiGe heterojunction bipolar transistor (HBT). Another front-end application is speculated in Paper VI: smoothing for corner rounding or to create microoptical devices. Papers I-III investigate the basic silicon CMP process and Paper IV investigates CMP in silicon wafer bonding. Pad conditioning is a common issue to all CMP processes. Paper IX introduces geometrically defined abrasive surface for pad conditioning.

The outline of this thesis is as follows: first is the introduction above followed by description of CMP in practice, describing a common machine configuration, consumables and cleaning technologies. This is followed by a summary of some modeling, theory and surface characterization as well as fundamental experimental work done on CMP. Then, processing to realize STI is described in depth. Here, concepts and issues also common to other CMP processes, such as dishing, erosion and dummy pattern, are outlined. Then the included papers are summarized. Last follows a discussion on further research based on the results obtained in this work.

2 CMP in practice

For CMP, a system is needed together with consumables, which are pads, slurries, and pad conditioners. This chapter will discuss these different components as well as cleaning after CMP.

2.1 CMP machines

Several machine configurations exist, such as rotating, linear and orbital tools.[18] In this work, two rotating machines, the Applied Materials Mirra system, a common system used in the industry, and the bench-top Logitech PM4, a laboratory-scale polishing machine, were used.

In Paper VII a Mirra is used for processing STI/DTI for bipolar/BiCMOS is for up to 200 mm wafers. A schematic top view of the system is shown in Fig. 2. It has three plates onto which pads are mounted and four heads. The heads, fixed to a carousel, can sweep in the radial direction of carousel. The wafers are transferred from plate to plate and to the load station by rotation of the carousel. At the load station the wafer is removed from the load cup by a robotic arm. The wafers are taken from and loaded to cassettes in a wet tank.

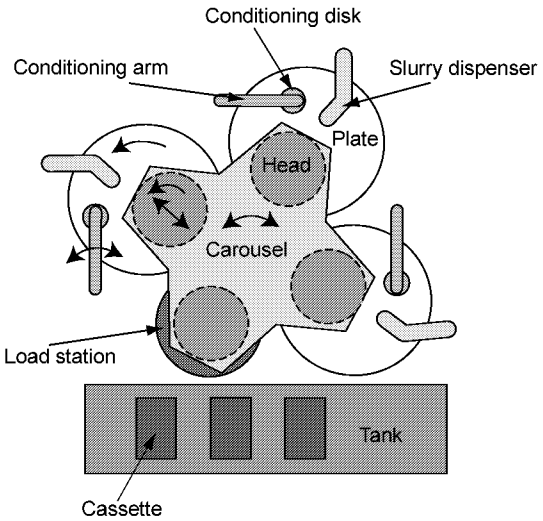

Figure 2. Schematic of the Mirra system.

It is necessary that the wafers are not allowed to dry before cleaning. Otherwise, adhered particles could be difficult to remove. The Mirra is also supplied with an integrated cleaning tool, the Mirra Mesa system. This gives a fully automated dry in/dry out process and, therefore, the cassettes with the wafers do not need to be manually loaded into a cleaning station. Since the Mirra has three plates, different processes could be run on the different plates. One common configuration is to do main polish on the first two plates and a buffing/cleaning step on the last. The head sweeps the plate to even out the pad wear. Mirra has (like most CMP system) the possibility to do pad conditioning (in-situ or ex-situ) to maintain pad roughness. A diamond pad conditioning disc is fixed at the end of a conditioner arm. The conditioner arm sweep can be set to different retention time over different radius of the pad. One way to optimize the pad conditioning for the Mirra is described in Ref. [39]. Pad conditioning is further described in section 2.2. Pumped delivery systems supply slurry to the plates. The polish pressure on the wafer is supplied by pneumatics on a polymer membrane in the polish head. Around the membrane there is a retaining ring, holding the wafer in place. The retaining ring pressure is set separate from the wafer (membrane) pressure. By this, the stress from the pad will be more uniform across the wafer.

The Mirra has an in-situ end-point system (in-situ rate monitor).[40, 41] The plate has an opening over which a window in the pad is fitted. A laser beam is directed through the widow and reflects on the wafer back through the window. A sensor in the plate collects the reflected beam and the signal is filtered. If there is a change in material over a large part of the wafer area when the CMP step should be stopped (for instance in metal CMP or in STI-CMP with a large pattern density) there is large change in the reflectivity of the wafer surface and that will trigger the process to a halt. In oxide planarization there is no change in surface material, but the oxide thickness removed is measured based on interferometry. The thickness of the remaining oxide can be set to be the same in a lot if the incoming thickness results in a reflected signal which is within the same period. Other endpoint methods used or proposed for CMP include friction sensing, conductivity, impedance, acoustic and electrochemical methods.[42]

A bench-top PM4 Precision Lapping and Polishing Machine, from Logitech Ltd., was used for the fundamental research (Papers I-IV, VI), to demonstrate CMP of SEG collector (Paper IV), and to test the new abrasive surface for pad conditioning (Paper IX). Figure 3 shows the general features of the equipment. The machine has a 30 cm diameter polishing plate to which a polishing pad is mounted.

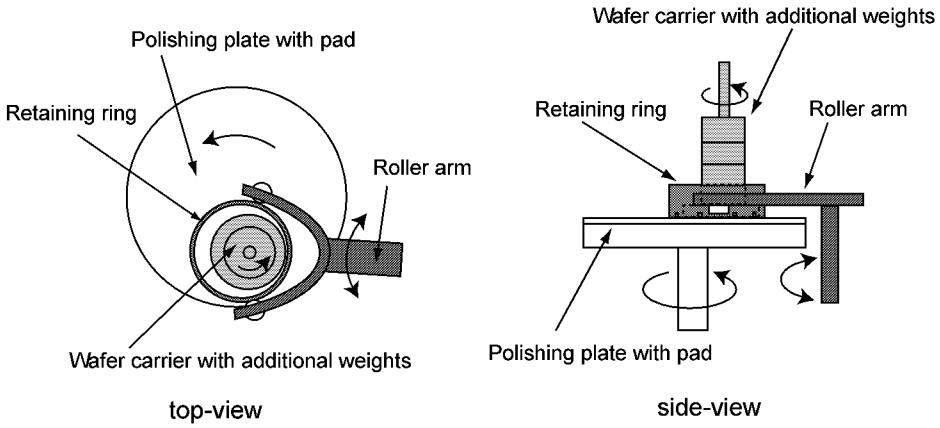

Figure 3. Schematic of the Logitech PM4.

To support the wafer during polishing, it is mounted with wax, Thin Film Wax from Logitech, or by using a template assembly, NTA DF200 from Rodel, Inc., onto a glass substrate. When using wax, a VPB1 Vacuum/Pressure Bonding Jig from Logitech is employed in order to get a more uniform bond. The template assembly consists of a polymer backing material, DF200, on which the wafer rests, and the template, which holds the wafer in place. The template used has a pocket depth of 0.010". The assembly has an adhesive on the back, which is used to mount it to the glass substrate. The glass substrate, with the mounted wafer, is put in a wafer carrier (with the wafer facing the polishing pad). The carrier rotates inside a ring held in place by a roller arm. The ring has openings at the bottom to increase the amount of slurry reaching the wafer. To increase the friction between the carrier and the ring, an elastomer ring is fitted around the side of the carrier. Starting rotating the plate, the ring and wafer carrier adopt the same rotation orientation as the plate. The roller arm can sweep the ring (and the carrier) across the pad in order to have a more uniform pad wear. Pressure is applied by adding weights to the wafer carrier. The polishing slurry is supplied to the pad from a small container at the side of the polishing plate. When 4" wafers were polished, a template assembly fitted directly on a carrier with the size of the ring was used.

Polishers in manufacturing of prime wafers are multiwafer machines (several wafers are ran on the same plate at the same time). However, in VLSI processes single wafer CMP, as the Mirra, is used to get sufficient process control. Even though up to three wafers can be run at the same time (one wafer per plate), the Mirra is classified as a single wafer machine because the polishing for each wafer can be individually controlled. Before smart cut, bonded SOI wafers where made by bonding two wafers (as least one oxidized) and thinning by grinding and polishing one of them to the desired thickness. This is still used to obtain a thicker device layer. To

achieve appropriate thickness control in the polishing, the SOI community turned to use single wafer VLSI CMP tools instead of prime wafer polishers.[43] Therefore, the development of CMP for planarization gave a spin-off effect in a much enhanced process control in thinning for bonded SOI. Furthermore, it is claimed that there is a lack of characterization data for silicon polishing what so ever for most of VLSI CMP tools. To the author's knowledge, no extensive characterization data on silicon has been published in the open literature since Ref. [43] was published. This further motivates study of the basic silicon CMP process.

2.2 Pads for CMP

In this work only pads from Rodel, which is the largest supplier of CMP pads, have been used. Therefore, only pads from this manufacturer will be discussed. CMP pads can be classified in three different types, which have different uses. The most common type in VLSI processing consists of microporous polyurethane, such as the IC1000 pad. This type of pad is the hardest of three types. This makes the pad conform less to the wafer surface and, therefore, it gives the highest planarity. However, the pad should adjust to any bow or long-range waviness across the wafer. Otherwise, the nonuniformity over the wafer would be high. To achieve a high planarity as well as a low within wafer nonuniformity, stacked pads, consisting of a harder pad on top with a softer pad beneath, are used.[44] One common configuration is IC1000 on top of Suba IV. Suba IV consists of a polyurethane impregnated polyester felt, which is the second hardest type. Another type of stacked pad is IC1400, which consists of IC1000 on top of a foam base pad. Microporous pads, such as IC1000, are often grooved to improve slurry access to the center of the wafer.[45] The IC1000 pad alone, without subpad, is commonly termed solo IC1000 pad.

Polyurethane impregnated polyester felt pads alone are used for stock removal polishing, the first polish step (after slicing and grinding/lapping) in wafer manufacturing. Above, Suba IV has been mentioned. Another pad of this type is Suba 500. This type of pads give high silicon removal rate and plane parallel surfaces. A third type of pads is made of napped poromerics, which is the softest type. These are used for final polishing of silicon, such as UR100, or for cleaning/buffing after main polish in CMP in VLSI processing, such as Politex.

The effect of pad properties on the CMP performance, such as removal rate and planarity, will be further discussed in Chapter 3. The type of pad used could affect electrical quality of polished oxides.[46]

One wellknown phenomena in CMP in VLSI processing (using IC1000 or similar types of pads) is pad glazing, which results in a decrease in removal rate of material from the wafer with pad use. This has been attributed to pad

glazing involving deformation and smoothening of the pad surface, possibly caused by compressive and shear stresses during polishing[47] or interaction with the slurry.[48] The glazing decreases the ability of the pad to distribute slurry uniformly and increases the pad-wafer direct contact area. The latter effect decreases the effective pressure at the pad-wafer interface for a constant nominal pressure.[49] Modeling work has coupled the effect of pad deformation to the decrease in removal rate.[50] Figure 4 shows a new and a glazed IC1000 (the top pad of a IC1400). In the center of the glazed pad (left) a flat region is seen. Such flat regions increase the contact area.

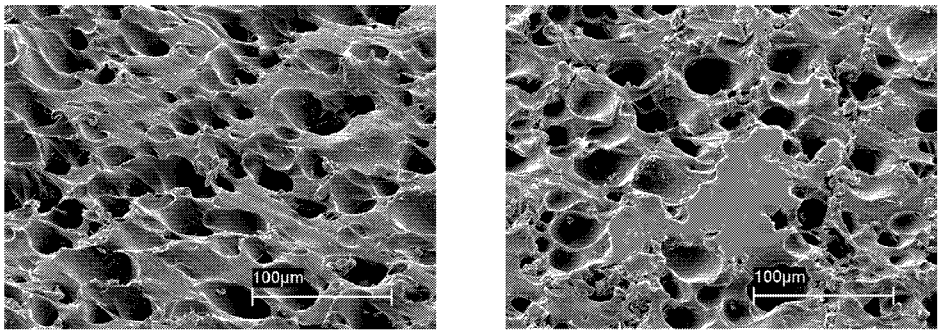

Figure 4. IC1000 (from a IC1400), right new pad, left glazed pad.

To retain a stable removal rate, the pad needs to be conditioned.[51] Optical interferometry measurements of conditioned and unconditioned pads have indicated that conditioning increases and stabilizes the pad surface roughness.[52] Pad roughing due to conditioning has also been recorded using stylus profilometry.[53] Also, a break-in is performed to stabilize new pads before running production wafers. Pad break-in involves pad conditioning without running wafers as well as in-situ pad conditioning running dummy wafers. If no break-in of a new IC1000 pad is performed in in-situ conditioning oxide CMP processes, the removal rate will initially increase from wafer to wafer.[54]

The state of the pad conditioner affects the pad asperity heights and the resulting removal rate of silicon dioxide deposited on the wafer.[55] Higher pad asperities gave a higher removal rate.

Usually, disks or rings with fixed diamond particles are used as conditioning tools. The particles can be mechanically held by being physically entrapped in an electroplated metal matrix. The diamond retention can be increased by formulating a matrix that bonds chemically and metallurgically to the particles[56] or by using a sintering process.[57] Much effort has been spent on retention, since diamond loss could cause severe scratching of the wafer.

Slurries formulated for metal CMP can cause dissolution of the metal matrix and hence promote diamond loss. If metal dissolution is avoided, in-

situ pad conditioning can be used in metal CMP, which increases the throughput compared to ex-situ pad conditioning. One way to avoid slurry contacting the metal matrix is using physical vapor deposition (PVD) diamond as a shield on a diamond grid brazed onto a stainless substrate.[58, 59] A cathodic arc method with a graphite cathode was used, giving nanocrystalline diamond.[58] Pad conditioners have also been created by chemical vapor depositing (CVD) a diamond film on uniformly placed diamond grit on silicon.[60] Metal dissolution is not as critical using slurries formulated for oxide CMP.

Paper IX introduces a new pad conditioning abrasive fabricated by chemical vapor deposition of diamond on an anistropically etched silicon mold. Pad glazing depends on the pad structure. In the buffing after W main polish the Politex pads is not conditioned even though oxide planarization slurry is used.

In Paper III the different behaviors of Suba 500 in silicon CMP and IC1400 in oxide CMP are shown. The silicon removal rate increases for a new Suba 500 pad, in contrast to a new IC1400 pad where the oxide removal rate decreases due to glazing.

Lately, a new type of pad utilizing fixed abrasive has been developed.[61] For this type of pad the abrasive particles are fixed at the pad surface. Only chemicals are supplied onto the pad.

2.3 Slurries for oxide, silicon and STI-CMP

For silicon and oxide CMP fumed or colloidal silica, particle size about 20-100 nm, in an alkaline solution is mostly used.[47, 49, 62] Water is important for the removal. Using other solvents, the removal rate is much smaller.[63] Ceria based slurries have also been investigated for oxide CMP.[47, 49] They gave a higher removal rate but lower selectivity between high and low areas. Ceria is softer than silica, and, therefore, the higher removal for ceria should be from enhanced chemical reactions.[64] By adding a surfactant (not disclosed more than it is a polymer of an anion group) to a ceria slurry a better planarity could be obtained compared to a conventional slurry.[65] Others have proposed that a MnO_2 slurry should be used to avoid pad glazing.[48] However, mostly silica based slurries are used today for oxide CMP.

For silicon CMP using silica slurry, it has been found that the removal rate reaches a maximum at pH 11, where also the highest hydrogen surface concentration and hydrophobicity are found.[66] For oxide CMP, it has been found that the removal rate slightly increases, when increasing pH of KOH added water used to dilute a silica based slurry (1:1 dilution).[67] Others have reported that the removal rate increases more significantly with the slurry pH.[49] Both NH_4OH and KOH are used to raise pH and stabilize slurries in oxide CMP slurries on the market today. In TEOS deposited oxides polished

using KOH stabilized slurries an about two orders higher mobile charge compared to using NH_4OH stabilized slurries has been detected.[46] However, KOH stabilized slurries are widely used, indicating that this is not critical.

Silica particles could agglomerate and cause defects if slurries are diluted on site due to pH variations during the dilution process.[67] The defect adding to the wafers when spiking the slurry with coarser particles has been investigated systematically.[68] Avoiding coarse particles entering the pad is done by filtration.[69] However, due to local variations and transients in the process, soft agglomerates could be formed after the point of filtration. Therefore, there is a continued research interest in the effect of soft agglomerates and in stabilizing silica slurries for oxide CMP using different polymeric surfactants.[70-73] Apart from slurry stability and defect adding, surfactants also affect other CMP process results such as removal rate and nonuniformity.[72, 73] Adding surfactants also showed the possibility to tailor the selectivity between oxide and polysilicon.[74] For baseline slurries oxide is removed slower than polysilicon. By adding surfactants, speculated to adsorb on hydrophobic polysilicon surfaces, the polysilicon removal rate is reduced and the oxide removal rate remains almost the same. Paper VII gives another example what slurry formulation can do; the difference in nonuniformity across the wafers after poly CMP for the two investigated slurries.

Effect of particle size has been investigated keeping the silica weight concentration constant. 30 nm size particles give a larger removal rate than 7 nm particles.[49] The removal rate increased with silica concentration for both sizes. Others have found that the removal rate goes through a maximum at a particle size of 80 nm.[75] The effect of particle size has been investigated for larger alumina (200 nm and more) particles in W CMP.[76] The removal increased with decreasing particle size.

Lately, in order to obtain a high selectivity between oxide and nitride, a renewed interest in ceria based slurries as high selectivity slurries (HSS) for STI-CMP (further described in Chapter 4) has arisen.[77-79] One issue with the use of ceria slurries has been the stability of the slurry, which can cause more defects on the wafer.[78] Detailed reports on slurry development of ceria based slurries, including the effect of abrasive morphology, physical characteristics and surfactant concentration as well as nanotopography (further described in Chapter 4) have recently been published.[80-83] There has been reported on silica based HSS with an additive that forms a passivation layer on the nitride.[84] Low nitride removal rates have also been obtained with corundum slurry.[85]

For metal CMP, slurries with alumina particles are used containing several additives, such as surfactants, inhibitors and oxidizers. It goes beyond the scope of this thesis to detail the development and formulation of metal CMP slurries. Some references are here given for the interested reader.[18, 86-94]

Research has been started on very sophisticated slurries for instance mixed abrasive slurries containing particles of different materials and size or slurries with coated particles.[94-97] Using these approaches it can be possible to at the same time take advantage of mechanical properties of one material and the chemical properties of another material. Slurry manufactures do not disclose much information about their slurries. The author to this thesis believes that slurry engineering is a field suitable for academic research. There is a lack of fundamental understanding and much can be done without having an industry CMP machine. For investigating properties such as selectivity, removal rate and resulting surface chemistry a bench-top machine is enough. It involves several fields, such as surface chemistry, synthesizing and characterization of colloidal particles, and tribology. Also, it requires understanding of the microelectronic motivation for the research. Obviously, pad development in academia is difficult because at some stage a fullsized pad within given tolerances to verify a new pad structure has to be made.

2.4 Cleaning

After CMP the wafers need to be cleaned in order to remove the slurry particles. Buffing (running wafer on a soft pad), brush scrubbing, and megasonic bath are used. Cleaning is often done at alkaline pH. A negative surface potential is present both at silica particle surface as well as the oxide (silica) wafer surface (negative Zeta potential). Therefore, the particles are repelled. Surfactants can be added to reduce the surface tension.[98] The wafers should never be allowed to dry before final cleaning.

In Paper VII where an industry Mirra was used, rinsing is done on the third plate with ammonium added DI water and a Politex pad. After completed rinsing the wafers were transferred to a cassette in the storage tank. After completing the batch, the cassette was transferred to an OnTrak cleaner, which utilizes brush scrubbing to further remove any particles.

In Paper VIII, where a bench-top machine was used, the plate with the mounted Suba 500 (Suba 500 was used since no pad conditioning is available for the bench-top machine) for the main polish pad was replaced with a plate where UR100 was mounted. The UR100 pad was rinsed with DI water when running the wafer. Thereafter, the wafers were cleaned in standard RCA1 and RCA 2 (always kept wet before final spin-dry). For metal CMP, the cleaning is somewhat different from post-oxide CMP cleaning, for instance Cu could corrode if ammonium is used. For further reading on post-metal CMP cleaning, consult Ref. [18].

3 Theory, modeling and fundamental experiments

In this chapter an overview of some theoretical, modeling, and fundamental experimental work on CMP is given. CMP is a rather complicated process to model. It contains chemical reactions as well a mechanical abrasive removal. Reactive species need to reach the wafer surface and react. This process could be reaction or diffusion limited. The process is complicated compared to wet etching by the fact that the slurry layer is turbulent and the presence of abrasive particles. The particles could enhance the reaction rate due to frictional heat as well as increase the diffusion since reactive species could adhere to the particles. The hydrodynamics is also important on a wafer scale in order to avoid depletion of reactive species before reaching the center of the wafer, which could cause nonuniformity. The particles are believed to remove a reactive surface layer. Therefore, the removal rate could be limited by the mechanical removal or the chemical reaction rate (which could be limited by transport or by kinetics).

The type of contact is important. Are the particles settled between pad asperities and wafer (i.e. pad and wafer in direct contact) responsible for the removal or is CMP a result (or a combination of) erosive wear by free particles impinging the surface? For removal by settled particles, the contact on particle scale is important. It could for instance be modeled as an elastic or plastic pad-particle and particle-wafer contact. The pad is rough and, therefore, only pad asperities are in contact with the wafer, which compress when applying pressure. The pad transfers pressure to the particle, which abrasively remove material from the wafer. Due to the compliant pad, the effect of applied pressure is more complicated to model than in abrasive wear, for instance grinding, where the applied pressure directly transfers to the load bearing area between the abrasive and the counter surface. Goals in CMP modeling on asperity scale are to understand how the applied pressure affects the direct pad-contact area and the pressure on the particles.

So far the issue of planarization has not been discussed. To understand this the pad-wafer contact is modeled on a feature scale. Important issues are to understand how pattern density, pitch and other layout issues affect the planarity of the surface. A further larger scale of contact modeling is on the wafer scale to understand how the CMP parameters affect the nonuniformity across the wafer. In this section some important work on modeling is

outlined, divided into chemistry, removal on particle and asperity scales, removal on feature scale, removal on a wafer scale, and hydrodynamics. Reference [99] gives a review on early CMP modeling work. Figure 5 describes the different scales.

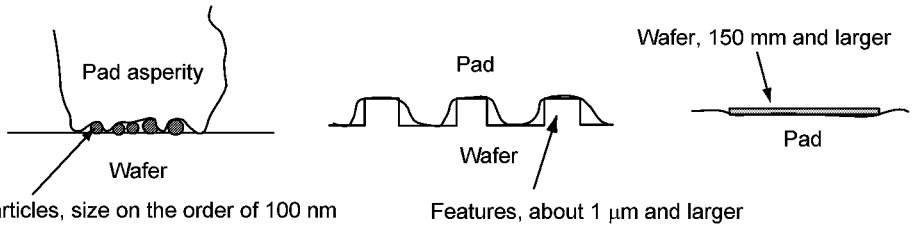

Figure 5. Different scales of modeling.

3.1 Chemistry and surface characteristics

The removal mechanism in glass polishing, which should similar to oxide CMP, has been explained by water diffusing under stress into the surface during particle indent affecting the silica structure.[63] Net removal occurs if depolymerized silica is removed either by the fluid layer or by being bound up by the polishing particle. Oxide CMP has been visualized as a two-step process involving release of substrate-derived species into solution (dissolution) followed by adsorption of these species by the abrasive particles.[100] Combining mass action equations for the complex formation reaction as well as protonation and deprotonation of surface hydroxyls present on the abrasive particles and massbalances of surfaces sites and dissolved species, it has been shown that the silicate adsorption concentration goes through a maximum as the point of zero charge (pzc) of the abrasive particles increases. Furthermore, it has been shown that the removal is at maximum when the pzc of the abrasive material coincides with the pH of the polishing slurry. Experimental results have shown that the oxide surface is more hydrophilic after CMP compared to as-deposited oxide,[101] indicating a higher surface density of surface hydroxyl groups on the polished oxide surface. FTIR, TEM, and X-ray reflectivity have recorded some surface modification of a near surface layer.[102, 103] The lower removal rate for nitride compared to oxide may be explained by hydrolysis of surface nitride monolayers being the rate-limiting step.[104] Understanding of the nitride CMP mechanism is important in the development of STI-CMP slurries.

For silicon CMP a microscopic model has been proposed which describes the process as a corrosive process where OH^-, H_2O, or O_2 dissolved in the slurry attack either surface Si-H bonds or upper silicon-silicon hydride backbonds.[66] The model is based on results from infrared absorption

spectroscopy and contact angle measurements. The removal rate peaked at around pH 11, where also the highest hydrophobicity and the maximum hydrogen coverage were obtained. Si(111) was monohydride-terminated, indicating atomically flat domains. Si(100) was terminated with a mixture of mono-, di-, and trihydrides, indicating an atomically rough surface. Away from the pH where the removal rate peaked, a higher concentration of hydroxyl groups was observed, increasing the hydrophilicity. At all pH, some oxidation beneath the H-terminated surface occurs evidenced by the presence of oxygen back-bonded hydrides. Similar conclusions regarding the surface chemistry have been drawn from X-ray photoelectron spectroscopy (XPS) and high-resolution electron energy loss spectroscopy (HREELS).[62] Electrochemical *in-situ* measurements during CMP of Si(100) have shown that anodic dissolution current is greatly enhanced with pad rotation compared to without, suggesting that the CMP mechanism can be considered as a sequential formation and removal of a film of complex hydrated silicates.[105] Cross-sectional transmission electron microscopy (TEM) has shown that Si(100) surfaces after CMP appear smooth without any subsurface defects.[2] Cross-sectional high resolution TEM (HRTEM) has shown that in fact a near-perfect Si(100) lattice is obtained after CMP.[106] The roughness of SCS surfaces after CMP has been measured to be 1-20 Å, depending on the specific CMP process and measuring technique.[62, 107-110]

3.2 Removal on particle and asperity scales

One often used formula to describe CMP is the empirical Preston Equation, $RR=KVP$, originating back to very early work on glass polishing.[111] RR is the removal rate, K is a constant, V is the relative speed, and P is the applied pressure. The equation states that the removal is linearly dependent on the on applied pressure as well as speed. Assuming elastic contact and spherical particles Preston Equation has been derived.[63, 112] In these models it was assumed that all the applied pressure was carried by slurry particles settled in between the pad and the wafer. The particles indent the wafer surface and remove material. The coefficient was dependent on elastic modulus and hardness of pad, wafer and particles. However, in CMP sublinear, for oxide[113, 114] and Al[93], proportional (prestonian), for polysilicon[36] and polymer low-κ material[115], and linear with non-zero removal extrapolating the fitted line to zero pressure, for Cu[90], dependence of removal rate on pressure has been reported. In Paper III, a sublinear dependence of removal rate on pressure for Si(100) is reported.

A paper that really provided a new view to understand sublinear pressure dependence was published by Shi and Zhao.[116] They recognized that when the pressure is applied the pad asperities deform, therefore there is a larger area that supports the applied pressure. They suggest that the applied

pressure controls the removal rate by the number of settled particles which is proportional to the contact area. Elastic theory suggested that the contact area is linearly dependent on $P^{2/3}$. They have also proposed a threshold pressure below which the particles roll in the wafer-pad asperity interface.[117] The rolling particles are not participating in the removal process.

Luo and Dornfeld have proposed very elaborate modeling, where they take into account the increased pressure each settled particle acts on the wafer.[50] They refer back to experimental results done by them or in literature. In their modeling, factors such as pad surface and material properties, abrasive size, distribution, and concentration are included. They assume elastic deformation of the pad asperities and plastic deformation over wafer-particle and pad-particle interfaces. Their model suggests a lower removal rate (assuming constant pad hardness) for a smoother pad (due to for instance pad glazing), which could be explained by less force on each particle. Assuming the ratio of real contact area to apparent contact area is the same (a softer and rougher pad could yield the same contact area as a harder and smoother pad) a softer pad gives a larger removal rate, since the active abrasive number is larger.

A higher removal rate for a softer pad has been found in silicon[118] and W CMP processes.[87] In oxide CMP, it has been found that the initial removal rate as well as the drop in removal rate without conditioning is larger for a softer pad.[119] The removal rate of oxide in alumina slurries for Cu CMP[89] and Al CMP[93] (in Al and Cu CMP stops on oxide) has been found to be larger using a harder pad compared to a softer, probably due to a more mechanical process.

A linear dependence without offset of removal rate on the speed could be expected since the length per time unit indenting particles travel and remove material is proportional to speed. However, sublinear, for oxide[113, 114] and Al[93], as well as linear, for Cu,[90] with non-zero removal extrapolating the fitted line to zero speed, dependence of removal rate on speed has been recorded. Paul has treated CMP as a combination of a number of processes with different rate constants.[120, 121] The processes include formation of complexes by surface reactions, dissolution of the complexes to the solution, mechanical removal of the complex and particles entering and leaving sites on the pad where pressure determines the number of sites. Thereby, a sublinear speed dependence could be understood from the assumption that the chemical reactions become more limiting for the removal rate at higher speeds.

The validity of the Preston equation depends on the pad. For W CMP, it has been found that using a soft Politex pad and a harder IC1400 the removal rate is sublinearly dependent and proportional, respectively, on the PV product.[87] Above, it has been mentioned of oxide CMP processes exhibiting sublinear dependence on both pressure and speed. However, it has also been reported on oxide CMP processes, where the removal rate is linearly

dependent on the PV product, with non-zero removal extrapolating the fitted line to zero PV.[49] The slope was dependent on the type of particles used, ceria gave the highest slope followed by precipitated silica and fumed silica.

The stationary contact area between pad and wafer for an IC1000 pad has been experimentally found to be less than 0.5 % of the nominal area.[71] The importance of pad asperities has been demonstrated.[55] The removal rate decreased with decreasing pad asperity heights.

Temperature increase during CMP, which could result from mechanical work, has been recorded and modeled for different CMP processes.[87, 88, 122-125] The increase, measured outside the wafer on pad using an IR camera or on the wafer directly using a temperature sensor, is in the order of 10-20°C. However, the local temperatures at wafer-settled abrasive contacts could be much higher.

3.3 Removal on feature scale

This scale deals with the planarization of patterned wafer, for instance in ILD planarization and STI-CMP. Intuitively, a small elevated feature is removed faster than a wider one. An isolated feature is removed faster than a feature in an array. Therefore, it is quite clear that the removal of up-features is dependent on the pattern density. One issue is how to determine the pattern density. Cleary, it should be some characteristic maximum interaction distance above which features at one site do not affect the removal of an up-feature on another site. Warnock presented a phenomenological model.[126] He associated the removal rate with a kinetic factor taking into account the slope of surface, an accelerating factor associated with points which protrudes over the surface and a shading factor describing of how elevated features around a point decrease the removal rate. Sivaram et. al. have modeled pattern sensitivity using pad bending.[45, 127] Chekina et. al. have modeled removal on a feature scale using contact mechanics.[128]

A group at MIT has done very interesting work deriving a more analytical description on removal on feature scale. They call the maximum interaction distance "planarization length". In the initial MIT model, only up-areas were assumed to be contacted, i. e. pad was perfectly rigid. The removal of up-areas was modeled to be inversely proportional to the effective pattern density. Using a test mask, measuring the thickness for different pattern densities after polishing the interaction distance could be obtained. Initially a uniform weight square window was used to calculate the effective pattern density.[129] However, recognizing physical characteristics of pad bending a circular elliptic weighting function was used.[130] The planarization distance is dependent on process parameters. A harder pad and lower pressure gives a larger length. Therefore, if the process is changed a new planarization

distance has to be derived. After the planarization distance is derived using a test mask, the effective pattern density of a real production mask could be obtained by layout biasing (taking into account deposition profiles), local discretized density evaluation, and effective density evaluation using the weighting function (determined by planarization length).[131] Then, the planarity after CMP could be predicted for the production mask. The predicted planarity could be used in the placement of a dummy pattern or to optimize the process in terms of how thick oxide that has to be deposited. MIT test masks are now widely used to characterize CMP processes.

The pad is not perfectly rigid. Very early in CMP research for planarization it was found that the step height exhibits a logarithmic dependence on oxide removed for features wide enough that the pad contacts the down area, and a nearly linear dependence for narrow features where the pad does not contact down areas.[132] Burke found that down area removal rate, D^o, normalized to the rate of a large up-area, is linear, for $D^o>0.3$, and logarithmic, for $D^o<0.3$, dependent on step height.[133] He also provides equations to fit the results.

A very clarifying paper on step height reduction based on pad substrate interactions has been published by a group at IMEC.[134] At a sufficiently large step height when the pad does not contact down areas, the removal at down areas is limited to chemical dissolution. The step height reduction should then be linearly dependent on the polish time. At some point in time the pad will also contact the down areas and down area abrasive removal starts. However, the down area abrasive removal should be smaller compared to up-feature since the effective pressure is lower. Assuming that Hookes´s law applies, i.e. that pressure is linearly dependent on pad deflection, and that removal is linearly dependent on pressure, an exponential decrease in step height with time can be derived. Polishing experiments using IC1400 pad indeed showed linear and exponential dependence of measured step height on polish time, indicating two different contact modes (non-contact and contact of down area). The IMEC step height model has also been incorporated with the MIT pattern density model with good fit between the combined model and experiments.[135]

In Paper VI, an exponential dependence of step height on polish time is shown for a Politex pad, indicating that the pad contacts the down area from the beginning. Similar results have also been found for a felt type pad, SubaIV.[136] Step height reduction depends on the process parameters. The step height ratio, the ratio post- to pre-polish step height (lower ratio for a more planarizing process), increases with pressure and decreases with speed.[113] The state of the pad also affects step height reduction. Without pad conditioning, planarization efficiency (defined as the step height reduction per unit removed oxide on up-area) increases with use.[53] However, as described in section 2.2, the removal rate decreases at the same time.

3.4 Removal on wafer scale

Model removal on a wafer scale is important to predict the within wafer nonuniformity. The distribution of stress across the entire wafer surface depends on down pressure, pad compressibility and carrier film compressibility.[137] There is a sharp increase close to wafer edges, which correlates an enhanced removal rate. Further modeling has taking into account the effect of the retaining ring in the Mirra tool on the wafer scale stress distribution.[138] Others have investigated the redistribution of the pressure profile across a wafer induced by wafer bow due to film stress.[139] If the head and plate angular speed are the same analysis has shown that the relative velocity for points on the wafer are the same.[136] By changing the ratio, the relative velocity oscillates for each point on the wafer (except the absolute center point).[140] This oscillation increases from the center point of the wafer out to the edge. The average velocity also differs, increasing from the center of the wafer and out.[141]

3.5 Slurry flow

So far, models to describe pad-wafer contact on different scales have been discussed. This section discusses the slurry flow. Slurry flow is important to understand slurry depletion effects which could cause nonuniform removal across the wafer, to understand if the slurry affects the pressure the pad exerts across the wafer, in the most extreme cases it could even be speculated that the slurry totally separates the pad and the wafer.

The first work on hydrodynamics was published by Runnels.[142] Three dimensional Navier-Stokes equations for an incompressible Newtonian flow with constant viscosity were used. Finite element methods were used to solve the equations. It was assumed that both the wafer and the pad were smooth and rigid. The wafer was assumed to be curved. In further papers the flow and stress due to a fluid layer was considered on a structured wafer.[143, 144] These papers treat removal on a feature scale. However, the physical motivation, erosive removal by free particles in the slurry, is different from the models in section 3.3 which assume direct pad wafer contact (abrasive removal by settled particles).

To increase the understanding, there is a drive to derive more analytical solutions for slurry flow characteristics and couple this to experimental results. In one of the later works on hydrodynamics, it has been recognized that, since the Reynolds number is very small, lubrication approximation for sliding bearings is valid.[92] Both pad and wafer were considered smooth. Deflection of the pad under the wafer was taken into account. See references therein on other modeling work on CMP hydrodynamics. Two different slopes in the normalized removal (removal per traveled distance) plotted

versus ratio of pressure and relative velocity is explained by different modes of contact: direct contact and hydroplaning. However, others have measured a subambient pressure between the pad and a work piece (plate with drilled holes and pressure sensors), which could be understood from the fact that there is a wider diverging space between the work piece and pad compared to converging.[145, 146] Therefore, it was argued that the fluid layer works to further press down the wafer against the pad asperities. The pressure measuring assembly was stationary. By measuring the friction for a rotating work piece compared to stationary it was concluded that rotation increases the suction pressure.[146] Others have measured the pressure directly for a rotating work piece, and concluded that the fluid layer helps to carry the load.[147]

The pad surface has also been modeled as a grid of cells.[91] This model is physically motivated by the fact that a pad consists of pores (planarization pad such as IC1400) of fibers which bend (felt pad, Suba 500). Before a cell enters below the pad the slurry chemical concentration is assumed to at maximum. When the cell then travels below the pad the slurry chemicals react with the wafer surface and the cell is depleted. The supply of chemical to the wafer surface for a cell is dependent on the slurry velocity field within the cell, which is treated in the modeling. Slurry entrainment rates investigated using fluorescence and test equipment for which all input variables were scaled with the same factor compared to an industry CMP machine.[148, 149] The entrainment rate was dependent of process settings, type of pad and type of conditioning (ex-situ or in-situ).

4 Shallow trench isolation, emphasizing on STI-CMP issues

In this section shallow trench isolation (STI) is discussed. Paper VII describes development of a shallow and deep trench process module for BiCMOS/bipolar processes. In this section general STI is discussed. STI-CMP issues are treated more in depth. Even though the discussion is restricted to STI-CMP the reader is here introduced to many terms common to several CMP processes, such as dishing, erosion, dummy pattern, etch back to enhance CMP and uniformity.

STI has several advantages compared to LOCOS, such as increased lateral control, better planarity and a reduction of parasitic capacitances. STI gives the possibility to apply tighter design rules, to have a higher packing density, and to increase the field oxide thickness. Realization of the STI is outlined in Fig. 6.

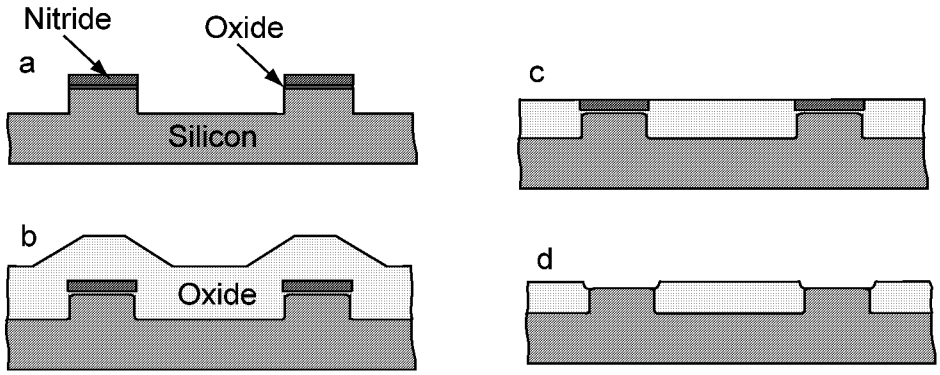

Figure 6. Realization of STI: (a) growing thin oxide, nitride deposition, patterning (lithography and etching) nitride/oxide stack, etching of shallow trench; (b) nitride undercut, liner oxidation, deposition of oxide; (c) removing excess oxide by CMP, stopping at nitride; (d) wet etching of nitride and pad oxide.

The shallow trench process starts by growing a thin oxide (called pad oxide) about 10-20 nm thick. Thereafter about 100-200 nm thick nitride is deposited. The nitride is opened by dry etching, the photoresist is removed, and the silicon is etched to a depth of about 500 nm (in reference to the silicon surface). Often a sacrificial oxidation is performed to remove etch

damage. One important issue in STI is corner rounding of the upper corners. Otherwise, a parasitic corner transistor with a lower threshold voltage, distorting subthreshold characteristics, due to an enhanced field from gate poly wrap around could be present. To enhance corner rounding the pad oxide could be etched back from the upper corner before liner oxidation.[150] Other schemes for corner rounding have been proposed.[24] After corner rounding, oxide is deposited to fill the shallow trench. Several different deposition methods have been used.[24] High density plasma chemical vapor deposited (HDP-CVD) oxide exhibits low HF etch rates even without densification.[151] Densification could result in defects in the silicon due to difference in thermal expansion between oxide and silicon. Low etch rates of the filling oxide are important to avoid poly wraparound in the etching and cleaning steps in the end of STI processing. Also, this deposition method gives good gap filling, even for narrow trenches. This is a result of a simultaneous sputtering during deposition. Thereby, species at corners are sputtered off, giving a void free filling. In an HDP-CVD equipment, the plasma is inductively coupled, usually by a coil around the source chamber. The potential on the chuck is independently controlled from the source.

After filling, the excess oxide is removed by CMP (before the use of STI-CMP etch-back has been employed with less planar result). The CMP is stopped at the nitride. Some overpolishing, to ensure that all nitride areas are cleared from oxide is always necessary. The removal of nitride on active area is denoted erosion (erosion has previously in this thesis had the meaning of free impinging particles, the common use in tribology). Controlling nitride erosion is very important, since remaining nitride determines the step at the edge of active area up to the field. The oxide thickness at the corner after removal of the pad oxide and sacrificial oxidations depends on this step. Therefore, nitride erosion control is of great importance to avoid poly-wrap around and the parasitic corner channel. A nonuniform STI-CMP process could result in varying erosion, result in differing transistor characteristics across the wafer due to differences in the appearance of the corners.

Due to flexibility of the pad a bowed surface in the field oxide occurs (similar phenomena occurs in metal damascene CMP). Dishing, a measure to describe this bow, is usually defined as the height difference between the lowest point of the field oxide surface and the top of the nitride surface. Dishing depends on trench width, and gets larger for wider trenches.[152] The dishing results in nonplanarity and a nonuniform field oxide thickness. Figure 7 illustrates the dishing and erosion.

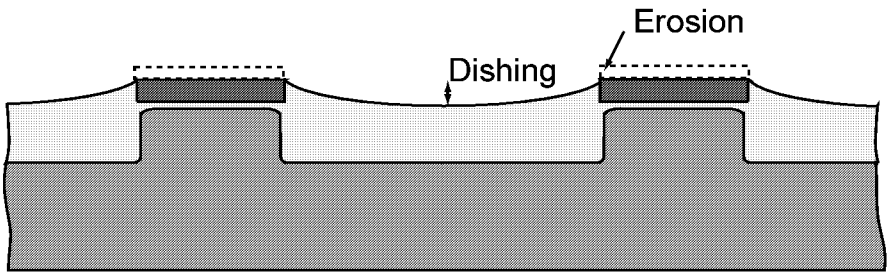

Figure 7. Dishing and erosion.

To avoid excessive dishing a dummy pattern can be employed to make the pattern density more uniform and to reduce the maximum trench width, as shown in Fig. 8a.[24, 153] However, the draw back of this approach is that it increases capacitive coupling to the substrate. This could be especially detrimental if the dummy pattern is autogenerated, giving capacitances not accounted for by the circuit designers, especially important in mixed signal IC:s. Another common approach to alleviate for the STI-CMP is to use reverse mask, see Fig. 8b.[24] It is an autogenerated mask which is the reverse of the active area mask, adjusted so the openings in the reverse mask is slightly smaller than the active area. By using this method less oxide has to be removed, only "spikes" at active area edge need to be planarized which is beneficial since the polish rate is faster for narrow features. The total STI-CMP time can be reduced, and the time difference between the point were nitride starts clearing and the point when all nitride cleared is reduced, which decreases nitride erosion and dishing. One drawback of a true reverse mask process is that dense areas of narrow features will not receive any etch back (the revere mask openings need to be smaller than active area. This has been accounted for by etching narrow pillars in those regions.[154] This issue is important if conformal deposition process is used, i.e. not for HDP-CVD oxide. Nitride overlayer, patterned[85] or blanket[153, 155, 156] has also been used to enhance the results for the STI-CMP, Fig. 8c. For patterned overlayer, the nitride on top of the deposited oxide on active area is removed. Another method is reverse etch-back, Fig. 8d; a block resist is patterned in the field regions, a second resist layer is spin-on, which follows by an etch-back stopping in the oxide.[25]. The spin-on and etch-back has also been applied twice.[157] By using reverse etch-back, a larger tolerance can be allowed in the placing of the counter mask.[158] The main drawback of the reverse mask, reverse etch-back and nitride overlayer is that it adds process steps increasing the cost. There is a drive to implement STI-CMP without any of these cost adding approaches as well as a dummy pattern, i.e. to develop direct STI-CMP processes.

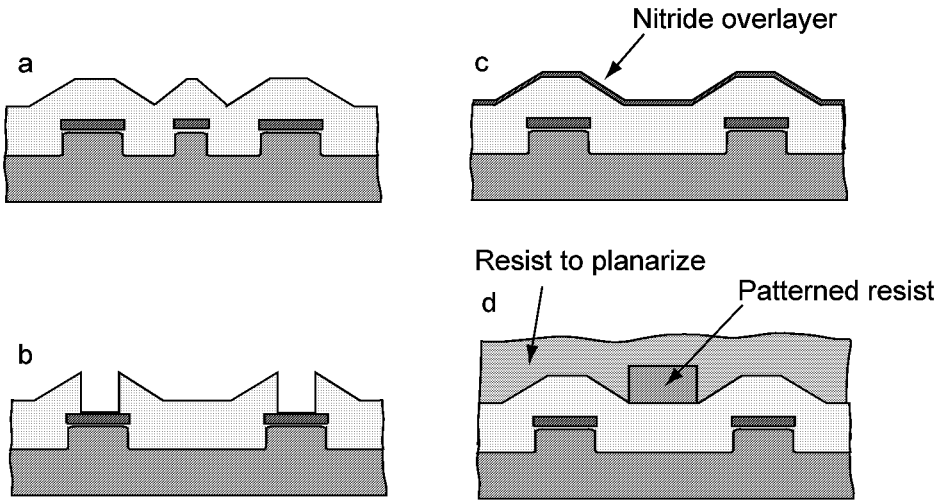

Figure 8. Methods to alleviate the STI-CMP: (a) dummy pattern, (b) reverse mask, (c) nitride overlayer (for patterned overlayer, the nitride overlayer on active area is removed before CMP), (d) reverse etch-back: a block resist is patterned in the field regions, a second resist layer is spin-on, which follows by an etch-back stopping in the oxide.

Conventional slurries (which are mostly used, as in paper VII) have only a selectivity of 3-4. As has been discussed HSS has been used for STI-CMP to reduce nitride erosion.[77-79] It has been reported on oxide-nitride selectivity consistently more than 100 varying down force and speed.[78] The uniformity across the wafer can be enhanced, since less nitride is removed in the overpolishing to account for nonuniform removal across the wafer. However, HSS could cause more dishing. Therefore, a dummy pattern had to be employed in wide field regions to avoid excessive dishing.[78] Also, agglomeration of particles causing defects on the wafer is also an issue.[78] However, recently direct STI-CMP processes (without a dummy pattern) using HSS with better performance than reverse mask silica slurry STI-CMP have been developed to be implemented in production.[79]

With the introduction of CMP the flatness of the wafer has become more important. Random nonuniformites after CMP is often attributed to nanotopography, which is height variations of up to 100 nm on a length scale of 0.2-200 mm.[159] Nanotopograhpy depends on the wafer manufacturing processes, i. e. slicing, grinding/lapping and prime wafer polishing.[3] The nanotopographical "hills" on a wafer receive a higher CMP removal rate, which result in a thinner film thickness at those areas. A signature match for blanket wafers between nanotopography and oxide thickness after CMP has been recorded.[160] As would be expected, a softer pad gives a more uniform oxide thickness, i.e. the nanotopography has a smaller effect since the pad conforms more to the surface. However, using a soft pad gives a low

planarization rate. Spatial power spectral densities of nanotopography and oxide thickness variation have been analyzed and a transfer function has been proposed.[161, 162] Longer wavelength nanotopography has less effect on post-CMP oxide thickness nonuniformity since pads conforms more to longer wavelengths. A harder pad, which conforms less than soft, increases the effect for longer wavelengths. The power spectral density analysis of the nanotopography has also been used to compare 8" single side polished wafers subjected to different prime wafer etching and polishing processes.[163] By avoiding wax mounting and using an etch before polishing, the nanotopography could be reduced. The combined effects of nanotopography, CMP process imposed nonuniformity and deposited thickness nonuniformity have been correlated.[164] The effect of nanotopography is of particular concern in STI-CMP process. To ensure all oxide on nitride is removed (otherwise, the nitride will be masked in the subsequent wet nitride removal), a prolonged CMP has to be employed due to nanotopography. This will give a larger variation in trench dishing across wafer (giving variation in capacitances and nonplanarity) and nitride erosion. As has been mentioned, nitride erosion control is of great importance to avoid parasitic corner channel. Modeling work has been done on the effect of nanotopography in STI-CMP.[159] This could be used to predict the effect of a known nanotopography on dishing and nitride erosion, which can reduce the effort in process development to decrease the effects.

5 Summary of papers

Paper I

Effect of dopants on chemical mechanical polishing of silicon

In this work, the effect of wafer properties on the CMP removal rate of single crystalline silicon (SCS) is investigated. A high boron concentration decreases the removal rate. A high phosphorus concentration from a long diffusion increases the removal rate. Figure 9 shows the removal for 20 min of CMP for Si(100) wafers diffused with boron and phosphorus, respectively. There was a small difference in the reference polish step (wafer not subjected to diffusion), which could be attributed to the pad being more soaked with slurry during the last reference step. Wafers for which only isolated areas are diffused (rest of the area were covered by an oxide mask during diffusion) were also investigated. For a patterned boron diffused wafer, it is clearly seen that the diffused areas elevate above the surroundings during polishing, Fig. 10. It is speculated that the reduction in removal rate for high boron concentrations could be explained by an enhanced recombination of electrons, similar to a common explanation for the boron etch stop in alkaline etchants.[165] For phosphorus, it is suggested that chemical reaction rates increase due to the strain in the lattice. Also, the effect of crystal orientation was investigated. It was found that Si(100) has a higher removal rate than Si(111).

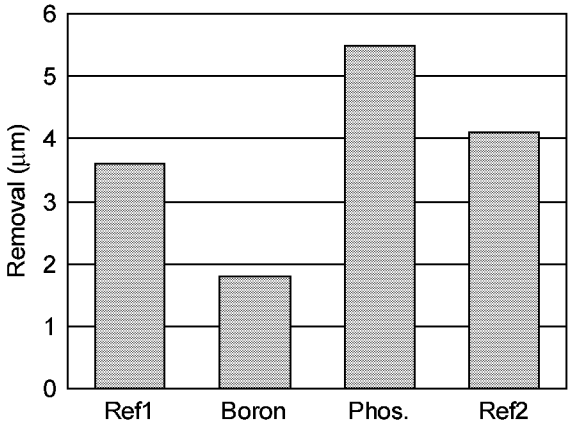

Figure 9. Removal for 20 min polishing of a reference (polished first and last), boron and phosphorus diffused Si(100) wafer.

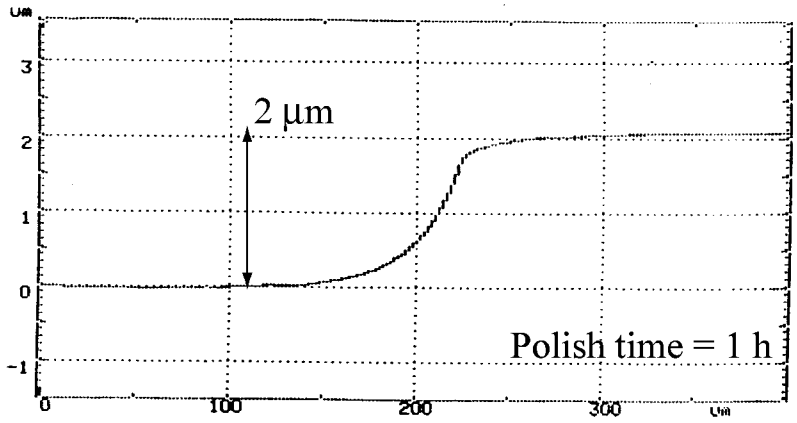

Figure 10. The boron diffused areas elevate above the surroundings during CMP.

Paper II

Effect of Diffused Boron and Phosphorus in Si(100) on Chemical Mechanical Polishing Removal Rate

In this paper the results of the effect of diffused boron and phosphorus on Si(100) removal rate first presented in Paper I are extensively discussed in conjunction with findings in the literature. Simulated doping profiles, reasonable confirmed by four-point resistivity measurements are included, Fig. 11. These profiles clearly show that only highly doped silicon is removed. The discussion is based on findings that during CMP of Si(100) the anodic dissolution current is greatly enhanced with pad rotation compared to without,[105] the surface is hydrogen terminated after CMP and that the decrease in removal rate above pH 11-12 is due to formation of a thin (sub)mono oxide layer,[66] the CMP removal rate increases with both boron and phosphorus concentration, concentrations in the order of a couple of wt%, in deposited silicate glass films.[166] Reduced etch rates in KOH for highly boron and phosphorus doped Si(100) have been attributed to spontaneous passivation producing a thin oxide-like layer or formation of a prepassive layer, respectively, which are possibly caused by strain due to the dopants.[167, 168] Boron has a much larger effect on etch rate than phosphorus.

The decrease in removal rate for boron diffused Si(100) is believed to be a result of complementary effects of paths towards oxide formation as well as a reduced surface reaction rate due to enhanced electron recombination. The last point was proposed in Paper I. The increase for phosphorus diffused Si(100) is believed to be an effect of an enhanced surface reaction rate. The effects of dopants on the Si(100) removal rate is probably not due to the direct presence of dopant in a formed surface layer.

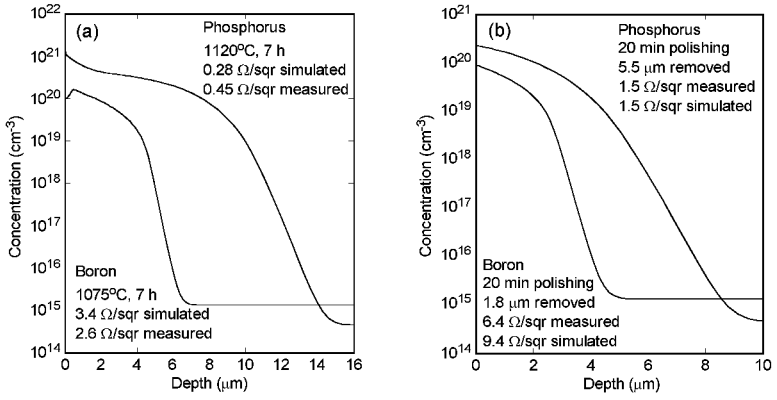

Figure 11. Simulated diffused profiles (a) before and (b) after polishing. The measured and simulated sheet resistivities agree reasonably well.

Paper III

Effect of Process Parameters on Material Removal Rate in Chemical Mechanical Polishing of Si(100)

The effect of process parameters, such as speed, pressure and slurry concentration, on the Si(100) removal rate is investigated. Even though CMP of SCS has been used for a long time, not that many reports on this topic have been published and, therefore, not that much removal rate data is available in the open literature. Previously, the effects of varying pH[66] and using different pads[118] have been investigated. In contrast, for polysilicon, oxide, low-κ, Al, Cu, and W CMP there are several reports on this subject, some of them discussed in section 2.2 and 3.2. SCS CMP has found many new applications recently outside prime wafer production, which increases the need and interest to investigate the influence of process parameters on the removal rate. It is found that the removal rate increases sublinearly with pressure, speed, and silica concentration.

Figure 12 shows the dependence of plate speed. There is a rapid increase in the removal from zero speed to 8 rpm (this was the lowest possible speed setting for the machine). It is suggested that at low speeds the mechanical removal of a chemically reacted surface is rate limiting. After silicon CMP, surfaces are hydrophobic hydrogen terminated as reported from separate laboratories.[62, 66] Therefore, the mechanism is probably always limited by surface reactions for practical silicon CMP processes. Otherwise, it would not be likely that different silicon CMP processes would give similar results regarding surface chemistry. The removal rate increase, after the rapid increase at low speeds, could be understood from the fact that the mechanical input energy increases which transforms to some extent to frictional heat which enhances the surface reactions.

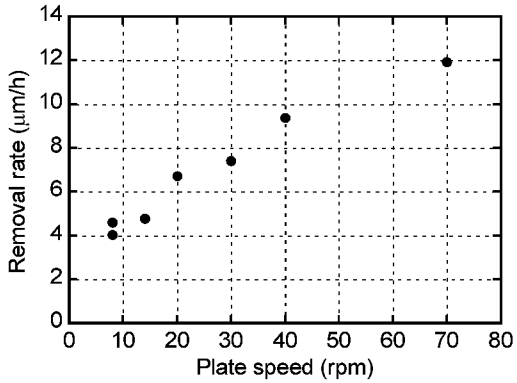

Figure 12. Si(100) removal rate as a function of plate speed. pad: Suba 500, slurry: Rodel 1520 1:15, pressure: 94 g/cm^2, roller arm sweep: 7 sweep/min except for the lower point at 8 rpm where there was no sweeping, mounting method: wax.

Paper IV

Silicon surfaces for hydrophobic wafer bonding

The objective of this work was to study how the Si crystal growth technique, FZ or CZ, affects the bondability of silicon wafers. The FZ and CZ wafers were from different vendors. Bonding wafers directly from the box (after cleaning), it is most likely that other differences in wafer manufacturing apart from the crystal growth could affect the bondability. Therefore, material is removed before bonding using lapping, etching, and polishing (stock removal and final polishing) in our laboratory. Furthermore, it is interesting to investigate if the polishing processes in our laboratory affect the bondability compared to wafers directly from the box and cleaned. Also, the effect of omitting etching was examined. Eight wafers were investigated, CZ and FZ wafers i: from the box, ii: polished, iii: lapped, polished, and iv: lapped, etched, polished. The wafers were cleaved into four quarters each. Two quarters were bonded and the bonding energy was measured using the crack opening method, and one of the other was used for AFM.

The results from the AFM measurements were presented as a surface scan, R_{rms}, R_a, peak-to-valley, and line trace Fourier spectrum. R_{rms}, R_a, and peak-to-valley do not give any information of the spatial frequencies of the surface. Assuming that the surface is very "spiky" (dominating spatial frequencies high) it could be argued that the "spikes" deform plastically, which results in a large direct contact area and, subsequently, in a strong bond. On the other hand, if the dominating spatial frequencies are sufficiently low, it could be argued that the wafers deform elastically, resulting in the surfaces conforming to each other and a strong bond as well. From this discussion, it is most likely that the spatial frequency of the surface should have an effect. Therefore, in order to give information about the spatial frequencies, Fourier spectrum of AFM line traces is also included, as has been proposed previously.[169] It was difficult to draw any definite conclusions from this limited study. No correlation between the bondability and Fourier spectrum was seen. It was clear, however, that omitting the etching step after lapping degrades the bonding.

It is argued in the conclusions in Paper IV that the results could be explained by a higher impurity concentration for CZ could help relax the Si lattice. However, it is most probably the other way around; interstitial oxygen in CZ appears to have strain hardening effects and serves as obstacles for dislocation initiation and propagation.[170] The surface of wafer from the box and of a wafer polished using the bench-top machine is quite similar, Fig. 13. This indicates that a low surface roughness can be achieved using the bench-top machine. The author to this thesis believes that this paper, even though the results as well as the discussion are somewhat

inconclusive gives valuable information to this thesis concerning surface characteristics.

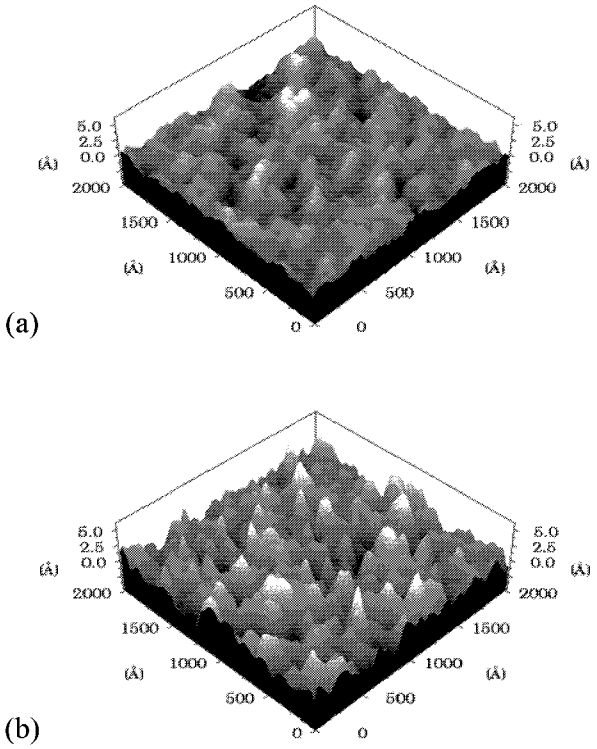

Figure 13. AFM of FZ-wafer; (a) from the box, (b) polished in two steps using Suba 500 pad/ Rodel 1520 1:15 slurry and UR100 pad/LS10 slurry.

Paper V

InP and Si Metal-Oxide Semiconductor Structures Fabricated Using Oxygen Plasma Assisted Wafer Bonding

InP offers several interesting properties for MOSFET, such as a high electron mobility and saturation velocity. However, it has been proven difficult to form high quality insulators on InP. Thermal, anodic and plasma growth, various depositions processes, as well as deposition in combination with growth have been employed. The main issue is that the formation has to be done at relatively low temperatures to avoid thermal decomposition of the InP.

In this paper, InP metal-oxide-semiconductor (MOS) structures are fabricated by transferring SiO_2, dry thermally grown at 1000 °C, to InP from oxidized Si wafers using oxygen plasma assisted wafer bonding followed by annealing at either 125 °C or at 400 °C. By exposing InP and Si wafers to oxygen plasma, it has previously been shown that annealing at temperatures as low as 125 °C is sufficient to get a strong bond. A low-temperature bonding process is desirable because, apart from the InP decomposition, with increasing temperature the defect density increases due to the large difference in thermal expansion coefficient. After the bonding process, the excess silicon was removed by wet etching and MOS capacitors were formed by depositing metal contacts on the front and backside. Well-defined accumulation and inversion regions in recorded capacitance-voltage (C-V) curves were obtained, Fig. 14. The long-term stability was comparable to what has been previously reported. It should be noted that the comparison PECVD sample in the stability measurement did not receive any anneal (an suggested annealing is 1 h at 300°C under O_2). Most probably, the stability of the PECVD sample would then be comparable to the bonded results. The structures exhibited high breakdown fields, equivalent to thermally grown SiO_2-Si MOS structures. The transferring process was also used to fabricate bonded Si MOS structures to learn more about the process. Wet activated wafer bonded InP MOS structures have been used in formation of optically controlled Si MOSFETs.[171] This further motivates our study of oxygen plasma assisted wafer bonded InP MOS structures, which could be a possible mean to decrease the annealing temperature in the process.

CMP is applied in thinning and to create bondable surfaces in the manufacturing of bonded silicon on insulator (SOI) materials. Bonded SOI is an example of layer transferring process, in which a silicon layer is transferred to an oxidized silicon wafer. The author thinks this paper gives an opportunity to include an example of layer transferring process, even

though CMP was not applied in thinning. In many other such processes, CMP plays an important role.

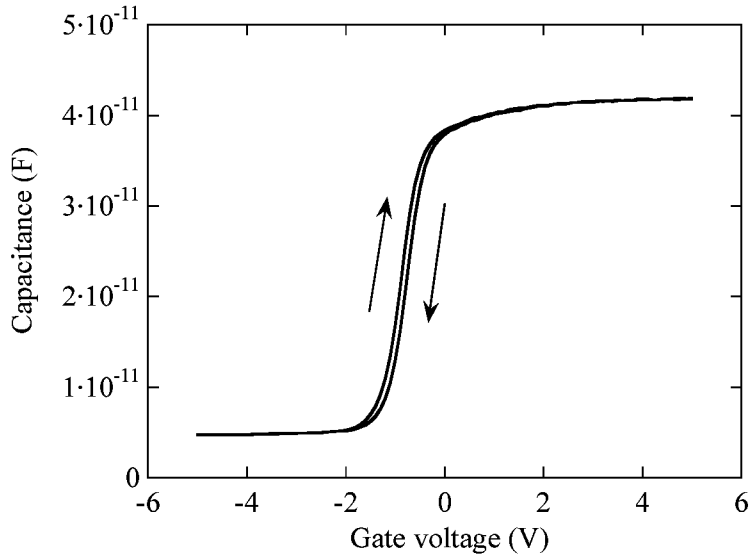

Figure 14. CV curve of bonded InP MOS structure annealed at 400 °C.

Paper VI

Chemical Mechanical Polishing for Surface Smoothing

Most work regarding the evolution of feature profiles during CMP has been emphasized on planarization using pads with a hard top pad (stacked IC1000/Suba IV or IC1400 (IC1000 on a foam base pad)). The hard top pad planarizes and the softer bottom layer decreases the nonuniformity across the wafer. Several papers describing feature profile change using these pads have been published. However, in this paper the evolution of feature profiles during polishing is investigated using a soft Politex pad, which is often used in the rinsing or buffing step after the main CMP step. Possible applications could be to create rounded structures for microoptical devices or corner rounding to reduce stress in microstructures. Surface profile evolution during CMP of both inlaid and protruding pattern of line arrays completely etched in silicon dioxide is investigated. It is found that there is an exponential dependence of the step height in the arrays on the polish time. Also, wide silicon areas were open through the silicon dioxide. It is found that the soft pad polishes the open silicon areas. Due to the selectivity of the slurry between silicon and oxide, the step height increases even though the silicon areas are situated below the oxide, as shown in Fig. 15.

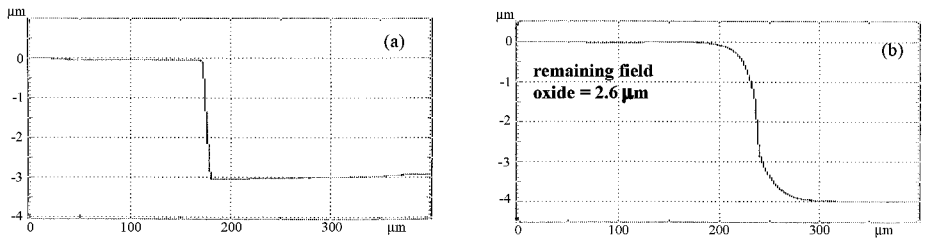

Figure 15. Etched step in oxide down to silicon (a) before and (b) after polishing using a Politex pad.

Paper VII

A Shallow and Deep Trench Isolation Process Module for RF BiCMOS

A complexity in high-performance RF BiCMOS processes is the integration of STI with deep trench isolation (DTI). DTI gives a smaller collector-substrate capacitance compared to junction isolation. A process module to realize STI/DTI is presented.

Shallow trench is etched prior to deep trench. Thereby, if desired, the deep trench could be placed self-aligned to the shallow trench edge. A new feature is the introduction of a CMP step to planarize the polysilicon deep trench filling before etch-back. The recess into deep trenches is decreased and polysilicon spacer formation at active area edges is avoided. The step height is reduced and only very limited additional amount of oxide had to be deposited in the shallow trench filling to account for deep trench recess. The poly CMP is stopped before all polysilicon on active area is removed, to avoid polysilicon dishing and erosion of oxide on top of nitride on active area. Two different slurries were evaluated for the poly CMP, a conventional slurry for oxide CMP (SS12), which is used for the later STI-CMP, and a slurry designed for poly CMP (EPP1000). The latter slurry gave a higher uniformity in polysilicon removal. For the SS12 poly CMP processed wafers, the nonuniformity transfers down to a recess in deep trench but, however, the results are better than not applying poly CMP at all.

HDP-CVD was used for shallow trench filling. Less oxide needed to be deposited for the wafers which were subjected to poly CMP using EPP1000. As rule of thumb, the oxide surface in shallow trench should be about 150 nm above the level of the nitride surface after deposition. Furthermore, less oxide removed in the CMP step reduces the effect of a nonuniform removal across a wafer. A direct STI-CMP process end pointed using ISRM was developed. A solo pad was tried but the effect of nanotopography was evident as a blotchiness of the wafer. Therefore, a conventional stacked pad was used. Oxide thickness in shallow trench, remaining nitride on active area and dishing in wide trenches were recorded. It was indeed found that the wafer subject to poly CMP using EPP1000 gave the best results. Figure 16 shows a completed STI/DTI structure. It was decided to use a special slurry for poly CMP even though it resulted in the use of two different slurries in the module. Several lots of a bipolar mask set using direct STI-CMP have been processed. However, switching over to a BiCMOS mask set, reverse mask was implemented to increase the STI-CMP process window.

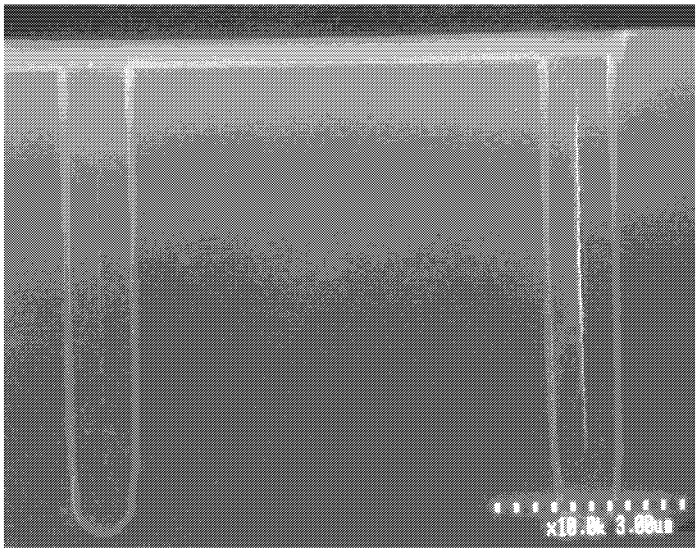

Figure 16. SEM of structure after STI-CMP. Sample polished with EPP1000 poly CMP process followed by deposition of 800 nm HDP-CVD oxide.

Paper VIII

A Base-Collector Architecture for SiGe HBTs using Low-Temperature CVD Epitaxy Combined with Chemical-Mechanical Polishing

In Paper VII, the transistors have a conventional collector architecture. The final collector doping is implanted after formation of the emitter opening. Therefore, the region with the collector doping becomes self-aligned to the emitter, which reduces the base-collector capacitance. This increases the maximum oscillation frequency, f_{max}, an important figure of merit for high-frequency transistors.

In Paper VIII, a collector architecture for SiGe HBT based on low temperature in-situ doped selective growth and CMP is introduced. A better doping control can be achieved on the expense of a non-self-aligned collector doping. Furthermore, implantation through a strained SiGe base is avoided. The collector is grown through an opened hole in the field oxide. SEG is used to avoid nucleation on the sidewalls. There is a trade-off in deposition temperature. A lower temperature gives a better dopant control and less stress from the sidewalls due to difference in the thermal expansion coefficient between the silicon and the oxide, which could cause defect generation. However, a lower temperature also results in a lower deposition rate. During growth, phosphorus segregates to the surface. CMP is used to remove the segregated phosphorus and to planarize the surface. If not removed, the segregated phosphorus will spread into the collector during subsequent process steps and the doping control is not retained.

This SEG-CMP is much less demanding than STI-CMP, because the active areas are much narrower than the field areas. A felt type pad could be used which is not prone to glazing. Also, there is a high selectivity between silicon and oxide. Therefore, oxide erosion was not critical. The SiGe base is grown by non-selective epitaxy because an extrinsic poly base is needed to contact the intrinsic epitaxial base. Figure 17 shows the surface (a) after SEG, (b) after CMP, and (c) after SiGe growth. A high planarity is achieved. Crystalline SiGe with exceptional surface morphology could be grown on the SEG after CMP. Working devices based on the SEG collector/CMP scheme proposed in this paper have been processed.[172]

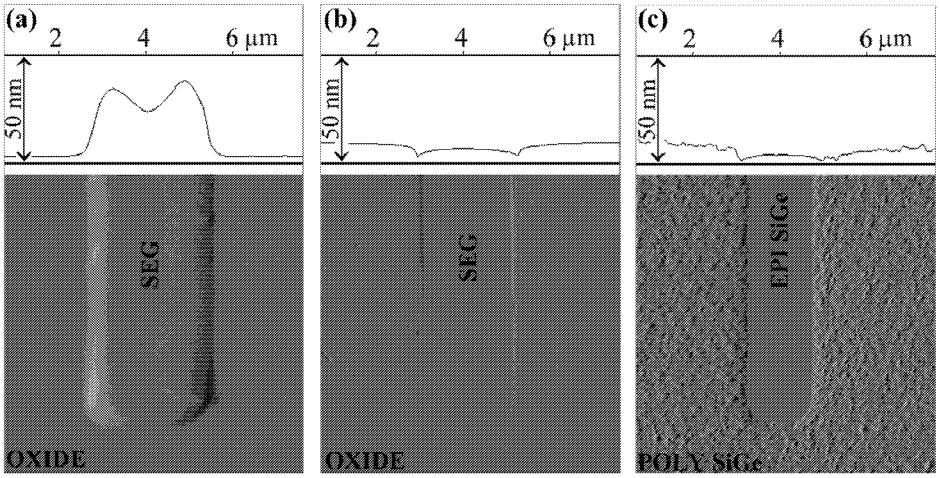

Figure 17. The surface: (a) after SEG of the collector, (b) after CMP, (c) after base SiGe epitaxial growth.

Paper IX

Geometrically Defined All-Diamond Abrasive Surface for Pad Conditioning in Chemical Mechanical Polishing

There is lot of work by manufactures of pad conditioning tools to create tool with ever increasing control of the diamond placement, protrusion, size, and so on. The goal is to obtain a conditioner which provides a CMP process which gives a sufficient removal rate, planarity, uniformity and defect density on the wafer. At the same time the wear of the pad should be low since pad removal with subsequent requalification takes time. Nowadays a pad needs to be changed once a day in production.

In this work, a geometrically defined abrasive surface for pad conditioning in chemical mechanical polishing is introduced. The all-diamond abrasive surface is formed by hot filament chemical vapor deposition (HF-CVD) of polycrystalline diamond onto a lithographically patterned and anisotropically etched silicon wafer mold. After electroplating a metal backing, the silicon is removed. Thereby, the diamond surface has replicated the silicon surface. An initial test shows that the fabricated sharp diamond tips endured a 1 h run on a glazed pad, as shown in Fig. 18. Less than 0.5% of the tips were damaged. The load-specific wear-rate, which is the removed volume divided by sliding distance and applied force, was calculated to be 0.31 $mm^3m^{-1}N^{-1}$. Figure 19 shows a scanning electron microscopy picture of an abraded pad, displaying the high roughening capability of the diamond tips.

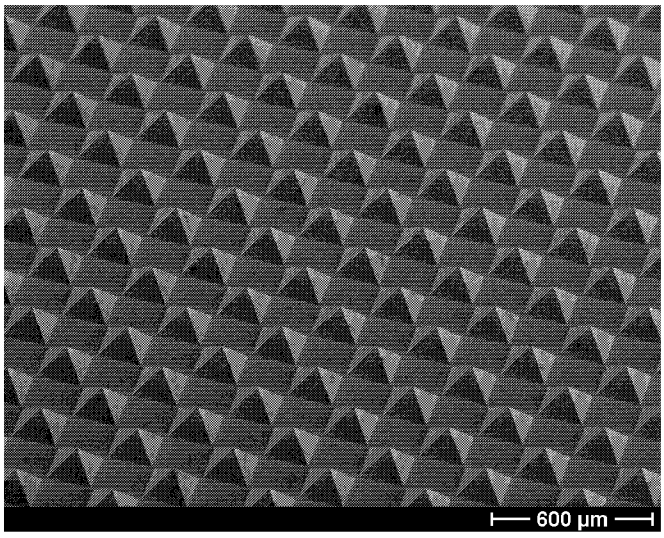

Figure 18. Overview of tips after abrading an IC1400 pad.

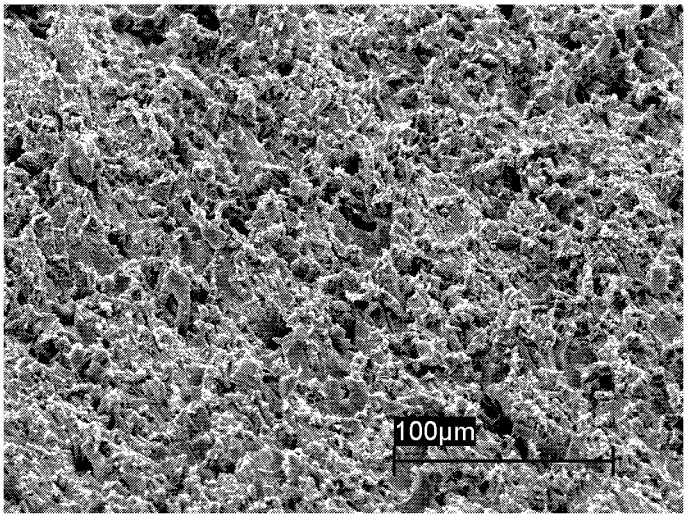

Figure 19. Abraded IC1400 pad surface using the replicated diamond abrasive surface.

6 Further Research

In this section, further research based on the work in this thesis is suggested. Even though silicon CMP has been used for a long time, several new demanding applications have arisen. Therefore, a deeper process understanding is needed.

For the work on the effect of dopants it would be very interesting to investigate the surface chemistry after CMP of boron and phosphorus diffused samples. Are the boron diffused samples more hydrophilic after CMP, indicating paths to formation of oxides?

Similarly, it would be interesting to investigate if the surface chemistry depends on the process parameters, to confirm the speculation that the surface reactions always are rate limiting (except for very low speeds).

It would be interesting to really show the feasibility of using a soft pad to create rounded structures for microoptics.

For the work on crystal growth method and bondabilty, one way to proceed is to obtain FZ and CZ wafers from the same manufacturer where the same slicing, lapping/grinding and polishing processes have been applied for both types. Thereby, more samples can be bonded. Also, a manufacturer has a greater control of their wafer lapping/grinding and polishing processes than what could be obtained using a laboratory equipment.

The new abrasive surface pad conditioning could become of great technological importance. To verify that the abrasive surface could be working as the active part in a conditioning tool a disk which can be fitted in an industrial CMP tool needs to be manufactured. Optimization of conditioning parameters and marathon testing should then be done to investigate if a sufficient removal rate, planarity, uniformity and defect density could be maintained for a large number of wafers using the same pad.

Acknowledgements

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Swedish Foundation for Strategic Research (SSF) is acknowledged for financing major part of this research.

My friends, for the friendship which means a lot to me and help reminding me that there are other things to do than polishing silicon.

Finally, I want to thank Jenny, and our families, for always being there for me.

Kemisk-mekanisk polering av kisel och kiseldioxid på transistornivå

Kemisk-mekanisk polering (chemical mechanical polishing (CMP)) är en avverkningsmetod som kombinerar mekanisk avverkning och kemisk etsning. En polervätska (slurry) tillförs en roterande platta med en polerduk (pad).

CMP har länge använts i tillverkningen av kiselskivor för integrerade kretsar. Under senare tid har även andra substrat börjat användas, som till exempel kisel-på-isolator (silicon-on-insulator (SOI)). Vid tillverkningen av dessa substrat så används CMP både för att göra ytor "bond"bara, (om två kiselskivors ytor har en mycket liten topografi, så binder (bonding) de till varandra) samt för att tunna ner ena skivan. CMP på relaxerat SiGe har använts för att växa töjt kisel med liten ruffhet. Töjt kisel ökar elektronmobiliteten i kanalen för MOS transistorer. Oxidgenombrottet och kanalmobiliteten för TFT-transistorer (TFT-thin film transistors), gjorda i en polykristallin kiselfilm ofta på glassubstrat, kan ökas genom att applicera CMP innan gateoxidering. CMP har också undersökts för att göra fina ytor på SiC och GaN. Dessa nya applikationer gör att man behöver en djupare förståelse för den grundläggande Si CMP processen.

Minskade fokaldjup i litografin gör att planheten för skivan blir allt viktigare. Topografi på skivan i metallagren kan även ge andra problem som tunnare ledningar över kanter och spacerformering vilket kan ge kvarvarande strängar av metall. Topografin ökar också för varje metallager utan planarisering av varje lager. CMP för att planarisera oxid och ta bort överflödigt volfram efter pluggfyllning (det senare polersteget kallas för damascene) är mogna processer i Al-ledningsteknologi. För att minska de resistiva förlusterna så kan Al/W bytas ut mot Cu. I Cu-ledningsteknologi så fylls pluggar och ledningar i ett steg och överflödig Cu tas bort med CMP (kallas dual damascene). Eftersom Cu inte har några flyktiga reaktionsprodukter, så är det svårt att torretsa Cu. Därför är CMP nödvändigt för att kunna implementera Cu-ledningsteknologi.

På transistornivå används CMP för att göra grund trenchisolering (shallow trench isolation (STI)), för att planarisera trenchkondensatorn i DRAM och för att kunna använda nya gatematerial. STI har många fördelar jämfört med lokal oxidering (local oxidation of silicon (LOCOS)), som bättre planhet och lateral kontroll. STI gör det möjligt att applicera snävare

designregler, en högre packningstäthet och en tjockare fältoxid. Det finns flera sätt att underlätta för STI-CMP, som omvänd mask ("reverse mask"), tillbakaets av resist med mönstrad block resist ("reverse etch-back"), deponering av ett nitridlager efter oxiddeponering ("nitride overlayer") samt dummy strukturer. Nackdelen med de förstnämnda metoderna är att de tillför processteg. Dummy strukturer kan ge en extra koppling till substratet. En process som ej behöver ta till dessa medel kallas för direkt STI-CMP.

I denna avhandling har enbart CMP-system med roterade platta använts. Det finns även andra typer som bygger på linjär eller orbital rörelse. Förutom ett system så behövs det förbrukningvaror; dukar, slurrys and dukkonditionerare.

Det finns tre typer av dukar: mikroporösa dukar av polyuretan med sfäriska porer med diameter i storleksordningen av 50 μm, dukar av poluretanimpregnerad filt och dukar med vertikala öppna porer. Mikroporösa dukar är hårdast, följda av filtdukar och dukar med vertikala porer. Den förstnämnda typen, som ofta har koncentriska spår för att underlätta slurrydistributionen, används vid processning av integrerade kretsar, ofta tillsammans med en mjukare duk under, så kallad stackad duk. En hårdare duk ger en högre planhet men även en lägre uniformitet över skivan. För att komma runt detta så används stackade dukar. Dessa kan bestå av en mikroporös duk över ett mjukare poröst material eller över en filtduk. Filtdukar används också för det första polersteget ("stock removal") vid tillverkning av kiselskivor. Dukar med vertikal porer används vid det sista polersteget ("final polishing") vid tillverkning av kiselskivor. Dessa dukar används också för att minska antalet partiklar och defekter efter planariserings eller damascene polersteget.

Mikroporösa dukar plattas till under polering, s.k. "glazing". Detta gör att avverkningshastigheten minskar från skiva till skiva. För att ha en stabil avverkningshastighet måste duken konditioneras. Detta görs med ett verktyg bestående av diamantpartiklar bundna i en metallyta.

För CMP av kisel och kiseldioxid används vanligtvis slurrys bestående av kiseldioxidpartiklar i en basisk lösning. I STI-CMP så stannar man på nitrid. Avverkningen av nitrid (erosionen) kan minskas genom att använda slurrys med en högre selektivitet mellan oxid och nitrid, till exempel slurrys med ceria partiklar (kan dock ge mer defekter). Därigenom kan man få en högre uniformitet över skivan. Detta kan dock ge en ökad dishing (nivåskillnaden mellan nitridytan och den lägsta nivån på oxiden i grund trench). Kontroll av nitriderosionen är viktig i STI-CMP eftersom den styr steget upp till fältoxiden vid kanten efter nitridets. Att ha god kontroll över kanten är viktigt för att undvika uppkomsten av en kanttransistor med en lägre tröskelspänning. För metall CMP används slurrys med aluminiumoxidpartiklar samt olika typer av tillsatser, som oxidanter, surfactanter och inhibitorer.

Denna avhandling fokuserar på CMP av kisel och kiseldioxid på transistornivå samt för att tillverka ursprungsmaterialet. Det undersöks hur dopningen, kristallriktningen, och processparametrar påverkar avverkningshastigheten. En hög borkoncentration minskar avverkningshastigheten, vilket kan bero på tendens mot formering mot oxid eller en ökad elektronrekombination, och en hög fosforkoncentration (diffusion från fast dopkälla) ökar densamma, vilket kan bero på en snabbare formering av silikat. Avverkningshastigheten för Si(100) ökar sublinjärt med rotationshastigheten, pålagt tryck och koncentrationen av kiseldioxidpartiklar i slurryn.

Skivbondning används för att framställa SOI-substrat. CMP och skivbondning av kiselskivor undersöks mekaniskt. InP MOS strukturer, framställda genom plasmaassisterad skivbondning studeras elektriskt.

En utmaning vid processning av bipolära och BiCMOS kretsar är att integrera STI med djup trenchisolering (deep trench isolation (DTI)). DTI ger lägre substrat till kollektorkapacitans jämfört med övergångsisolering (junction isolation). I avhandlingen presenteras en processmodul där CMP används för att planarisera polykristallint kisel efter fyllning av djup trench. Genom detta kan både nedetsning i djup trench minimeras och polyrester undvikas. Mycket lite extra oxid behöver deponeras på grund av neretsning i den efterföljande fyllningen av grund trench. Dessutom minskar steghöjden vilket gör det lättare att få ett bra resultat för STI-CMP processen.

Ett annat användningsområde som undersöks är att ta bort övergrodden på en selektivt epitaxiellt deponerad kollektor i en bipolär transistor. Genom att använda in-situ dopad selektiv epitaxi kan en mycket bättre kontroll av dopningen fås jämfört med en implanterad kollektor. Under deponeringsprocessen så segregerar fosfor ut mot ytan. För att detta segregerade fosfor ej skall sprida sig under efterföljande processteg så måste det tas bort. Det görs med CMP. En annan fördel med att använda CMP är att ytan blir plan. Det visade sig vara möjligt att växa kristallin SiGe (basen i den bipolära transistorn) av hög kvalitet på kollektorn efter CMP.

CMP för rundning av strukturer har också undersökts, vilket kan vara av intresse för att minska stress eller för att göra mikrooptik. En mjuk duk med vertikala porer har används. Steghöjden ökar över ett steg från oxid över till en öppnad kiselyta fastän kiselytan ligger på en lägre nivå och därför utsätts för ett lägre polertryck. Detta beror på att slurryn har en selektivitet mellan oxid och kisel.

Avverkningshastigheten för material på kiselskivan ökar med höjden på yttoppar på duken. Denna höjd har visats bero av skicket på dukkonditioneraren. Samtidigt som man vill ruffa upp dukytan med konditioneringen vill man ej ta bort för mycket material från duken i sig. Byte av duk med efterföljande kvalificering minskar tiden CMP-systemet processar produktskivor. I avhandlingen introduceras en ny typ av dukkonditionerare som inte bygger på diamantpartiklar. Öppningar tas upp i

oxiden på en oxiderad Si(100) skiva. Skivan etsas anisotropt i KOH, resten av oxiden tas bort, en diamantfilm deponeras med hot filament chemical vapor deposition (HF-CVD), metall pläteras och kiselskivan etsas bort. En pyramidformad diamantyta har erhållits. Eftersom både den plogande arean och inträngningsdjupet för spetsarna in i duken är proportionell mot den lastbärande arean så borde man bättre kunna styra ruffning och avverkningen av duken med det pålagda trycket jämfört med verktyg som bygger på diamantpartiklar. En annan fördel är spetsigheten, vilket medför att den plogande arean är förhållandevis liten. Därför kan verktyget ruffa upp ytan utan att så mycket dukmaterial avverkas. Initiala tester visar att spetsarna håller under konditionering av duken samt att de har en hög förmåga att ruffa upp ytan.

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