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Investigation of Novel Metal Gate and High-κ Dielectric Materials for CMOS Technologies

BY

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Abstract

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The demands for faster, smaller, and less expensive electronic equipments are basically the driving forces for improving the speed and increasing the packing density of microelectronic components. Down-scaling of the devices is the principal method to realize these requests. For future CMOS devices, new materials are required in the transistor structure to enable further scaling and improve the transistor performance.

This thesis focuses on novel metal gate and high-κ dielectric materials for future CMOS technologies. Specifically, TiN and ZrN gate electrode materials were studied with respect to work function and thermal stability. High work function, suitable for *p*MOS transistors, was extracted from both *C-V* and *I-V* measurements for PVD and ALD TiN in $TiN/SiO_2/Si$ MOS capacitor structures. $ZrN_x/SiO_2/Si$ MOS capacitors exhibited *n*-type work function when the low-resistivity ZrN_x was deposited at low nitrogen gas flow. Further, variable work function by 0.6 eV was achieved by reactive sputter depositing TiN_x or ZrN_x at various nitrogen gas flow. Both metal-nitride systems demonstrate a shift in work function after RTP annealing, which is discussed in terms of Fermi level pinning due to extrinsic interface states. Still, the materials are promising in a gate last process as well as show potential as complementary gate electrodes.

The dielectric constant of as-deposited $(Ta_2O_5)_{1-x}(TiO_2)_x$ thin films is around 22, whereas that of AlN is about 10. The latter is not dependent on the degree of crystallinity or on the measurement frequency up to 10 GHz. Both dielectrics exhibit characteristics appropriate for integrated capacitors. Finally, utilization of novel materials were demonstrated in strained SiGe surface-channel *p*MOSFETs with an ALD TiN/Al_2O_3 gate stack. The transistors were characterized with standard *I-V,* charge pumping, and low-frequency noise measurements. Correlation between the mobility and the oxide charge was found. Improved transistor performance was achieved by conducting low-temperature water vapor annealing, which reduced the negative charge in the Al_2O_3.

Keywords: metal gate, high-κ dielectics, titanium nitride, zirconium nitride, MOSFET, thin film, tantalum oxide, aluminum nitride

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List of Papers

I **On the thermal stability of atomic layer deposited TiN as gate electrode in MOS devices**
J. Westlinder, T. Schram, L. Pantisano, E. Cartier, A. Kerber, G. S. Lujan, J. Olsson, and G. Groeseneken
IEEE Electron Device Letters, vol. 24, no. 9, pp. 550-552, 2003.

II **Investigation of the thermal stability of reactively sputter deposited TiN MOS gate electrodes**
G. Sjöblom, J. Westlinder, and J. Olsson
Submitted to *IEEE Transaction on Electron Devices*, 2004.

III **Variable work function in MOS capacitors utilizing nitrogen-controlled TiN_x gate electrodes**
J. Westlinder, G. Sjöblom, and J. Olsson
Microelectronic Engineering, in press, 2004.

IV **Low-resistivity ZrN_x metal gate in MOS devices**
J. Westlinder, J. Malmström, G. Sjöblom, and J. Olsson
Submitted to *IEEE Electron Device Letters*, 2004

V **Effects of low-temperature water vapor annealing of strained SiGe surface-channel pMOSFETs with high-κ dielectric**
J. Westlinder, G. Sjöblom, D. Wu, P.-E. Hellström, J. Olsson, S.-L. Zhang, and M. Östling
Proceedings of the 33rd ESSDERC, pp. 525-528, 2003.

VI **Low-frequency noise and Coulomb scattering in $Si_{0.8}Ge_{0.2}$ surface channel pMOSFETs with ALD Al_2O_3 gate dielectrics**
M. von Haartman, J. Westlinder, D. Wu, B. G. Malm, P.-E. Hellström, J. Olsson, and M. Östling
Submitted to *Solid-State Electronics*, 2004.

VII **Electrical characterization of AlN MIS and MIM structures**
F. Engelmark, J. Westlinder, G. F. Iriarte, I. V. Katardjiev, and J. Olsson
IEEE Transaction on Electron Devices, vol. 50, no. 5, pp. 1214-1219, 2003.

VIII **Simulation and dielectric characterization of reactive dc magnetron co-sputtered $(Ta_2O_5)_{1-x}(TiO_2)_x$ thin films**
J. Westlinder, Y. Zhang, F. Engelmark, G. Possnert, H.-O. Blom, J. Olsson, and S. Berg
Journal of Vacuum Science and Technology, B 20, no. 3, pp. 855-861, 2002.

IX **Patterning of tantalum pentoxide, a high epsilon material, by inductively coupled plasma etching**
L. B. Jonsson, J. Westlinder, F. Engelmark, C. Hedlund, J. Du, U. Smith, and H.-O. Blom
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1. Introduction

In 1977, Ken Olson[*] said “There is no reason anyone would want a computer in their home”. Today, at least one PC is natural in each home, and personal electronic equipments such as mobile phones and personal digital assistants (PDAs, handheld computers), are each mans property. This tremendous, and sometimes inconceivable, development in the information technology industry is the consequence of several decades of enormous progress in the manufacturing of integrated circuits (ICs). The demand for faster, smaller, and less expensive electronic equipments and computers, and especially the potential of growth in wealth in the developing countries, will certainly imply a continued increase in the production rate of microelectronic devices.

One remarkable feature of silicon devices that fuels the rapid growth of the information technology industry is that their speed increases and their cost decreases as their size is reduced. The transistors manufactured today are 20 times faster and occupy less than 1 % of the area of those built 20 years ago. The increased performance of the devices is the consequence of improvements in both architecture and physical scaling of the devices.

This thesis deals with the latter and the research has been focused on novel materials in microelectronic devices. Especially the logic CMOS fabrication is facing a difficult task in the sense that new materials must be introduced in the heart of the transistor. The gate stack consist of the gate electrode and the gate dielectric, conventionally made of polycrystalline silicon and silicon dioxide, respectively, which must be replaced with novel metals or metal compounds and dielectric materials with high dielectric constant (κ-value[¤]), so-called high-κ dielectrics. In this thesis, various metal compounds and high-κ dielectrics have been fabricated and evaluated with respect to their electrical characteristics for implementation in CMOS applications. In addition, important fabrication process steps have been studied.

Chapter 2 presents the development in and limitations with down-scaling of MOSFETs with emphasis on metal gates and high-κ gate dielectrics,

[*] President, chairman and founder of Digital Equipment Corp.

[¤] The dielectric constant can also be referred to the Greek symbol, ε (epsilon), although κ has become the standard symbol in the literature with respect to dielectric materials in MOS devices.

whereas Chapter 3 describes the devices used in this thesis and the fundamental characteristics of them. Chapter 4 explains manufacturing methods and discusses results from both deposition and etching of dielectric materials (Papers VIII-IX). Chapter 5 accentuates the most important results achieved from the experiments on metal gate (Papers I-IV) as well as from the electrical characterization of metal gate/high-κ pMOSFETs (Papers V-VI) and of dielectric materials in capacitors (Papers VII-VIII). In some cases, this Summary presents new results and discusses the achieved results more extensively than what is done in the appended articles. First, a brief section on the IC history will finalize this Introduction chapter.

HISTORY

The first solid-state point-contact transistor was invented at Bell Laboratories by Bardeen, Brattain and Shockley in 1947, who also received the Nobel Prize in 1956 for their invention. Germanium was first used as the semiconductor material but since silicon was less expensive and more thermally stable, silicon became the preferred material. Consequently, the first commercial silicon transistor was available in the mid-50s. In 1958, the integrated circuit was born when Jack Kilby at Texas Instruments built a simple oscillator IC with five integrated components. The evolution of the modern microelectronics industry started with the first fabricated metal-oxide-semiconductor field-effect-transistor (MOSFET) in 1960 and the invention of complementary MOS (CMOS) transistors in 1963. Since then, CMOS devices have been the fundamental building block in logic circuits such as microprocessors and memories. As early as 1965, Gordon Moore wrote a paper where he observed that ”The complexity for minimum component cost has increased at a rate of roughly a factor of two per year” and he also predicted that the rate could be expected to continue [1]. This observation became known as Moore's law, a self-fulfilled prophecy which is still valid today even though it has been revised to: the number of components per chip doubles approximately every 2 years. As an example of the extremely fast rate of evolution, a comparison between different microprocessors is made in Table I.

Table I. The evolution of Intel microprocessors over the last 30 years.

Microprocessor	Year	Line width	Number of transistors	Clock speed
4004	1971	10 µm	2300	108 kHz
486	1989	1 µm	1 200 000	20 MHz
Pentium 4	2000	180 nm	42 000 000	1.3-3.4 GHz
Pentium 4	2004	90 nm	125 000 000	2.4-3.6 GHz

2. CMOS Development and Scaling

INTRODUCTION

A CMOS device consists of an *n*-channel and a *p*-channel MOSFET integrated on the same chip. A schematic illustration of the cross section of a modern CMOS transistor is shown in Fig. 1. Improvements in packing density, speed, and power are basically the driving forces for down-scaling the CMOS devices. To reduce the transistor design without compromising the performance, the scaling is carried out by following certain rules or principles. The scaling principles first proposed were following the *constant-field scaling*, where all device and circuit parameters should be scaled with the same factor, k [2]. This results, for instance, in increased speed by the same factor and reduced power dissipation by k^2. However, in constant-field scaling, the decrease in power-supply voltage is too restrictive, mainly due to no or low capability to scale the threshold voltage. The latter is due to increased off current when the transistor is in OFF state, as will be discussed in Section 3.2. A more *generalized scaling* was discussed where the voltage is scaled less rapidly than the dimensions at the expense of the electric field, which changes by another factor [3]. This keeps the voltage sufficiently large, but gives rise to increased power densities and high electric fields leading to hot electrons and oxide reliability problems. In reality, the CMOS technology scaling has followed mixed principles of constant-field and generalized scaling.

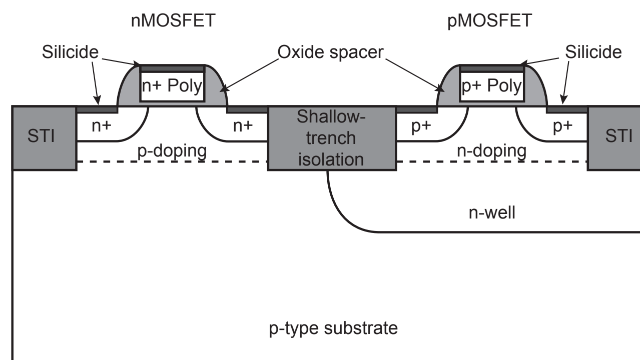

Figure 1. Schematic cross section of a CMOS device.

Despite following the mentioned principles, issues will eventually arise. One of them is the thickness of the insulating gate dielectric that will become only a few atom layers thick, which endanger the insulating capability. Due to the higher dielectric constant of a high-κ dielectric material, it can be made thicker with equivalent or better capacitance, i.e. control over the performance of the transistor, in addition to the increased insulating property. Another issue is the implementation of metals or metal compounds as gate electrode materials where an important criterion is to achieve complementary and stable work functions of the metals as well as to manufacture them.

The scaling requirements for future CMOS technologies are generally guided by the International Technology Roadmap for Semiconductors (ITRS) [4]. The ITRS identifies the technological challenges and needs, facing the semiconductor industry over the next 15 years. Every other year a new assessment is published and the reduction in gate length has been observed to be even faster than the predictions, see Fig. 2. The scaling falls into two main application categories, high performance (HP) and low power (LP), and depending on the application, different scaling goals are employed. For HP, typically high-end desktop and server applications, the main goal is to maximize the performance (i.e. speed) and aggressive scaling is utilized. High leakage current is acceptable and is a necessary trade-off, and the introduction of novel materials are not expected before 2007. For LP applications, typically mobile systems, the main goal is to minimize chip

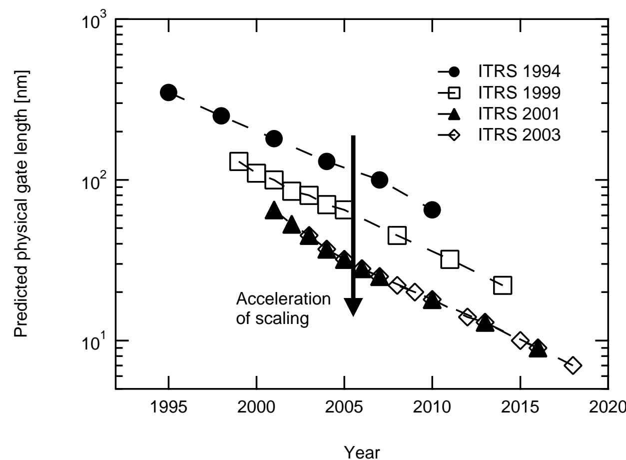

Figure 2. Predicted physical gate length by different editions of the ITRS. Historically, the next technology node has been introduced earlier than predicted by the roadmap.

power consumption and dissipation to preserve battery life. Here, conventional gate dielectrics will not meet the requirement and the introduction of novel gate dielectrics is in the near future [5]. According to the ITRS, the implementation of dual metal gate electrodes with appropriate work functions will occur 2008-2009. A step in this direction has already been taken by Intel Corp. who has manufactured transistors with both metal gates and high-κ gate dielectrics with record-setting I_{ON}/I_{OFF} characteristics [6]. This new technology will be implemented in their 45 nm node, due to begin production in 2007.

2.1 Metal Gate Electrodes

BACKGROUND

The gate electrode in MOS devices is conventionally made of highly doped polycrystalline silicon (poly-Si). Several problems are lately encountered due to the aggressive scaling. One of them is depletion of the poly-Si gate electrode when the gate stack is biased in inversion. The depleted region (2-5 Å) is added to the dielectric thickness and the equivalent oxide thickness (EOT) is increased, which results in reduced inversion layer charge density and degradation of the transconductance. Increased resistance of the gate electrode fingers is another issue due to the reduction in geometry when scaling.

To reduce the poly-Si depletion effect and to decrease the high resistance in the short gate electrodes, the doping level in the poly-Si electrode is increased with the scaling. During the high temperature activation of the dopants, diffusion of boron penetrates from the gate, through the gate dielectric and into the silicon channel, which will degrade the performance of the transistor. The step from conventional SiO_2 to high-κ materials might also induce troubles with respect to compatibility since some high-κ materials have been shown to react with poly-Si, making it a less favorable material for continued use as a gate electrode [7, 8].

A viable way to circumvent the mentioned issues with poly-Si is to use a metal or metal compound as the gate electrode. (Hereafter, “metal gate” refers to a metal gate technology consisting of a metal and/or a metal compound.) No doping is necessary due to the excess of electrons in the metal, hence no boron penetration will occur, and no gate depletion is expected. In addition, metal gates show the potential of reduced sheet resistance.

The present research activities around the world on metal gates involve developing accurate measurement methods to determine the work function

of the various candidates. It is also important to understand the factors that control the work function and the dependence of the work function on the underlying gate dielectric material. Further, the thermal stability with respect to work function, EOT, gate leakage, etc. is important as well as to develop dual work function tuning techniques that are compatible with the CMOS technology.

REQUIREMENTS AND INTEGRATION ISSUES

One requirement on a new metal gate technology is the correct set of work functions in order to replace poly-Si in conventional CMOS transistors. In the *p*MOS (*n*MOS) transistor, heavily *p*-type (*n*-type) doped poly-Si is used as gate electrode and the work function is about 5.2 eV (4.1 eV). Consequently, the substituting metals or metal compounds should have matching work functions for optimal performance of the transistor [9]. Several candidates have been proposed and Appendix C summarizes some of the different stacks as well as extracted work functions and extraction methods. For some stacks, an interval in work function is given which is due to variation in composition (for example modification in nitrogen content) or variation in work function after various thermal treatments. Duplicate stacks are from different references. It is obvious that no standardized extraction method exists and values scatter somewhat depending on deposition method, fabrication flow, and how the measurement methods have been conducted.

Introducing new materials into the complex and well established IC fabrication is not a straightforward task. For successful implementation, the proposed metal gate technology should be compatible with standard CMOS processing with respect to process integration and contamination, reproducible, as well as thermally and chemically stable. Further, uniform deposition and etching as well as selective etching to stopping layer and mask materials are critical.

Since the gate electrode is deposited on top of the ultra thin gate dielectric, care has to be taken and preferably a one-step deposition process is desirable. This has been one of the advantages of using poly-Si; complementary work functions are easily achieved by ion implantation (I/I) into the one-step deposited un-doped poly-Si. Finding one metal with two different work functions is not possible, but several process flows have been proposed for manufacturing complementary metal gates.

For example, ion implantation by certain species into a metal to obtain the desired work function, similar to the I/I process of poly-Si, could be a viable solution. This has been demonstrated for Mo and TiN_x films where a reduction in work function is seen [10, 11]. However, only small variations in work function were found, hence complementary work functions could not be achieved. Another integration route could involve depositing a stack

of metals or metal compounds. By depositing material A and B followed by selectively removing B in one of the transistors regions (*n*MOS or *p*MOS), and then thermally anneal the stacks, reaction (diffusion or intermixing) between the materials occur such that a complementary work function is achieved compared to the region where only metal A exist, see Fig. 3. Examples of such processes are: over-stoichiometric TiN_{1+x} on Ta or Mo, where nitrogen from the TiN_{1+x} is diffusing into the Ta or Mo [12]; Ni and Ti intermixing, where the threshold voltage in *n*MOS devices are determined by Ti and Ni-rich alloy of Ti and Ni sets the threshold voltage for *p*MOS devices [13]. A related process flow is nickel silicidation of doped poly-Si, where the doping type and concentration in poly-Si sets the work function and the silicidation hinders the gate electrode depletion effect [14].

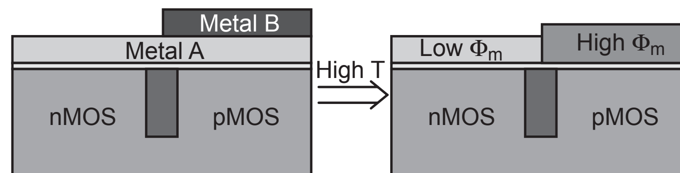

Figure 3. Schematic picture of a possible complementary metal gate formation process, which requires only one critical etch step. Metal A and B are deposited on both types of devices followed by selective removal of metal B. High temperature annealing give rise to intermixing or diffusion of metal A and B on one of the devices. Appropriate choice of metals results in complementary work functions.

FERMI LEVEL PINNING

Most literature on Fermi level pinning deals with the metal-semiconductor interface and the meaning of Fermi level pinning in such context is the fact that the Schottky barrier height is insensitive to the metal work function, i.e. the Schottky-Mott relationship is not supported by experiments [15]. Several mechanisms affect the barrier height in Schottky contacts, one of them being metal-induced gap states (MIGS). The MIGS are *intrinsic states* in the band gap of the semiconductor due to penetration of the wave functions of the metal electrons into the semiconductor in the energy range where the metal conduction band overlaps the semiconductor band gap [16-18]. States close to the semiconductor conduction band is most likely acceptor-type while those close to the valence band are donor-type. The energy level where the cross-over from donor- to acceptor-type occurs is called the charge neutrality level, E_{CNL}. Charging of these states give rise to a dipole across the interface which drive the Fermi level such that the dipole is reduced, i.e. Fermi level pinning. Depending on the position of the E_{CNL} in the semiconductor band gap, both an increase and decrease in extracted work function can occur. The

Fermi level pinning of metal-semiconductor interfaces is still in debate and lately it has been suggested that polarization of chemical bonds at the metal-semiconductor interface can lead to Fermi level pinning and a convergence of the Schottky barrier height toward one-half of the band gap [19].

In MOS devices, metal-dielectric and poly-Si-dielectric interfaces seem to suffer from Fermi level pinning even though the mechanism behind the phenomenon is not certainly the same as for metal-semiconductor interfaces. Various articles have reported deviation of extracted work function or threshold voltage shift from the expected values and some reports differs in conclusion. For instance, it has been found that poly-Si gates on HfO_2 and Al_2O_3 gate dielectrics suffer from Fermi level pinning [20, 21] whereas, a model based on the interface dipole theory [17] indicates that poly-Si gates on high-κ dielectrics are less affected by Fermi level pinning [22]. The latter article presents a model describing Fermi level pinning of the metal work function on high-κ dielectrics towards the E_{CNL} due to MIGS. The model predicts that the higher κ-value of the dielectric material, the more effective pinning of the Fermi level.

Further, it has been found that thermal annealing of the metal gates at temperatures above 800 °C results in mid-gap values for almost all metal gate candidates [23], which also is seen in Paper I-IV. The latter is related to *extrinsic states* in the interface and will be further discussed in Section 5.1.3.

2.2 High-κ Gate Dielectric Materials

BACKGROUND

When down-scaling the MOSFETs, the thickness of the gate dielectric must reduce in the same manner as the other dimensions according to the scaling principles. For the technology node of 65 nm that should be introduced year 2007 [4], the oxide thickness is predicted to be less than 10 Å, which is equivalent to only a few atomic layers of SiO_2. Direct tunneling becomes important for oxide thicknesses less than 40 Å and increases exponentially with decreasing oxide thickness [24]. The gate leakage current density is modeled to be increased by ten orders of magnitude as the oxide thickness decreases from 36 Å to 15 Å, where the leakage current density is predicted to be about 10^2 A/cm^2 [25]. For high performance applications, such high current density can be acceptable but the current flow through the dielectric will limit the reliability of the device [26]. For low-standby power, less leakage current density is tolerable and hence thicker dielectric thickness is a necessity.

To maintain the capacitance between the gate electrode and the silicon channel without reducing the SiO_2 thickness, a dielectric material with a higher dielectric constant (κ-value) is needed. Research on finding an appropriate substitute to the superior SiO_2 has been going on for almost a decade. Oxy-nitrides (SiO_xN_y) have been introduced to extend the use of SiO_2 in production but eventually it has to be replaced by a high-κ material, such as HfO_2, ZrO_2, Al_2O_3, La_2O_3, or mixtures of them or metal-oxide-silicates of the mentioned compounds. Not only the κ-value is important but also the band alignments of the conduction and valence band with respect to the silicon band structure are crucial in order to minimize gate leakage currents. In Fig. 4, the calculated conduction band and valence band offsets are shown for various dielectrics on Si [27]. The band offsets are quite asymmetric and the smallest barriers are found for the conduction band. For instance, Ta_2O_5 was for a long time considered a promising high-κ candidate, but the low barrier (0.3 eV) implies significant gate leakage current due to electron emission into the conduction band, which is not tolerable. In addition, Ta_2O_5 is thermally unstable in contact with Si [28, 29]. However, Ta_2O_5 has been successfully implemented in DRAM capacitors [30, 31].

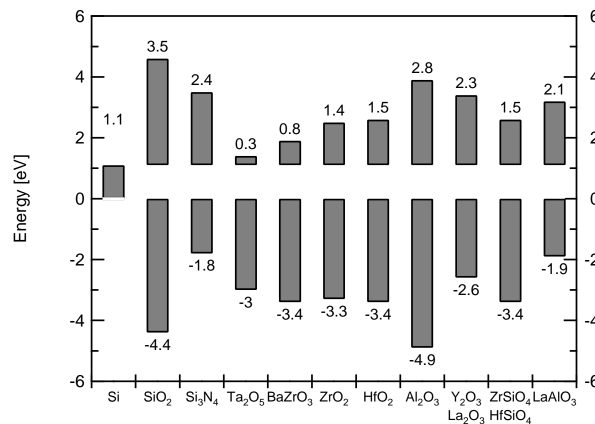

Figure 4. Calculated band offsets for the valence and conduction band of various oxides on Si (from ref. [27]). The band gap of Si is shown to the left and the valence band of Si is zero reference.

IMPLEMENTATION OF HIGH-κ DIELECTRICS

Silicon dioxide is thermally grown at very high temperature in oxygen ambient and is a clean and well controlled process that has been developed since the beginning of the CMOS era in the 60's. All high-κ materials are

deposited, usually with the aid of precursors or in a plasma environment resulting in a not too well controlled growth of the extremely thin film. Contamination, oxygen deficiency, and interface reactions give rise to high density of charges and traps in the grown dielectric film and at the interface to the silicon substrate, which will negatively affect the transistor characteristics. Fabricated transistors have shown characteristics with substantial shift in threshold voltage from the ideal value [Paper V], charge trapping and reliability issues [32], as well as instability in the threshold voltage [33, 34].

Mobility degradation is another issue when introducing high-κ materials. As will be discussed in Section 3.2, the charges in the dielectric material affect the density of inversion charge carriers in the channel, which directly affects the mobility. Since almost all high-κ materials have extensive amount of charges and traps at the interface, the gain of introducing a high-κ material is often found to be eliminated by the reduction in mobility. It is also considered that the high ionic polarization in high-κ materials gives rise to remote phonon scattering [35], which will degrade the mobility. The high κ-value in high-κ dielectrics is a direct result of the higher ionic polarization. Hence, remote phonon scattering might be inherently increased by the use of high-κ dielectrics.

Due to the mentioned issues, most often an ultra-thin silicon dioxide layer is deliberately grown between the silicon channel and the high-κ material. This will ensure that the mobility degradation is minimized while the benefits of increased κ-value are added to the stack. Of course, an interfacial layer of SiO_2 will increase the EOT and limit the thickness of the high-κ dielectric, and a trade-off between gate leakage current and mobility enhancement must be considered. For the technology node of 65 nm, an EOT of less than 10 Å is required and logically the interface oxide must be even less. Consequently, the formation of the interfacial layer is extremely critical and the thickness control and uniformity over a 300 mm wafer is crucial. Various deposition techniques exist for the ultra-thin interface oxide, including thermal annealing, wet chemical oxide, and different ozone treatments.

It is also discussed that the implementation of high-κ dielectrics should be accompanied by the introduction of metal gates. In addition to less severe reactions with high-κ dielectrics, metal gates are thought to be more effective in screening the surface phonons at the high-κ surface than a poly-Si electrode, hence increasing the mobility [36].

The most promising, or more accurately, most explored high-κ material today is HfO_2 due to its low leakage current, high enough conduction band offset, and acceptable thermal stability. Other promising materials that have been extensively investigated are ZrO_2 and Al_2O_3. The former has similar

characteristics as HfO_2 though it has been reported to be unstable in contact with silicon [37, 38]. The latter has high band gap and large band offset (Fig. 4) but only moderate dielectric constant (around 9) and, what is more detrimental, suffers from high density of negative fixed charge, see for example [Paper V]. Lately, lanthanide oxides are considered in addition to ternary metal-oxide compounds such as hafnium-aluminates and hafnium-silicates [39-42].

2.3 Novel CMOS Concepts

CHANNEL MATERIALS

The bulk mobility of electrons and holes in germanium is significantly higher than in silicon. Unfortunately, growing a thermal oxide on Ge typically results in a high density of interface traps besides the fact that the germanium oxide is soluble in water. Therefore, high performance Ge-based MOS devices are not easily fabricated in a conventional process flow.

Compressively strained SiGe has been shown to have hole transport properties about 4-6 times higher than in bulk Si [43]. Growth of a thin layer of SiGe on relaxed Si results in biaxial compressive strain and the increased hole mobility is primarily caused by reduced effective mass in the top-most valence band. The inverse stack can also be grown, i.e. Si on relaxed SiGe, which results in tensile strained Si that modifies the Si conduction band. As a consequence, the electron mobility in strained Si is about 2-3 times higher than in bulk Si [44].

Equal to the Ge case, thermal oxidation of SiGe produces an oxide of poor quality which will erode the performance of the fabricated device. In addition, high temperature annealing steps can result in relaxation of the strained layer, hence eliminating the performance boost. Therefore, the introduction of high-κ dielectrics that are *deposited* at low temperature opens new doors for implementing novel channel materials such as strained Si and SiGe as well as Ge [45].

ALTERNATIVE FABRICATION STEPS AND DEVICES

In a conventional MOSFET fabrication sequence, the gate dielectric and the gate electrode are deposited rather early. This means that several high temperature process steps remains which can cause thermal reactions between the materials in the gate stack. To avoid such issue, a fabrication sequence has been developed called the damascene process. The latter involves depositing a dummy gate stack which is removed by etching *after* the high temperature process steps followed by deposition of a new gate

stack. This can be functional when implementing high-κ gate dielectrics and metal gate electrodes, which might have limited thermal budget.

Silicon on insulator (SOI) devices are built in a thin layer of silicon (less than 500 nm) on top of an insulating buried oxide film. The advantages are superior insulating properties with reduced parasitic junction capacitances, suppressed leakage currents, and small or no body effect. The devices are mostly used in low-voltage applications, RF circuits and radiation-hard circuits as well as in high-voltage applications combined with logic circuits. Totally different MOSFET architectures are also developed from SOI substrates where the planar technology is abandoned. Double, triple, and gate-all-around FiNFETs are examples of such devices. Both high-κ gate dielectrics and metal gates will be of importance for these devices where the gate electrode might require materials with different work functions compared to conventional MOSFETs.

The mentioned alternative fabrication methods of MOSFETs and alternative device architectures increase the integration complexity, and low throughput and high cost makes fabrication of conventional devices economically unacceptable. Only devices intended for special purposes can justify the higher cost. However, the drive toward faster and smaller devices necessitates alternative manufacturing methods. The idea of using SOI in MOSFETs that started as a lab curiosity has now grown to commercially available components and 300 mm SOI wafers are standard products at SOI manufacturers.

3. Devices and Basic Device Parameters

Devices used in the experimental part of this thesis will be presented in this chapter. The basic building block in VLSI circuits, such as microprocessors and memories, are the metal-oxide-semiconductor field-effect-transistors (MOSFETs). The metal-oxide-semiconductor (MOS) capacitor is a device in itself and also a simplified structure of the MOSFET. Hence, the MOS capacitor gate stack is commonly studied even though the application will be for transistors.

3.1 The MOS Capacitor

CAPACITANCE-VOLTAGE CHARACTERISTICS

A schematic illustration of the two-terminal MOS capacitor structure is shown in Fig. 5, and it consists of a gate electrode, gate dielectric and semiconductor substrate. To reduce the series resistance of the structure, the substrate is usually high-doped (i.e. about 10 mΩcm) while the top-most epitaxial layer (epi-layer in Fig. 5) is low-doped (i.e. 1-10 Ωcm). Valuable information about the gate stack can be extracted from a capacitance-voltage (C-V) measurement such as insulator thickness (T_{ox}), doping density (N_A), flatband voltage (V_{fb}), oxide charge density (Q_{ox}), and work function (ϕ_m).

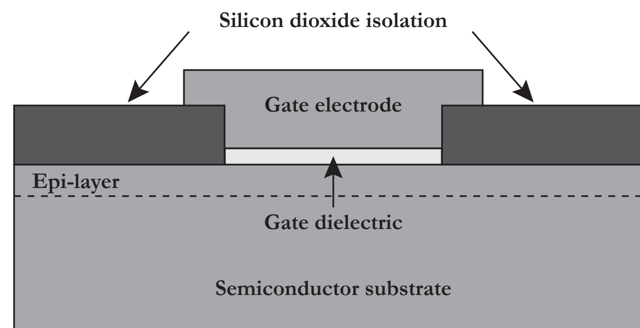

Figure 5. Schematic illustration of the MOS capacitor structure.

The capacitance of a MOS structure varies with gate voltage due to accumulation, depletion and inversion of charge carriers in the silicon substrate. A typical high-frequency (100 kHz) *C-V* curve for a *p*MOS capacitor is shown in Fig. 6a. The oxide thickness is calculated from the capacitance in accumulation and the doping density is extracted from the capacitance in depletion. When these two quantities are known, the flatband capacitance and the corresponding flatband voltage are easily calculated. The flatband voltage is the voltage at the gate when there is no band bending in the silicon. Ideally, this occurs at zero gate voltage, but due to work function difference between the gate electrode and silicon substrate and due to charges in the oxide, the flatband voltage is shifted in either direction according to the following equation:

$$V_{fb} = \phi_{ms} - \frac{Q_{ox}}{\varepsilon_0 \kappa_{ox}} T_{ox} \qquad (1)$$

where ϕ_{ms} ($\equiv \phi_m - \phi_s$) is the work function difference between the metal and the semiconductor, Q_{ox} is the equivalent oxide charge density per unit area located at the dielectric/semiconductor interface, ε_0 is the permittivity in vacuum, and κ_{ox} is the dielectric constant of the dielectric material in the stack.

Charges and traps in the oxide and at the interface between the dielectric and silicon will cause the *C-V* curve to decay in several ways. An example is shown in Fig. 6b, where the extracted flatband voltage will depend on measurement frequency due to different response of oxide traps to the frequency. Further, a hysteresis can appear when sweeping the gate voltage forth and back due to charging and discharging of traps in the oxide. In addition to shift in V_{fb}, interface trapped charge will stretch out the *C-V* curve along the gate voltage axis. The amount of charges can be reduced by appropriate annealing of the stack. For instance, forming gas anneal (FGA) at 400 °C is used for passivation of Si dangling bonds at the SiO_2/Si interface with hydrogen, thus reducing the interface states.

There are four general types of charges associated with the SiO_2/Si system and will be briefly mentioned here (for further reading, please refer to [46]). *Interface trapped charges* (Q_{it}) is positive or negative charge located at the SiO_2/Si interface and is in electrical interaction with the underlying silicon, thus they can be charged or discharged depending on the surface potential. *Fixed oxide charge* (Q_f) is positive charge in the oxide layer less than 2 nm from the SiO_2/Si interface. They are not in electrical interaction with the silicon and are primarily due to structural defects and depend on the temperature during growth. *Oxide trapped charge* (Q_{ot}) can be positive or negative due to holes or electrons trapped in the bulk of the

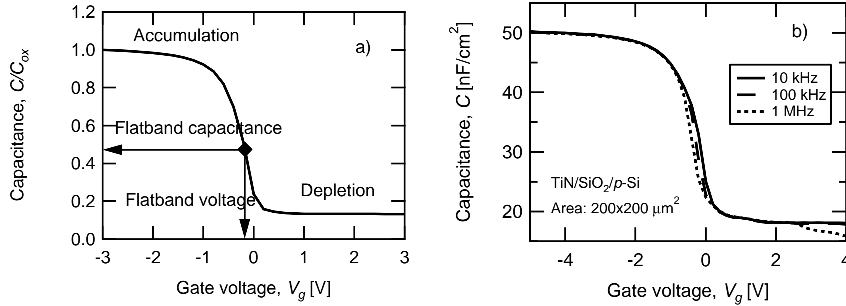

Figure 6. a) Typical C-V characteristic for a pMOS device. Flatband voltage and capacitance is shown. b) Frequency dispersion around flatband voltage due to different response to the measurement frequency by charges in the oxide.

oxide. Contrary to the fixed charge, the oxide trapped charge can sometimes be annealed by low-temperature treatments. *Mobile oxide charge* (Q_m) is caused by ionic impurities, primarily alkali ions, and possibly H^+, which are eliminated in modern clean room facilities.

The amount of charges and traps in the oxide is not only affecting the extracted flatband voltage of MOS capacitors but is also shifting the threshold voltage and could reduce the mobility in MOS transistors. The latter will be discussed in the Section 3.2.

A common parameter extracted from a MOS-device is the equivalent oxide thickness (EOT), which is the electrical thickness rather than the physical thickness, of a high-κ dielectric film in terms of an equivalent thickness of SiO_2 and is given by:

$$EOT = T_{ox}\frac{\kappa_{SiO_2}}{\kappa_{ox}} + T_{IL}\frac{\kappa_{SiO_2}}{\kappa_{IL}} \tag{2}$$

where κ_{SiO2} is the dielectric constant of SiO_2 (=3.9), κ_{ox} is the dielectric constant of the high-κ dielectric, T_{IL} and κ_{IL} are the thickness and dielectric constant of a possible interfacial layer between the Si substrate and the high-κ film, respectively. A plot of EOT vs. T_{ox} reveals κ_{ox} as well as the thickness of the interfacial layer, T_{IL}.

GATE CURRENT-VOLTAGE CHARACTERISTICS

Ideally, the MOS structure is an insulating device where no dc gate current is flowing. This is of course not true, especially not for thin dielectric materials and for high electric fields, which is the case in modern MOS devices. Depending on the current response to the voltage, electric field or temperature, various models have been adopted to describe the current

transport mechanism through a dielectric material. For instance, Schottky emission and Frenkel-Poole emission have strong temperature dependence, whereas tunneling is relatively insensitive to temperature, see for example [47].

Tunneling can be divided in two cases, direct tunneling and Fowler-Nordheim (FN) tunneling. Thin dielectric films (< 40 Å) suffer from direct tunneling, where electrons tunnel right through the dielectric film in contrast to FN tunneling where the electron tunnels to the conduction band of the insulator, see Fig. 7. The tunneling current density (J_{FN}) in FN tunneling is given by:

$$J_{FN} = \frac{q^3 E_{ox}{}^2 m_0}{8\pi h \phi_B m^*} \exp\left(-\frac{8\pi\sqrt{2m^*}\,\phi_B^{3/2}}{3qhE_{ox}} \right) \quad (3)$$

where m_0 is the electron mass, m^* is the effective electron mass in the oxide, E_{ox} is the electric field across the oxide, and ϕ_B is the barrier height between the electrode and the conduction band in the oxide (Fig. 7). FN tunneling can be used to calculate the barrier height between the gate electrode and the dielectric material (gate injection) as well as between the semiconductor substrate and the dielectric (substrate injection).

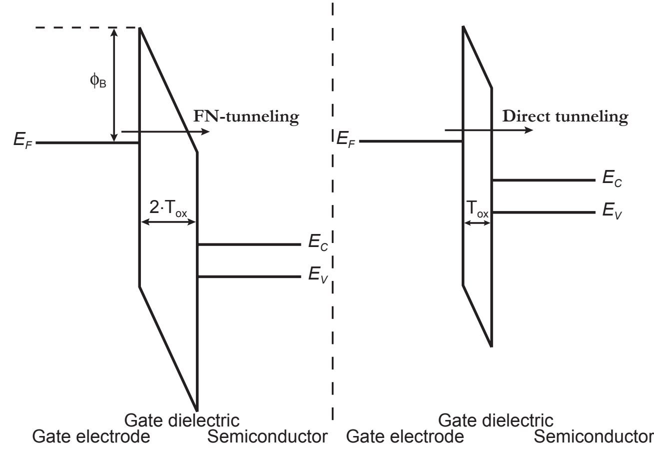

Figure 7. Schematic picture of Fowler-Nordheim (FN) tunneling and direct tunneling during gate injection. It is also illustrated that for the same electric field, a thinner dielectric film results in direct tunneling (if T_{ox} < 40 Å). E_F, E_C, and E_V are the energies of the Fermi level, conduction band, and valence band, respectively.

3.2 The Field Effect Transistor

BASIC DEFINITIONS

The MOS transistor is a four-terminal device and consists of a semiconductor substrate, heavily doped source and drain regions, and a gate electrode. Figure 8 shows a schematic picture of an *n*MOSFET where the source and drain regions are *n*-doped and the substrate is of *p*-type. The transistor acts like a switch where, in the ON state, current flows between the source and drain regions. The voltage at the gate electrode capacitively affects charge carriers in the channel and by attracting minority carriers in the *p*-type substrate, the substrate surface is eventually inverted, creating an *n*-channel between the source and drain through which the current can flow. Thus, the gate electrode modulates the conductance of the channel and in that way controls the current flow between the source and drain.

Important parameters of the transistor includes the channel length (L) and width (W), the insulator thickness (T_{ox}), the doping levels in the substrate(N_A), and in the source and drain regions, the junction depth (x_j), and the voltage at the terminals; which all affects the performance and the characteristics of the transistor. However, the current through the transistor is not only determined by the mentioned parameters, but also by the effective mobility of the charge carriers in the silicon channel (μ_{eff}), which will be discussed below.

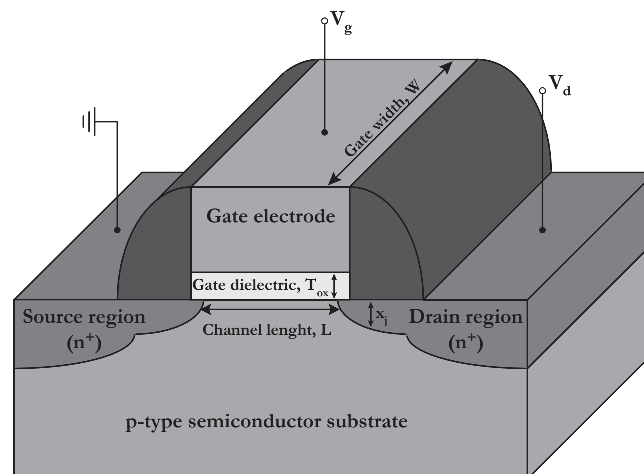

Figure 8. Schematic illustration of a nMOSFET structure.

MOSFET *I-V* CHARACTERISTICS

As explained above, the gate electrode voltage controls the inversion charge in the channel and hence the drain current. Idealized, schematic drain current (I_d) characteristics versus drain voltage (V_d) with gate voltage (V_g) as parameter are displayed in Fig. 9. Two distinct regions are marked in the figure, the linear and the saturation region, and each region's drain current is given by:

$$I_d = \mu_{eff} C_{ox} \frac{W}{L}(V_g - V_t)V_d \quad (4)$$

$$I_d = I_{d,sat} = \mu_{eff} C_{ox} \frac{W}{L}\frac{(V_g - V_t)^2}{2m} \quad (5)$$

respectively, where C_{ox} is the gate capacitance per unit area and m is the body-effect coefficient, typically between 1.1 and 1.4, and is given by:

$$m = 1 + \frac{\sqrt{\varepsilon_{Si} q N_A / 4\varphi_B}}{C_{ox}} = 1 + \frac{C_d}{C_{ox}} \quad (6)$$

where φ_B is the potential difference between the intrinsic Fermi level and the Fermi level of the substrate and C_d is the maximum depletion capacitance in the silicon. Note that in the saturation region, the drain current is independent of V_d [Eq. (5)]. An important parameter in Eqs. 4 and 5 is the threshold voltage (V_t), which is given by:

$$V_t = V_{fb} + 2\varphi_B + \frac{\sqrt{4\varepsilon_{Si} q N_A \varphi_B}}{C_{ox}} \quad (7)$$

V_t is defined as the gate voltage when the band bending (or surface potential) reaches $2\varphi_B$. V_t determines the current in both ON and OFF states. In saturation [Eq. (5)], V_t should be as small as possible to increase the drain current. On the other hand, the drain current in OFF state ($V_g = 0$) is exponentially decreasing with V_t, hence V_t should be as large as possible. For transistors with high supply voltage, this contradiction in generally not an issue, the important matter is rather that the V_t is the same for different transistors so that the hundreds of millions of transistors in a microprocessor turn on at the same voltage. On the other hand, for modern CMOS technology the supply voltage is reduced with scaling and approaches the threshold voltage, which gives a small gate overdrive (V_g–V_t) and thus low drain current. Hence, a trade-off between I_{ON} and I_{OFF} must be considered and the control of V_t is extremely important. Moreover, according to Eq. (7), the threshold voltage depends on the flatband voltage [Eq. (1)], which in turn depends on the charges in the oxide. Depending on the surface potential,

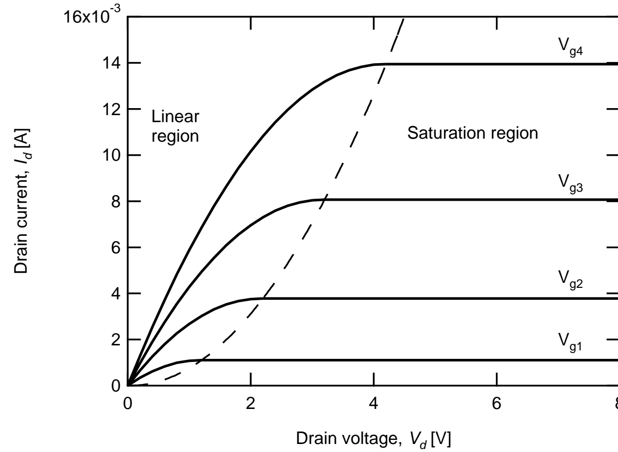

Figure 9. I_d-V_d characteristics with V_g as parameter for a MOSFET device. The dashed curve shows the onset of saturation, i.e. $I_{d,sat}$, $V_{d,sat}$. ($V_{g4} > V_{g3} > V_{g2} > V_{g1}$)

traps close to the interface can charge and discharge, which results in shifts of the threshold voltage and hence, non-consistent transistor performance.

When V_g is below V_t, a very small current is flowing and the transistor is in the subthreshold region. Even though the current flow is low in the subthreshold region, the region is important for the switching performance of the transistor. A subthreshold slope is defined as:

$$S = \frac{dV_g}{d(\log I_d)} \approx 2.3 \frac{mkT}{q} \tag{8}$$

and determines how much gate voltage swing that is needed to change the current one decade, typical value is 60-100 mV/decade. A steep subthreshold slope [low value of S in Eq. (8)] is desirable for the ease of switching the transistor on and off.

MOBILITY

The mobility in the MOSFET inversion channel is significantly lower than in bulk silicon due to different scattering mechanisms. The charge carriers in the inversion layer are primarily influenced by Coulomb scattering, phonon scattering, and surface roughness scattering.

Coulomb scattering occurs at low effective normal electric fields due to the doping concentration in the substrate and due to charges and traps in the oxide and at the oxide/silicon interface. Interface traps will capture charge carriers and reduce the mobile inversion charge, as well as act as charged scattering centers. At higher normal electric fields, the charge carriers are

distributed closer to the Si surface, and scattering due to surface roughness reduces the mobility. Phonon scattering occurs at medium electric fields.

SHORT-CHANNEL MOSFETS

For short-channel MOSFETs, the drain voltage starts to affect the channel and the gradual channel approximation and the charge sheet approximation are no longer valid, i.e. the electric field along the channel becomes comparable to the electric field perpendicular to the channel and the charge carriers are no longer confined to the surface in a charge sheet, respectively. Some basic features important for short-channel device design are considered briefly below (for further reading, please refer to [48]).

The short channel effect (SCE) is the drop in threshold voltage when decreasing the gate length. The effect can be understood by considering the charge in the transistor. For long-channel devices, the charge at the gate controls the charge in the channel, but for shorter devices, the drain and source voltage affects and produce charges in the channel, which results in that lower gate voltage is required to reach the threshold condition. An increase in off current can also ensue from an increased drain voltage, so-called *drain induced barrier lowering* (DIBL) and is monitored as reduced V_t as a function of V_d (mV/V). Due to *velocity saturation*, the drain current saturates at lower $V_{d,sat}$ in short-channel devices compared to long-channel devices. This occurs because the lateral field affects the charge carriers such that they are no longer confined to the surface channel. *Channel length modulation* is the decreased effective channel length due to pinch-off which is accentuated for short-channel devices as compared to long-channel devices where the effect is negligible.

3.3 MIM Structures

Since down-scaling occurs over the entire chip, not only transistors should increase their packing density but also other components such as capacitors. Integrated capacitors can occupy a large fraction of the total chip area. Increased packing density can be achieved by reducing the insulator thickness but that will eventually jeopardize the reliability of the capacitors since the breakdown voltage will decrease and the leakage current increase. A much better way to decrease the capacitor area is to use a dielectric material with a higher dielectric constant.

Tantalum pentoxide ($\kappa \approx 25$) was considered for gate dielectric material in MOSFETs, but, as already mentioned, due to low thermal stability and low conduction band offset, it is no longer considered as a potential high-κ material in MOSFETs. Nevertheless, Ta_2O_5 has properties that can be

beneficial in other applications, such as memory devices and metal-insulator-metal (MIM) capacitors [4]. For instance, the shift from metal-insulator-semiconductor (MIS) to MIM structures eliminates the thermal instability issue with Ta_2O_5 on Si. For ceramic bulk materials it is has been shown that by incorporating about 8 % of titanium into the Ta_2O_5, the dielectric constant is increased up to 126 [49].

HIGH FREQUENCY MEASUREMENTS

In digital logic applications, common transistor operation frequencies are hundreds of megahertz or gigahertz. However, most electrical characterization techniques are used at much lower frequency; the *C-V* curves are typically recorded below 1 MHz and standard *I-V* curves are measured at dc. Therefore it is most important to consider the frequency range above 1 MHz, in addition to the standard techniques, when characterizing the novel materials.

The vector network analyzer (VNA) is an instrument that emits a power wave into the devices under test (DUT) and measures the reflected and transmitted power wave in magnitude and phase for high frequencies, typically between 50 MHz and 40 GHz. The result is usually presented as coefficients called scattering parameters (S-parameters). The S-parameters can be converted to impedance or admittance and characteristic parameters of the DUT can be extracted, such as the dielectric constant and the dielectric loss factor (tan δ), and displayed as a function of frequency. Proper calibration of the instrument and de-embedding of parasitic components are critical for accurate and reliable parameter extraction. Further, co-planar probes and wave guide cables are used to connect the instrument to the DUT.

Basic theory states that dielectric relaxation of a material occurs at certain frequencies due to relaxation of different polarization mechanisms. For instance, relaxation of the ionic contribution to the dielectric constant is predicted to occur at around 1 THz [50]. The latter is of course a general statement, which motivates investigations of the high frequency behavior of novel dielectric materials.

4. Manufacturing and processing

INTRODUCTION

A critical phase in introducing novel materials in IC processing is the ability to fabricate the desired devices using standard equipment. Both the deposition and etching of metal gates and high-κ dielectrics are critical with respect to uniformity, selectivity, contamination, new masking materials, to mention but a few. The implementation of novel materials will most probably include more mask steps which will increase the overall integration complexity.

4.1 Deposition Methods

Materials can be deposited by a variety of processes but only the most important techniques will be briefly considered here. Various chemical vapor deposition (CVD) methods exist such as low pressure CVD, plasma enhanced CVD, metal organic CVD, and atomic layer CVD (ALCVD, also called ALD). The advantage of all CVD processes is the conformal deposition over large areas whereas negative aspects are that elevated temperature is needed and contamination from precursors is, to some extent, always incorporated into the film. The ALD process is extensively used for depositing gate stack materials such as metals, metal compounds, and dielectrics, mainly due to the precise thickness control but also because fairly low temperatures can be used (around 300 °C). Metal chlorides and organometallic (methyl-, ethyl-compounds) precursors are most often used in ALD processes, although reduced contamination have been shown by using iodine-based precursors [51, 52]. In the ALD process, layer by layer is deposited onto the substrate by alternately pulsing precursor fluxes through the deposition chamber. Between each pulse, the chamber is purged with an inert gas in order to remove by-products and/or remains of the precursors. Under optimum conditions, the growth is self-limited and the thickness increase is constant in each deposition cycle. Since the growth rate usually is lower than a monolayer in each cycle, precise thickness control can be achieved. ALD was used to deposit TiN and Al_2O_3 in Paper I, and for the gate stacks in the pMOSFETs in Paper V-VI.

Reactive sputtering is a physical vapor deposition (PVD) method. It is a plasma process that can be conducted at room temperature and is inherently contamination free. Another advantage with reactive sputtering is the versatility of the process since a variety of materials and compounds can be deposited in the same equipment. For instance, both conducting and insulating materials can be deposited, e.g. Ti, TiN, and TiO_2, by only excluding or changing the type of reactive gas. Consequently, reactive magnetron sputtering has been used to deposit both insulating high-κ (Ta_2O_5, $(Ta_2O_5)_{1-x}(TiO_2)_x$, AlN) and conducting metal gate (TiN, ZrN) materials. The disadvantage could be low step coverage and plasma damage of the growing film or of the devices on the substrate.

In the sputter deposition process, atoms are ejected from a surface (target) as a result of the bombardment of the latter by heavy energetic particles (usually argon ions). The ejected target atoms will be deposited all over the chamber, including the substrate, and form a film. In reactive sputtering, a reactive gas such as oxygen or nitrogen is introduced into the chamber. Depending on the partial pressure of the reactive gas, compound formation takes place on the substrate surface and/or on the target surface. For additional details regarding the basics of the sputter process, the reader is referred to any handbook of thin film deposition, for example [53]. Worth discussing further though, is the characteristic hysteresis effect that occurs for most reactive sputter processes when increasing and decreasing the flow of reactive gas. The hysteresis becomes obvious when studying the deposition rate, partial pressure of reactive gas, target voltage, or stoichiometry of the deposited film, and is mainly due to different sputter yields of a pure metal and its compounds. The deposition rate varies with the reactive gas flow. At low supply of reactive gas, a pure metallic target is sputtered at high rate, while at high flow, the compound is formed on the target resulting in lower sputter rate. Most often, and especially for industrial applications, a high-rate deposition process is desirable to ensure high throughput while at the same time form a stoichiometric compound on the substrate. Hence, the characteristics of each reactive sputter process are crucial in order to attain desirable film quality.

To facilitate the understanding of the reactive sputter process and also to have a tool for simulating the process, a theoretical model was developed by Berg *et al.* [54]. Basically, the model uses balance equations at steady state for the flow of gases, gas consumptions at the target surface and at the substrate surfaces as well as of the sputtered fluxes. The co-sputtering process of Ta and Ti in an argon and oxygen ambient was carefully investigated in Paper VIII where pulsed dc reactive magnetron sputtering was utilized to deposit tantalum pentoxide and titanium incorporated Ta_2O_5. Both the oxygen flow and the current to the titanium target were varied in order to

find optimal deposition parameters. The process was modeled and simulated in order to study the hysteresis effect on the stoichiometry. The model very well describes the characteristic hysteresis behavior of the reactive sputter process and predicts that the metal composition exhibits a hysteresis effect. The latter is a consequence of the difference in reactivity at the two targets, which makes the deposition rather complex in the transition region between metallic and compound mode.

For sputter depositing TiN_x and ZrN_x, it was important to find out the transition region between the metallic and compound region. This was accomplished by either monitor the target voltage or measure the film resistivity. A sudden change in target voltage occurs and a minimum in resistivity is expected when entering the compound region. Another viable method for these metal-nitride compounds is simply to visually examine the samples. A bright yellow-golden color is seen for compound films, which turns more dark as more nitrogen is added.

4.2 Dry Etching

Dry etching is the selective removal of one material with respect to another by using reactive species in a gas phase. The reactive species are created in a plasma, which react with the substrate material and form volatile products that leave the system. Depending on the process and material to be etched, different gases are utilized where the most common are based on chlorine, fluorine, or bromine. Important parameters in etching are selectivity, anisotropy, and uniformity. Selectivity is simply the ratio of the etch rate between the material to be etched in relation to mask materials or stopping layers. Anisotropy, or directionality, is the ratio between the vertical and horizontal etch rate. An isotropic etch could cause under-etch and thus loss in dimension control. It is also important to have sufficient uniformity, both across a wafer such that the over-etch time can be minimized, as well as to maintain a constant etch rate from one wafer to another.

The dry etching mechanism can be divided into chemical and mechanical etching where the key mechanism in the former is the formation of volatile etch-products while in the latter is the material erosion by ion bombardment of energetic species from the plasma to the substrate. Further, chemical etching can be highly selective whereas mechanical etching is generally nonselective.

A combination of the two mechanisms results in *ion-enhanced etching*, where energetic ions transfer energy to the surface which enhances the chemical reactions at the surface. Nearly an order of magnitude higher etch rate can be achieved in ion-enhanced etching, compared to the individual

etch rates [55]. In *inhibitor controlled etching*, a very thin passivating film is formed on all surfaces. The film is not chemically etched but when energy is supplied to the surface through energetic ions, the film can be removed. Since the ion bombardment always is perpendicular to the surface, horizontal areas will be cleared from the protecting film while vertical surfaces will be left unaffected. This makes it possible to achieve highly anisotropic etching [56].

DRY ETCHING SYSTEMS

The plasma etching is commonly carried out at low pressures and various chamber setups are available. The ordinary etching system is the capacitively driven rf diode system with the power connected to the electrode where the wafer is positioned and the counter electrode is grounded, as is the whole chamber. These systems are referred to as reactive ion etching (RIE). The major drawback with RIE systems is that the plasma density and ion energy cannot be varied independently, which has lead to the development of various triode systems where two independent power supplies are used. Further progress resulted in high-density plasma systems where the plasma density is typically one order of magnitude higher than in a RIE system, resulting in higher etch rates. However, the primary reason for using high-density plasma systems in modern IC fabrication is the feasibility to operate the process at reduced pressures, thus enabling high directionality. One example is the inductively coupled plasma (ICP) system where the power from one rf source is inductively delivered to the plasma while the bias (ion energy) is capacitively controlled by the other power supply connected to the substrate electrode.

4.2.1 Etching of Ta_2O_5

Reactive ion etching in fluorine-based chemistry was carried out by using both the diode RIE system and the triode ICP system in order to realize a capacitor structure consisting of poly-Si, Ta_2O_5, and SiO_2 (Paper IX). The etch rates of the three materials were examined for a variety of process parameters such as bias voltage, ICP power, pressure, gas flow of CHF_3 and the addition of O_2, as well as the temperature on the substrate chuck and on the surrounding chamber walls.

When the CHF_3 dissociates in the plasma, CF_x radicals and atomic fluorine are created. The fluorine reacts with the Ta and forms TaF_5 and the oxygen in the Ta_2O_5 will react with the fluorocarbon species and various CO_x and COF_x molecules are formed. The created species are volatile, hence pumped out of the system. Under certain conditions, the CF_x will be deposited in a polymer-like film on all surfaces in the chamber, including the

wafer, and will limit the etch rate. The ion bombardment, controlled by the substrate bias, and the amount of oxygen will determine the thickness of this polymer film, which was found to strongly correlate with the etch rate, see Fig. 10.

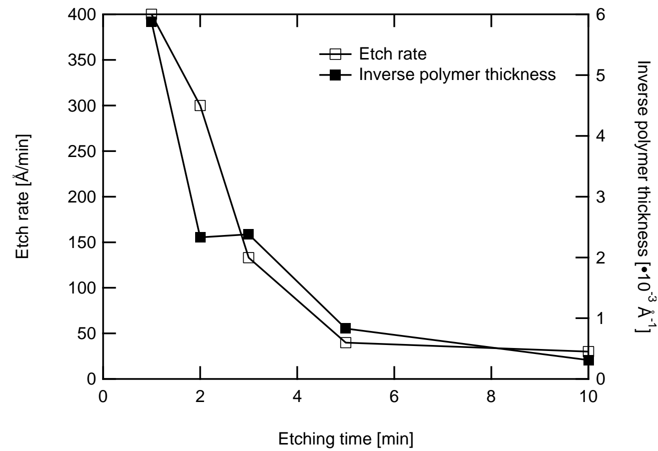

Figure 10. Etch rate of Ta_2O_5 and inverse of polymer thickness as a function of etching time.

Another parameter that will influence the thickness of the polymer film on the wafer is the temperature on the substrate and on the surrounding chamber walls. Less polymer will be deposited on a surface with high temperature. Hence, as the temperature is increased on the chamber walls, more polymeric species will be present in the plasma, which results in a thicker polymer film on the cooler substrate. During etching, the chamber is heated and it was found that the starting temperature of the chamber walls had a large influence on the etch rate. For instance, the etch rate is more than twice as high for SiO_2, if the starting temperature on the chamber walls is reduced from 250 °C to 150 °C.

5. Device Characterization

5.1 Metal Gates in MOS-Devices

The work function of a material is a measure of the energy required to extract an electron from the inside of a bulk solid to the outside. It is defined more precisely as the energy difference between the state in which an electron has been removed to a point sufficiently far outside the surface so that the image force is negligible and the state in which the electron is in the bulk. The work function can be measured by a variety of methods. For the gate stack in MOS-devices, two methods can be used and is described in the next sections followed by recent results.

5.1.1 Work Function Extraction Methods

THE *C-V* METHOD

The *C-V* method requires capacitors with multiple oxide thicknesses. The flatband voltage from a recorded *C-V* curve is extracted and plotted for the different oxide thicknesses. If the charges in the oxide are independent of the oxide thickness, i.e. can be modeled as an effective oxide charge concentrated close to the SiO_2/Si interface, then Eq. (1) is valid (repeated here):

$$V_{fb} = \phi_{ms} - \frac{Q_{ox}}{\varepsilon_0 \kappa_{ox}} T_{ox} \qquad (9)$$

An example is shown in Fig. 11 for the TiN/SiO_2 stack. The work function of the semiconductor is calculated from the energy band by knowing the doping concentration in the substrate:

$$\phi_s = \chi + \frac{E_g}{2} \pm \varphi_B \qquad (10)$$

The plus (minus) sign is used for *p*-type (*n*-type) substrate. A least squares fit of the V_{fb} vs. T_{ox} data is extrapolated to zero oxide thickness and the

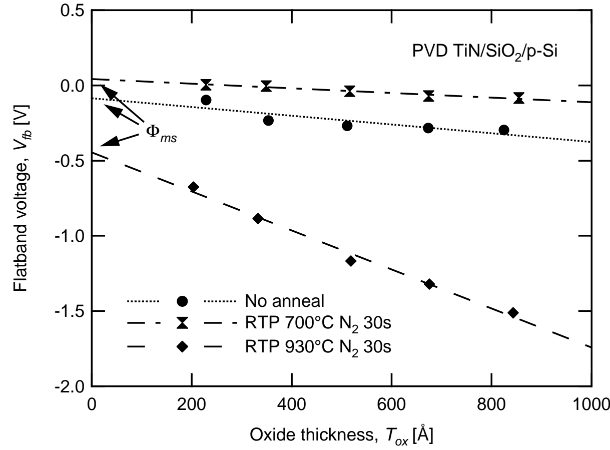

Figure 11. Extracted flatband voltage as a function of oxide thickness. The work function difference between the gate electrode and the semiconductor is the intercept at zero oxide thickness. The slope corresponds to the density of oxide charge in the MOS device.

intercept gives the ϕ_{ms} and the work function is easily calculated. From the slope of the fit (Fig. 11), it is possible to extract the density of oxide charge.

In order to reach reliable values of the extracted work function, errors must be minimized. One source to errors can be the charges in the oxide, which could vary from wafer to wafer when oxidized to different thicknesses. To avoid such issue, a wafer with thick oxide can be partially wet etched in a solution of buffered hydrogen fluorine in steps across the wafer in order to achieve the multiple oxide thicknesses. The metal gate is then deposited over the whole wafer. Hence, the work function can be extracted from one wafer having the same SiO_2/Si interface and virtually should have the same amount of oxide charge. This process scheme also minimizes any variation in composition and/or structure between different depositions of the metal gate.

When characterizing high-κ gate stacks, it is important to be aware of the charges in the different interfaces and layers that the stack comprises. Usually there is an interfacial layer between the high-κ and the silicon substrate, and charges can be in any of these interfaces as well as in any of the bulk dielectrics. Consequently, the extraction of the work function might be more complicated and several stacks with different high-κ/SiO_2 thickness combinations might be needed to accurately determine the work function [57].

THE *I-V* METHOD

The *I-V* method uses the FN tunneling mechanism of electrons from the electrode into the conduction band of the oxide, which was illustrated in Fig. 7. The tunneling current density was given in Eq. (3) but is repeated here:

$$J_{FN} = \frac{q^3 {E_{ox}}^2 m_0}{8\pi h \phi_B m^*} \exp\left(-\frac{8\pi\sqrt{2m^*}\,\phi_B^{3/2}}{3qhE_{ox}} \right) \tag{11}$$

where ϕ_B is the barrier height between the electrode and the conduction band in the oxide. The electric field has been modeled as:

$$E_{ox} = \frac{V_g - V_{fb}}{T_{ox}} \tag{12}$$

Figure 12 illustrates the method, where the experimental and modeled gate current density for the ALD TiN/SiO_2 stack is shown for both gate and substrate injection. To arrive at the work function of the metal gate electrode, the electron affinity of the oxide has to be added to the extracted value of the barrier height. The latter makes the method rather sensitive to the gate stack under investigation. For SiO_2, the electron affinity is known (0.9 eV), but for high-κ materials and for stacked gate dielectrics, the interpretation of how to relate the work function to the extracted barrier is not straightforward. In fact, the FN tunneling model in its simplest form is uncertain when dealing with multi-layer stacks having ultra-thin interfacial layers.

Sufficiently thick oxides are required to use this method in order to avoid direct tunneling, which does not obey Eq. (11). For practical purposes, the oxide cannot be too thick either since the instrument supplying the gate

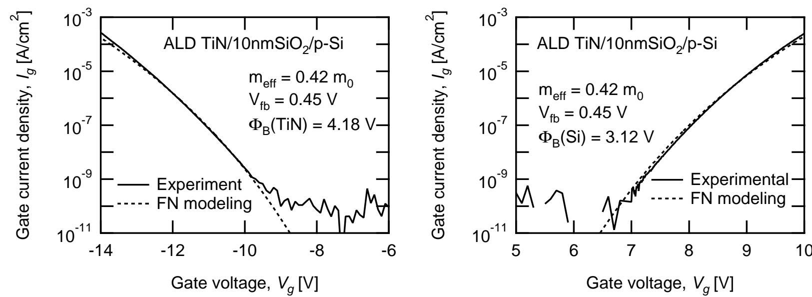

Figure 12. I_g-V_g characteristics of the ALD TiN/SiO_2/p-Si stack for both gate (left) and substrate (right) injection. The FN tunneling current is modeled and fitted to the data. The barrier height and work function of TiN is 4.18 eV and 5.08 eV, respectively, whereas the barrier height between the conduction bands in Si and SiO_2 is 3.12 eV.

voltage usually never handles voltage in excess of 100 V. For silicon dioxide films an electric field above ~ 8 MV/cm is necessary to have FN tunneling (of course dependant on the electrode/dielectric barrier height). Consequently, appropriate SiO_2 thickness ranges from 5-6 nm up to 30-40 nm.

The value of the electron effective mass in the SiO_2 conduction band is debatable. It is reported to vary from $0.32 \cdot m_0$ to $0.86 \cdot m_0$ depending on theoretical model [58]. In addition, the electron effective mass can be affected by the energy of the electron in the conduction band [59], as well as the oxide thickness [60-62]. At low energies, thick films (> 3-4 nm), and for most models, the effective mass of the electron is between $0.50 \cdot m_0$ to $0.40 \cdot m_0$. For the extraction of work functions reported in this thesis, the electron effective mass is set to $0.42 \cdot m_0$. The effective mass in high-κ gate stacks is neither definite, making work function extraction from such gate stacks challenging.

One way to check the validity of the *I-V* extraction method is to measure the substrate injection current where the barrier height between the silicon substrate and the silicon oxide is extracted (Fig. 12). This barrier should be consistent between different gate stacks and in agreement with literature values for accurate modeling.

An additional issue to be aware of is that charging during measuring might occur and must be taken into account during certain circumstances. Due to charging, the flatband voltage will shift, which will change the electric field in the oxide [Eq. (12)] and alter the band diagram. The result is seen in that the current density of the experimental curve deviates from the FN modeled current density at high gate voltages (or corresponding electric fields).

5.1.2 Results on Metal Gates

VARIATION OF NITROGEN

The most promising results for implementing the reactively sputtered TiN_x and ZrN_x metal gate technology in MOSFET fabrication is the fact that the work function can be varied by more than 0.6 eV, when depositing the different metal gates at different nitrogen gas flow (Γ_{N2}). This is visualized in Fig. 13 for both TiN_x and ZrN_x films. However, implementing any of these metal systems into a CMOS process requires dual deposition steps, which is equal to depositing two metals of any kind. The promising part is that it might be possible to deposit the low-nitrogen-content film and then utilize ion-implantation of nitrogen to modify the work function, similar to the complementary poly-Si process.

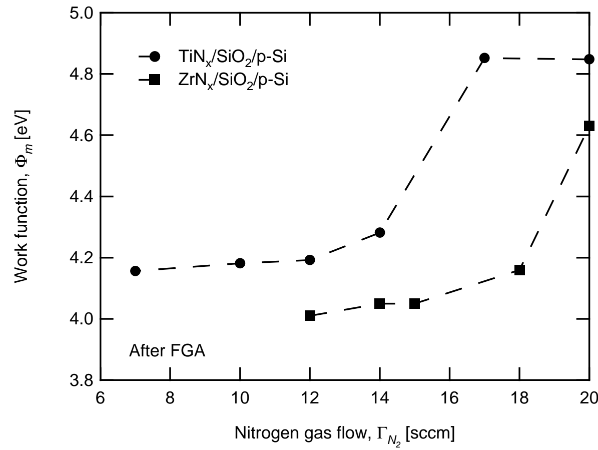

Figure 13. Extracted work function of sputtered TiN_x and ZrN_x metal gate electrodes in MOS capacitor devices as a function of nitrogen gas flow used during deposition.

THERMAL ANNEALING EXPERIMENTS

The extracted work function seems to change upon thermal annealing. For ALD TiN, monotonously decreasing work function was seen (Paper I), whereas for PVD TiN, first a slight increase and then a reduction in work function was seen (Paper II), see Fig. 14a. For the TiN_x gates, huge variation in work function ($\Delta\Phi_m \approx 0.6$–0.7 eV) is seen upon annealing for certain nitrogen concentrations (Γ_{N2} = 12 and 14 sccm), see Fig. 14b.

Generally, when annealing the TiN gate stacks above 800 °C, the extracted work functions are close to mid-gap values irrespective of deposition method (Fig. 14a) or for nitrogen content, see Fig. 15.

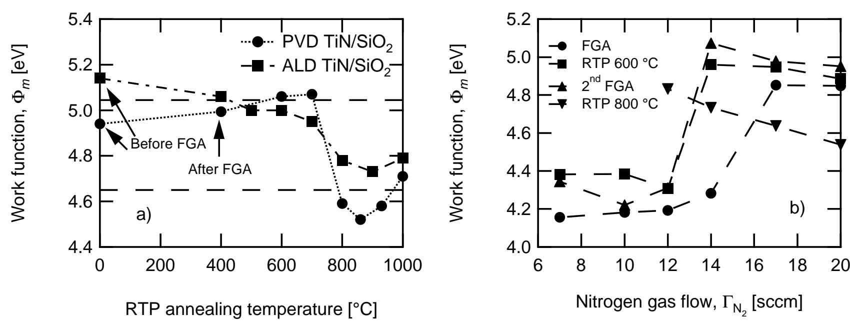

Figure 14. a) Work function of ALD and PVD TiN as a function of RTP annealing temperature. b) Work function of TiN_x as a function of nitrogen gas flow for various annealing conditions.

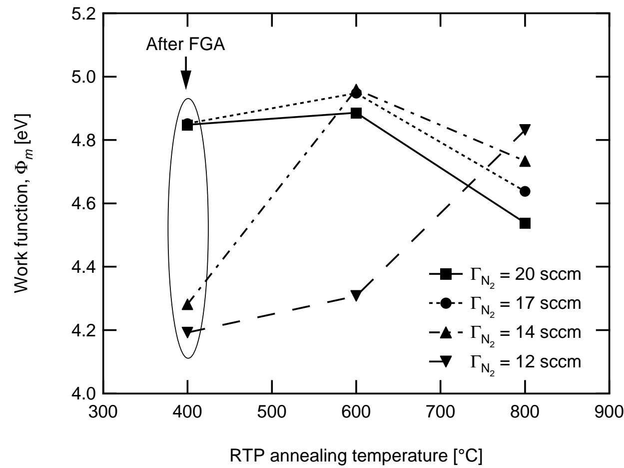

Figure 15. Variation in extracted work function with RTP annealing temperature for TiN_x metal gate electrodes with varying nitrogen content.

MATERIAL CHARACTERIZATION

The various metal gate stacks have been physically examined by employing the following methods: secondary ion mass spectrometry (SIMS), x-ray diffraction (XRD), high-resolution transmission electron microscope (HRTEM), scanning electron microscopy (SEM), electron energy loss spectrometry (EELS), x-ray photoelectron spectroscopy (XPS, also called electron spectroscopy for chemical analysis, ESCA), and Rutherford backscattering (RBS). Generally, no correlation between physical parameters and the change in work function upon annealing has been found for the stacks.

Analysis by XPS was performed on the TiN/SiO_2 stack for various RTP annealing temperatures. The Ti 2*p* peak was monitored during depth profiling by sputtering through the TiN electrode. Figure 16 summarizes the intensities of the Ti 2*p* peak close to the TiN/SiO_2 interface after the RTP anneals. Obviously, no chemical shift occurs, which means that the Ti is bonded to the same element for all annealing temperatures. Hence, the XPS analysis could not provide an explanation to the change in work function. Further, smooth interfaces were seen for PVD TiN_x/SiO_2 stacks (HRTEM), see Fig. 17, and no nitrogen was observed in the SiO_2 for neither PVD TiN/SiO_2 nor ALD TiN/SiO_2 stacks, as analyzed by EELS and SIMS, respectively. It was also concluded by XRD analysis that the change in extracted work functions is not correlated to a change in crystalline orientation of the TiN films or the appearance of any other crystal phases.

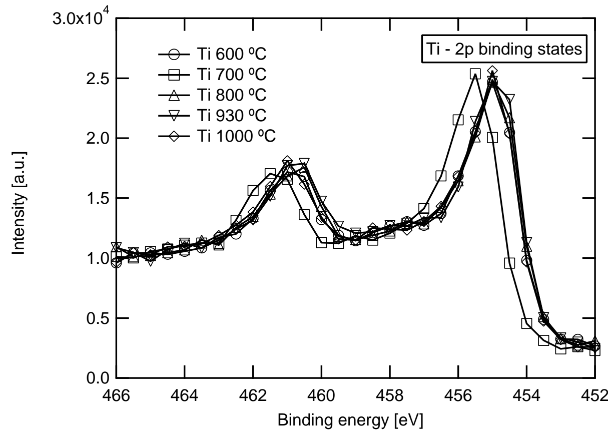

Figure 16. Binding energy of the Ti 2p binding state, close to the TiN/SiO_2 surface, for several RTP annealing temperatures. No significant chemical shift occurs.

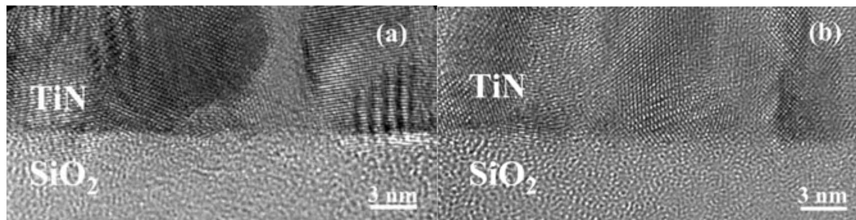

Figure 17 High-resolution transmission electron micrographs of the TiN_x/SiO_2 interface for TiN_x films deposited at nitrogen flows of (a) 12 sccm and after RTP at 600 °C, and (b) 17 sccm (no anneal).

RESISTIVITY

The flow of nitrogen gas during the reactive sputtering is not only affecting the work function of the TiN_x and ZrN_x thin films, but also affects the resistivity, see Fig. 18. The change in resistivity with nitrogen gas flow is similar for the different metal compounds, and there is a minimum of 120 and 70 μΩcm for TiN_x and ZrN_x films, respectively, when deposited in the beginning of the compound mode regime. For further increase in nitrogen gas flow, there is an obvious increase in resistivity. The latter cannot be attributed to any change in the crystal structure for the TiN_x case.

Annealing of the TiN_x film reduces the resistivity slightly, which could be due to a more compact film with larger grains, hence better conduction. The behavior of the ZrN_x film upon annealing is different since after RTP at 600 °C an increase is seen, and further annealing at 800 °C decreases the resistivity. This could be due to competing events where the former might be

caused by incorporation of contamination species whereas the latter may be because of densification of the ZrN_x film at high temperature.

Optimization of the reactive sputter deposition process results in enhanced resistivity. For instance, by depositing the TiN_x films at reduced pressure, a slightly lower resistivity than was shown in Fig. 18 is observed. It might be possible to achieve further reduction in resistivity, but operating the sputter process at lower pressures involves higher energy transfer to the growing film, which might result in degraded device performance. The main objective of the investigations in question for this thesis has been on the work function of metal gates hence, deeper examination of the deposition process with respect to the resistivity has not been carried out.

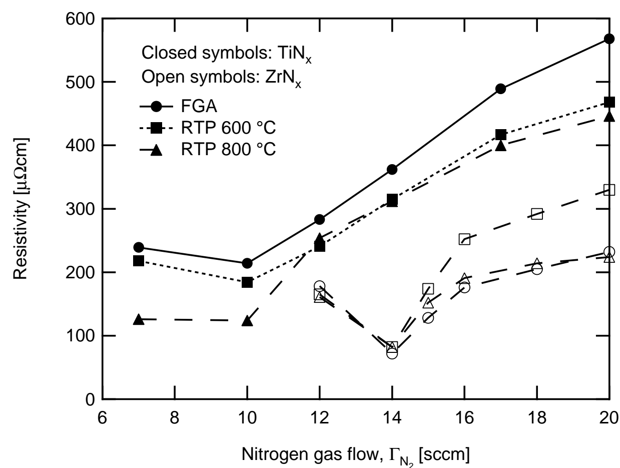

Figure 18. Resistiviy of TiN_x and ZrN_x as a function of nitrogen gas flow during deposition of the different films.

5.1.3 Discussion of the Work Function of Metal Gates

The increase in work function with annealing temperature for sputter deposited TiN samples and TiN_x and ZrN_x samples deposited at intermediate nitrogen gas flow, could depend on a gradient in nitrogen concentration in the film thickness. It was discovered visually that thinner ZrN_x films exhibited a more metallic nature whereas thicker films were more compound (golden color), for the same process parameters – the only variable was the deposition time. This could be due to non-steady-state during the initial deposition. The deposition was carried out by pre-sputtering the target in both metallic mode (i.e. pure argon) and in appropriate compound mode for several minutes each. The shutter was then removed and the actual deposition of the wafer took place. A viable explanation for the varying film

appearance might be that the removal of the shutter causes a change in the plasma condition and a short time interval is needed before steady-state is recovered. Since the same deposition process is used for TiN films, a similar nitrogen gradient could be present in them as well.

The metallic behavior of the interface could result in that a lower value of the work function is extracted. The possible gradient in nitrogen concentration might be reduced by a diffusion mechanism during the first annealing steps, making the metal gate/SiO_2 interface more nitrogen-rich and thus a higher work function is extracted. The lack of increase in work function of ALD TiN could be due to absence of a nitrogen gradient since the ALD process is saturated in each cycle.

The reduction in work functions after annealing above about 800 °C (Figs. 14 and 15) is also seen for many other metal gates, mainly on SiO_2 dielectrics. A plot of the variation of the metal gate work function with annealing temperature, similar to the one presented in [23], is shown in Fig. 19. Elliptical symbols are for metal gates on SiO_2 dielectrics while square-shaped symbols are for HfO_2 high-κ dielectrics. It is realized that the work function of all metal gates on SiO_2 except Ru ends up with a mid-gap value while metal gate/HfO_2 stacks changes slightly and arrive at a somewhat lower value. The work function of HfN on both dielectrics is about mid-gap before and after annealing.

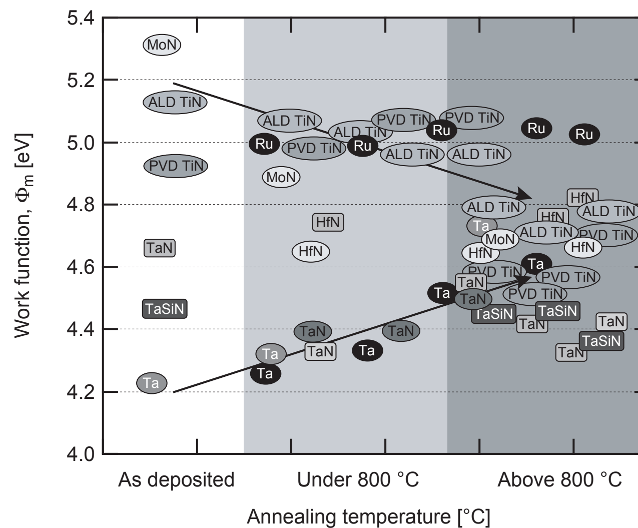

Figure 19. Work functions of various prospective metal gate technologies as a function of annealing temperature. Elliptical symbols are for metals on SiO_2 whereas square-shaped symbols are for HfO_2 dielectrics.

The present explanation is based on Fermi level pinning due to the existence of a high density of extrinsic interface states. These states could be interface defects such as vacancies, variation in chemical bonding, or small compositional and/or structural variations. The model of a charge neutrality level (as discussed in Section 2.1) can be adopted here as well, and extrinsic states below the metal Fermi level become negatively charged and tends to lower the extracted work function of the metal gate electrode. Lower work function of metals on HfO_2 could be interpreted as no Fermi level pinning or as pinning to a lower value due to lower E_{CNL}.

Hence, the behavior of the TiN_x and ZrN_x stacks after annealing can be due to two competing events. The increase in work function could be attributed to the diffusion of nitrogen due to a nitrogen gradient while the reduction in work function to mid-gap values for the TiN and TiN_x films could be the result of Fermi level pinning due to the creation of extrinsic interface states.

The oxide charge in the MOS capacitor gate stack is proportional to the slope in Fig. 11. Clearly, the slope increases with RTP annealing temperature, which implicates that charges are created during the annealing steps. The latter could be an indication of simultaneous creation of extrinsic interface states that result in Fermi level pinning and the apparent decrease in work function.

For films sputtered at different nitrogen gas flows, there is also different amount of oxide charge for the various stacks. An increase in charge occurs for both TiN_x and ZrN_x gate stacks for decreasing nitrogen gas flow. Since the gate oxide virtually is the same for all stacks, the higher amount of charge must be generated by any process during the fabrication of the devices. It was found that the metal gate deposition rate correlates well to the extracted oxide charge density, see Fig. 20. Both the TiN_x and ZrN_x system exhibits the same trends, which was not considered when Paper III was written. Since the correlation is observed for two independent metal-nitride systems, it is most likely a correct observation and not a coincident. Several possible plasma damage mechanisms exist, including energetic bombardment by electrons, negative ions, or neutrals (Ar, N, H), as well as radiation by UV-light. The deposition rate in reactive sputtering relates to the degree of target poisoning, consequently, the observed variation in oxide charge should relate in the same manner, which in turn implies that the plasma damage mechanism should vary accordingly. The above mentioned mechanisms are always to some extent present in the plasma and are not believed to vary considerably depending on target poisoning. In addition, constant thickness of the TiN_x and ZrN_x films were used, which means that

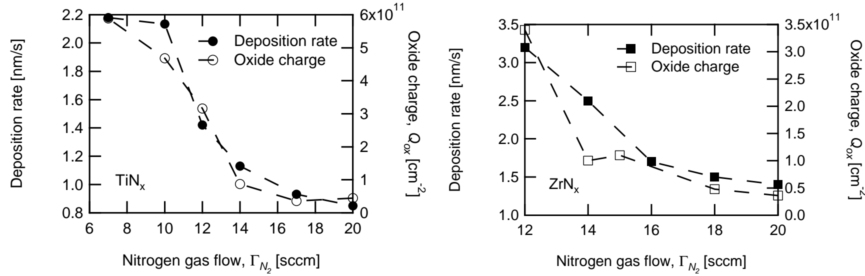

Figure 20. Deposition rate and oxide charge density as a function of nitrogen gas flow for TiN_x (left) and ZrN_x (right) metal gate electrodes.

shorter deposition times were required for the stacks with high deposition rate, i.e. the stacks with high density of oxide charge were exposed to the plasma shorter times. Hence, to date it is not clear what causes the variation in oxide charge.

5.2 Metal Gate and High-κ SiGe *p*MOS Transistors

Compressively strained SiGe surface-channel *p*MOSFETs were fabricated using ALD TiN/Al_2O_3 and TiN/Al_2O_3/$HfAlO_x$/Al_2O_3 gate stacks [63]. A schematic picture is shown in Fig. 21, where the 10 nm strained SiGe layer is shown on top of the relaxed Si buffer layer. The devices exhibit the expected enhancement in performance as compared to a reference Si channel *p*FET, see Fig. 22. However, large subthreshold slope and shift in threshold voltage from simulated value for the SiGe devices were extracted, which imply the existence of large density of interface traps as well as fixed

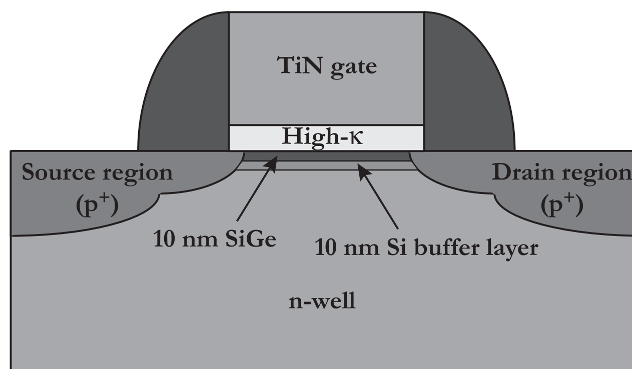

Figure 21. Schematic picture of the pMOSFET with an ALD TiN/Al_2O_3 gate stack and strained SiGe surface channel.

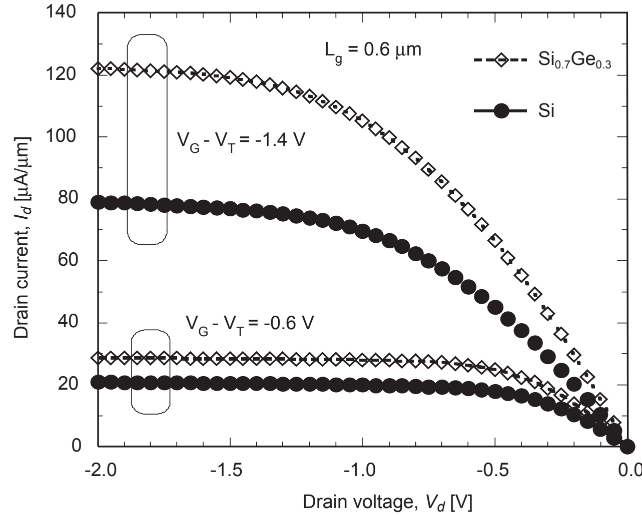

Figure 22. I_d-V_d characteristics for different gate overdrive voltages for $Si_{0.7}Ge_{0.3}$ and Si surface channel pMOSFETs with ALD $TiN/Al_2O_3/HfO_x/Al_2O_3$ gate stack. An increase by about 50 % is seen for the strained $Si_{0.7}Ge_{0.3}$ channel as compared to the Si reference.

charges. In order to improve the dielectric/SiGe interface [64], low-temperature water vapor annealing at 300 °C was conducted for successive 30 minute intervals and the devices were electrically characterized between each anneal.

The transistors were characterized by conventional I_d-V_d, I_d-V_g, and I_g-V_g measurements. From the various *I-V* characteristics, quantities such as transconductance, threshold voltage, subthreshold swing, and mobility were extracted and compared for different annealing times. In addition, charge-pumping measurements were carried out in order to extract the density of interface states. The extracted mobility was correlated to the low-frequency noise and coupled to the amount of charge in the high-κ dielectric.

5.2.1 Water Vapor Annealing Experiments

The low-temperature water vapor annealing causes a substantial shift in the threshold voltage indicating a reduction in negative charge in the Al_2O_3 layer, see Fig. 23. However, the H_2O annealing could not improve the subthreshold slope, which is in contrast to H_2O annealing of thermally grown oxide in SiGe transistors. The latter has been seen in our devices as well as for other's devices [64]. The subthreshold slope is sensitive to the density of interface states, which was investigated by charge-pumping measurements

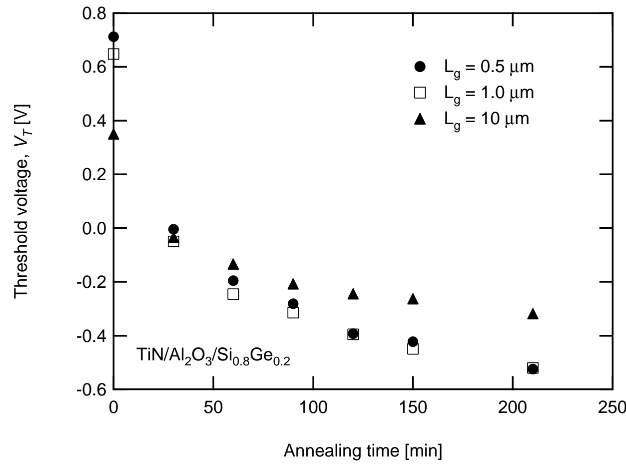

Figure 23. Threshold voltage shift after consecutive low-temperature water vapor annealing for pMOS transistors with different gate length.

where it was concluded that the interface state density remained unchanged (D_{it} = 3-5·10^{12} cm^{-2} eV^{-1}) in the high-κ *p*MOSFETs after various annealing sequences. Moreover, the ideal threshold voltage was calculated to be around -0.4 V, which indicates that the 0.5- and 1-μm transistors likely contain a positive oxide charge after annealing longer than about 120 min.

The TiN/Al_2O_3 gate stack was further investigated by calculating the effective mobility (μ_{eff}) from I_d-V_g characteristics [Eq. (4)]. The low-field mobility (μ_0) was extracted by modeling the effective mobility as $\mu_{eff} = \mu_0$ / $(1+\Theta \cdot (V_g - V_t))$, where Θ is the mobility attenuation coefficient, and visualized as a function of annealing time, see Fig. 24. It is realized first of all that the mobility is different depending on the transistor gate length. It is also observed that the mobility increases with annealing time, i.e. with decreasing density of negative oxide charge (cf. Fig. 23). This could be due to reduction of negative charges or screening of negative charges by introduction of positive charges. In either case, the Coulomb scattering is reduced and the low-field mobility increases. For the 0.5- and 1-μm transistors, the low-field mobility decreases after annealing longer than about 120 minutes, which is consistent with the possible introduction of positive charges that was mentioned above. The latter will give rise to higher Coulomb scattering and hence lower mobility.

Due to charging of the devices, care has to be taken in the measurement procedures in order to avoid discrepancies. Figure 25 illustrates the V_t instabilities where I_d-V_g traces are shown for various stress times. First an initial long trace was recorded by sweeping the gate voltage from +1 to –1 V

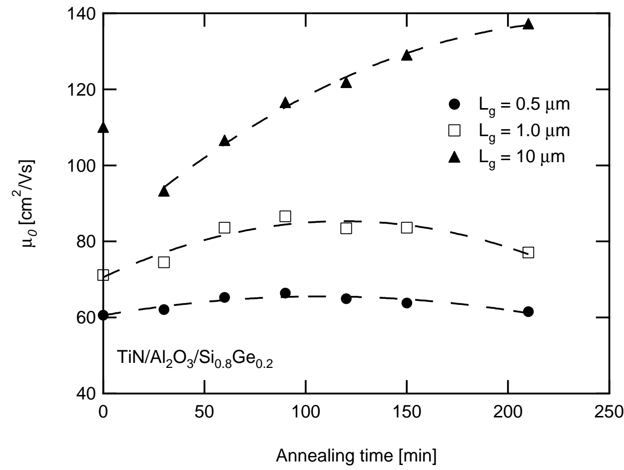

Figure 24. Low-field mobility versus water vapor annealing time for pMOS transistors with different gate length. (The lines are drawn as guidance for the eye.)

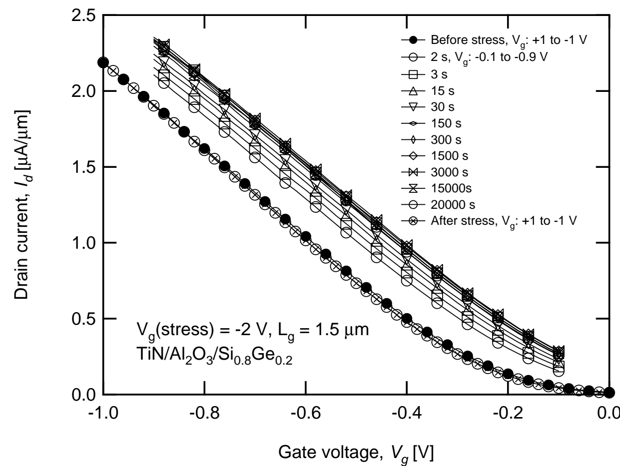

Figure 25. I_d-V_g traces after several stressing times at V_g = -2 V. Shift in threshold voltage is clearly seen due to trapping of electrons. Full recovery of the threshold instability is revealed for a final long sweep trace due to charge de-trapping.

and then, in order to avoid creation of new traps and minimize de-trapping, short traces were recorded by sweeping the gate voltage only for negative polarity (-0.1 to -0.9 V), after stressing at $V_g = -2$ V for different times. It is realized that already very short stress durations alters the threshold voltage in positive direction, indicating electron trapping, which diminish for longer

stressing times. A final long trace between +1 V to –1 V reveals a full recovery of the V_t instability due to de-trapping of charges. The latter demonstrates that the details of the measurement procedure must be carefully considered in order to extract reliable results.

5.3 Dielectric Materials

5.3.1 Electrical Characterization of AlN

Aluminum nitride thin films were reactively sputter deposited and both MIS and MIM capacitor structures were fabricated and electrically characterized. Two types of films were deposited at different plasma conditions. Highly (002)-oriented films were grown at low pressures enabling higher energy of the species bombarding the substrate, whereas amorphous films were obtained at higher pressures.

The dielectric constant of the AlN thin films is about 10 and no variation in dielectric constant between the oriented and amorphous films could be detected. Hence, the dielectric constant is not dependent on the crystallinity of the AlN. Further, a thin interfacial layer of about 20 to 30 Å is detected between the AlN and the Si substrate (the calculation of the interfacial layer is based on the assumption that the κ-value of the layer is equal to that of SiO_2). The thicker interface layer corresponds to the capacitors with oriented AlN, which were deposited at low pressure and hence higher energy of species arriving at the substrate surface. It is believed that the higher energies is responsible for breaking bonds a few monolayers deeper, as compared to the high pressure deposition case (lower energies), facilitating the formation of a slightly thicker interface layer.

I-V characteristics at various temperatures of oriented AlN films in MIS structures revealed that the leakage current mechanism is likely to be Frenkel-Poole field-enhanced thermal emission of trapped electrons in the AlN conduction band. The extracted trap energy is calculated to be about 0.6 eV below the conduction band.

The MIM structures were fabricated by growing a thick insulating SiO_2 layer followed by depositing a 3 μm thick Mo layer, which served as the bottom electrode. The AlN film was then deposited onto Mo and was always amorphous due to growth kinetics. One-port high-frequency measurements were performed on the MIM structures using a co-planar HF-probe and a network analyzer, and no frequency dispersion of the capacitance was recorded up to 10 GHz, see Fig. 26. In addition, the dielectric loss tangent

was determined to below 0.03 in the measured frequency range, comparable to literature values [65].

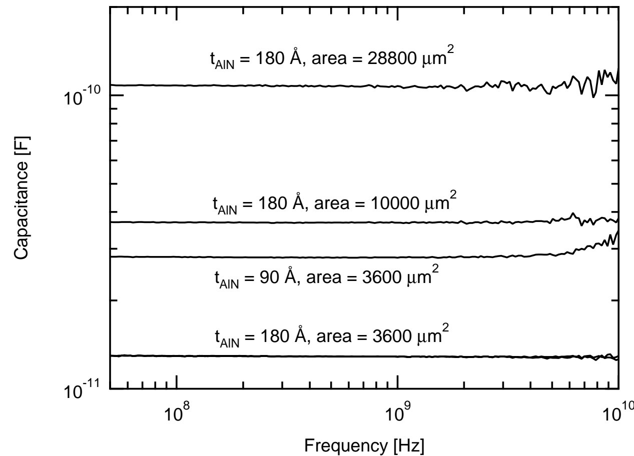

Figure 26. Capacitance versus frequency for AlN MIM capacitors.

5.3.2 Electrical Characterization of Ta_2O_5

C-V characteristics of as-deposited Al/Ta_2O_5/*n*-Si and Al/$(Ta_2O_5)_{1-x}(TiO_2)_x$/*n*-Si MOS capacitors indicates a very large amount of charges in the oxides. After a 600 °C argon anneal, proper *C-V* curves are obtained and the Al/Ta_2O_5/*n*-Si stack has a flatband voltage of about -0.2 V, which corresponds to a fixed oxide charge density of about $-6\cdot10^{10}$ cm^{-2}. However, the expected increase in dielectric constant by the incorporation of Ti is absent for annealing up to 600 °C. On the other hand, about 50 % increase in κ-value is found after annealing at 800 °C, unfortunately with a severe increase in leakage current density. For lower annealing temperatures, the leakage current density remains below 10 nA/cm^2 at an electric field of 0.5 MV/cm.

6. Summary and Concluding Remarks

Extensive investigations of potential metal gates and high-κ dielectrics have been and are globally carried out in order to sustain the scaling trends for future CMOS devices. Several metal gate candidates are investigated and, hitherto, no candidate is really more promising than another. For the gate dielectrics, HfO_2 is a favored material that is believed to be the primary choice in the forthcoming CMOS transistors.

The contribution from this thesis to the field of metal gates has been on exploring the work function of various metal gate materials and the thermal stability of them as well as on the understanding of the factors that control the work function. Work function suitable for *p*MOSFET has been achieved for TiN/SiO_2 and TiN/Al_2O_3 metal gate stacks whereas *n*-type work function has been realized for the ZrN/SiO_2 stack. Further, tunable work function is accomplished by varying the nitrogen gas flow when reactively sputter depositing TiN_x and ZrN_x films, which makes the studied metal nitride systems promising for ion implantation to achieve complimentary work function gate electrodes. However, the thermal budget is limited since alteration of the work function towards mid-gap values occurs after RTP annealing at about 800 °C. No conclusive answer is found for the latter, but several investigations (in this thesis and in the literature) point in the direction of Fermi level pinning due the creation of extrinsic states at the metal gate/dielectric interface.

As for gate dielectrics, extended use of SiO_2 has been realized in industry by introducing nitrogen into the dielectric, and further development will certainly involve initiation of other elements as well. For instance, a gradual transition from SiON to HfO_2 via HfSiON could be a feasible course of action. Several concerns with high-κ HfO_2 and Al_2O_3 dielectrics are seen in the investigated SiGe *p*MOSFETs, where substantial amount of negative charge exist in the gate dielectrics. The latter is reduced by low-temperature water vapor annealing, which also improves the device performance. However, the high subthreshold slope and especially the mobility degradation of high-κ MOSFETs needs to be solved before the implementation of such materials will become a reality. Moreover, the instability of the threshold voltage due to charging and discharging is a general issue of high-κ materials that also needs to be tackled.

Improved packing density of integrated capacitors can be achieved by using high-κ dielectrics. MOS capacitors with Ti incorporated Ta_2O_5 as high-κ dielectric exhibits a dielectric constant of about 22 for low annealing temperatures. Improvement in the κ-value with Ti content is only observed for higher annealing temperature (800 °C). However, the increase is less for the thin films than what is observed for bulk material, besides that the increase in κ-value for thin films is accompanied by unacceptable high leakage current. Another interesting dielectric material for IC applications is AlN. The investigation of MIS and MIM structures show a dielectric constant of about 10, independent of crystallinity of the AlN, as well as frequency stability up to 10 GHz. Further, the leakage current through the (002)-oriented film is found to follow the Frenkel-Poole mechanism.

Acknowledgements

The work that is summarized in this thesis would not have been completed without the assistance and encouragement from colleagues and friends around me. It is time to recognize their contribution.

First of all, I would like to express my sincere gratitude to Jörgen Olsson, for being an excellent and competent supervisor. I appreciate your skill and effort in keeping the balance between leading and leaving room for individual development.

All fellow co-authors that I have had the opportunity to work with are greatly acknowledged. Specifically the collaboration with KTH has been creative and learning.

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The person who dragged me into this business of clean room, sputtering, conferences, research, as well as writing papers and finally a thesis, really deserves my gratitude – Fredrik Engelmark. I truly enjoy that almost all of our discussions end with a big laughter – and usually that we are the champs! – even when we are talking about serious matters. "Take the line of least resistance" is our adage and you have made it particularly easy for me. Thank you for all great times, both on and off work!

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Jörgen Westlinder
Uppsala, 27 September 2004

Summary in Swedish

Undersökning av nya metalliska och dielektriska material för CMOS-tillämpningar

Skalning (storleksreducering) av fälteffekttransistorer (FET) och andra mikroelektroniska komponenter har pågått under flera årtionden, där de främsta drivkrafterna är ökad beräkningshastighet och billigare integrerade kretsar. Metall-oxid-halvledar-transistorer (eng. metal-oxide-semiconductor field-effect transistor, MOSFET) uppfanns i mitten på 1960-talet och har sedan dess varit den fundamentala byggstenen i mikroprocessorer och minneskretsar. För att uppnå lönsamhet och ökad prestanda hos varje ny generation av mikroprocessorer, förminskas de ingående komponenterna kontinuerligt vilket ställer oerhörda krav både på tillverkningen och på de ingående materialen. Som ett exempel kan nämnas att ”gate”-längden i 1970-talets början var ungefär 10 µm och idag har den minskat med en faktor 200, till 50 nm.

Grunden till framgångarna inom fälteffektkomponenter är den överlägsna prestandan hos kiseldioxid/kisel (SiO_2/Si) systemet, vilket framställs genom termisk oxidering av Si vid hög temperatur (mellan 800 och 1100°C). Systemet har utvecklats och förfinats sedan MOSFET:ens ursprung och idag kan en närmast perfekt gränsyta mellan det enkristallina Si-substratet och den amorfa och elektriskt isolerande SiO_2 uppnås. Storleksreduceringen medför att geometrier och parametrar i MOSFET-strukturen minskar, alla med i stort sett samma faktor, och riktlinjer för hur framtida transistorers prestanda ska uppnås har tagits fram av en sammanslutning av världens största halvledartillverkare (Semiconductor Industry Association, SIA), som vartannat år ger ut riktlinjerna i skriften International Technology Roadmap for Semiconductors (ITRS).

Med fortsatt takt av skalningen förutspås en tjocklek av det dielektriska SiO_2-skiktet på ca 10 Å inom en snar framtid. Ett sådant tunt skikt består endast av några få atomlager och den isolerande förmågan blir närmast obefintlig då direkttunnling av elektroner blir markant, d.v.s. läckströmmen

och därmed förlusterna blir oacceptabelt höga. För att bibehålla prestandan hos transistorerna men minska läckströmmarna är det önskvärt att använda ett dielektriskt material med högre dielektrisk konstant (κ-värde, eng. high-κ material). Ett ”high-κ” material kan göras tjockare än kiseloxiden men med ekvivalent kapacitansvärde, d.v.s. kontrollen över transistorns egenskaper består medan läckströmmarna minskar.

Att införa nya material i det väletablerade SiO_2/Si systemet sker inte helt utan svårigheter. Det nya dielektriska materialet måste uppvisa jämförbara eller bättre egenskaper gentemot SiO_2 i form av bl.a. termisk stabilitet mot kisel och andra material i transistorn samt elektriska egenskaper, där det senare innebär låg densitet av laddningar och fällor i dielektrumet förutom låg läckström. Även andra områden har användning av material med hög dielektrisk konstant. Ett exempel är integrerade kondensatorer där ett material med högre dielektrisk konstant inte bara sänker läckströmmarna utan också kan medföra reducerad area och därmed högre packningsdensitet i minneskretsen.

En annan del i MOSFET-komponenten där nya material måste införas är ”gate”-elektroden. Vanligtvis tillverkas den av polykristallint kisel (poly-Si), men vid skalning uppkommer effekter som utarmning och hög resistans i poly-Si-elektroden vilket gör att en metall eller metallförening är att föredra. En viktig parameter hos ”gate”-elektroden är dess utträdesarbete vilket bestämmer tröskelspänningen hos transistorn, d.v.s. spänningen där transistorn slår på eller av samt även nivån på läckströmmen hos transistorn vid avslaget tillstånd. För en konventionell komplementär MOSFET, ska utträdesarbetet hos den/de ersättande metallen/metallerna vara jämförbara med utträdesarbetet hos de högdopade p+/n+ poly-Si elektroderna. Vidare måste de nya materialen vara termiskt stabila och kompatibla med övriga material vid tillverkningen.

Denna avhandling omfattar både tillverkning och karaktärisering av såväl metalliskt ledande material som elektriskt isolerande material med hög dielektrisk konstant för att utröna deras tillämpbarhet i framtida integrerade kretsar. Mer specifikt avhandlas bestämning av utträdesarbetet och resistivitet samt termisk stabilitet hos de metalliska föreningarna TiN och ZrN, som tillverkats med olika deponeringsmetoder (ALD och PVD) och med olika innehåll av kväve. Dielektriska material såsom Ta_2O_5, $(Ta_2O_5)_{1-x}(TiO_2)_x$, AlN och Al_2O_3 har utvärderats i både MOS-kondensatorstrukturer och MOSFET-komponenter med avseende på läckströmmar, dielektrisk konstant, termisk stabilitet samt tillverkning (både deponering och etsning). Diverse materialanalyser har utförts på de olika materialen för att stödja slutsatserna.

RESULTAT

Utträdesarbetet hos TiN, deponerat med ALD eller med PVD vid höga kväveflöden och för värmebehandlingar under 800°C, är omkring 5 eV vilket kan vara lämpligt för att ersätta *p*+ poly-Si i *p*MOSFET-komponenter. För högre värmebehandlingstemperaturer sjunker det uppmätta utträdesarbetet till 4.7-4.8 eV vilket gör materialet mindre lämpat för standardtillverkade *p*MOS-transistorer. Det ovan nämnda gäller för TiN deponerat på SiO_2 men detsamma gäller även för ALD TiN deponerat på Al_2O_3. Utträdesarbetet för TiN som funktion av kvävgasflöde vid deponering uppvisar en markant ökning om ca 0.6 eV när flödet ändras från 14 till 17 sccm, vilket gör TiN intressant som en komplementär metallelektrod, dock med ovan nämnda temperaturbegränsning vid tillverkningen.

Resistiviteten för TiN deponerat vid olika kvävgasflöden ökar som funktion av kväveflödet med ett minimum i resistivitet på ungefär 120 $\mu\Omega$cm. Detsamma gäller även för ZrN, dock med en lägsta resistivitet på ca 70 $\mu\Omega$cm. Det uppmätta utträdesarbetet för ZrN deponerat vid låga kväveflöden är runt 4 eV vilket innebär att det är en lämplig kandidat till att ersätta *n*+ poly-Si i *n*MOS-komponenter.

Fördelarna med att använda både en metall och ett ”high-κ” material studerades genom att tillverka *p*MOS-transistorer bestående av ALD TiN och Al_2O_3. Substratet hade ett ytskikt av kompressivt spänningssatt SiGe. Fördelen med att använda kompressivt SiGe som aktiv kanal är att hålmobiliteten är högre än i en konventionell Si-kanal. SiGe-transistorerna uppvisade goda elektriska egenskaper med högre ”drain”-ström än kontrollkomponenter med Si-kanal. Ingen utarmning kunde påvisas i metallelektroden. Dock avslöjades en hög subtröskellutning vilket indikerar en hög densitet av tillstånd i gränsskiktet mellan Al_2O_3- och SiGe-kanalen. Värmebehandling i vattenånga vid låg temperatur (300°C) har visat sig vara effektiv för att reducera gränsskiktstillstånd för termiskt grodd oxid i SiGe-transistorer, varför samma behandling utfördes för dessa metall/”high-κ” *p*MOS-komponenter. Tillstånden i gränsskiktet gick ej att avlägsna med vattenångebehandlingen, men däremot uppmättes ett negativt skift i tröskelspänning vilket betyder att densiteten av negativa fasta laddningar i Al_2O_3-filmen reducerades.

Aluminiumnitrid är såväl ett piezoelektriskt som ett dielektriskt material, varför det har funnit tillämpningar inom akustiska filterapplikationer. Här studerades dock det elektriska beteendet hos kristallint och amorft AlN i både MIS- och MIM-kapacitansstrukturer. Mätningarna visade att den dielektriska konstanten är oberoende av kristallstrukturen då både de kristallina och amorfa filmerna uppvisade liknande κ-värde på omkring 10. Läckströmmen är starkt temperaturberoende och genom att tillämpa Frenkel-

Poole formalism kunde läckströmmen konstateras bero av termisk emission av elektroner via fällor ca 0.6 eV under ledningsbandet i AlN-filmen.

Så gott som alla reaktiva sputtringsprocesser karaktäriseras av en hysteres när flödet av reaktiv gas ökas respektive minskas. Detta gör att processen är synnerligen komplex och för att underlätta förståelsen samt kunna förutspå beteendet hos nya processer har en beräkningsmodell tidigare utvecklats. Denna befintliga modell användes för att simulera den reaktiva deponeringsprocess där tantal och titan samtidigt sputtras i en atmosfär av argon och syre. Det visade sig att det finns en hysteres i sammansättningen hos den deponerade filmen under specifika flödesförhållanden av reaktiv gas. Utifrån simuleringarna kunde den komplexa hysteresregionen undvikas vid tillverkningen av $(Ta_2O_5)_{1-x}(TiO_2)_x$ MOS-kondensatorer.

Elektrisk utvärdering av MOS-kondensatorstrukturerna tillverkade av tunna filmer av Ta_2O_5 och titanlegerad Ta_2O_5 visar att den dielektriska konstanten inte varierar nämnvärt med Ti-innehållet. Det senare är till skillnad mot vad som uppvisats för homogena material där en tillsats av 8 % Ti till Ta_2O_5 ger en ökning av dielektricitetskonstanten från 35 till 126. Den dielektriska konstanten för de olika tunna filmerna efter värmebehandling vid låg temperatur är ungefär 22. Om man vid värmebehandlingen ökar temperaturen till 800°C, sker en ökning av dielektricitetskonstanten med ca 50 %, dock med en avsevärd och oacceptabel ökning av läckströmmen genom filmerna. Begränsas temperaturen vid värmebehandlingen av komponenterna till 600°C, erhålls låga läckströmmar och låg densitet av laddningar i filmerna.

En nödvändighet för att skapa en kondensatorstruktur är att de ingående materialen ska kunna etsas med tillfredställande selektivitet gentemot varandra. Därför studerades etshastigheten hos Ta_2O_5, SiO_2 och poly-Si som funktion av substratspänning, effekt, processtryck, gasflöden och temperaturen hos både kammarväggen och substratet. En polymeriserande gas användes (CHF_3), vilket innebär att en tunn polymer bildas på alla ytor i kammaren under vissa förhållanden, som till viss del hindrar etsningen. Det visade sig att bl.a. temperaturen bestämmer hur mycket och var denna polymer bildas. Till exempel, om starttemperaturen på kammarväggen höjdes från 150°C till 250°C, minskade etshastigheten för SiO_2 till hälften. Detta p.g.a. att en mindre mängd polymer deponeras på en varm yta (kammarväggen) vilket lämnar mer polymersubstans i plasmat som kan deponeras på en kallare yta (substratet) och således sjunker etshastigheten. Minskning av polymeriseringen uppnås också genom ökad substratspänning samt tillsats av syrgas. Förutom temperaturen, påverkades etsprocessen kraftigast av processtryck och substratspänning.

Appendices

A. Summary of Appended Papers

PAPER I

On the thermal stability of atomic layer deposited TiN as gate electrode in MOS devices

The work function of ALD TiN deposited on both SiO_2 and Al_2O_3 gate dielectrics was carefully investigated with respect to the thermal stability of the MOS devices.

The metal gate of as-deposited and low-temperature RTP annealed devices, exhibits a high work function of about 5.1 eV, which is appropriate for *p*MOS transistors. Further, the stacks are thermally stable in contact with the underlying dielectrics and material analysis by SIMS indicates no change in the TiN composition or diffusion of species into the dielectric materials upon annealing. However, both stacks suffer from reduced work function by about 0.3-0.5 eV after annealing above 800 °C, approaching mid-gap values, which may implicate that ALD TiN is less suitable as a metal gate for *p*MOSFETs in a conventional CMOS fabrication scheme.

PAPER II

Investigation of the thermal stability of reactively sputter deposited TiN MOS gate electrodes

Thorough examination of reactively sputter deposited TiN metal gate electrodes on SiO_2 gate dielectric of multiple thicknesses was carried out.

The extracted work function is close to 5 eV for RTP annealing temperatures below 700 °C, a value suitable for *p*MOS transistors. However, similar to the ALD TiN, a drop in work function occurs when annealed above 800 °C, which is not correlated to a change in physical structure or composition, as analyzed by XRD and XPS, respectively. Specifically, analysis by XPS revealed no shift in the Ti 2*p* binding energy neither for

depth profiling of a particular film nor for films annealed at different temperatures.

PAPER III

Variable work function in MOS capacitors utilizing nitrogen-controlled TiN_x gate electrodes

Metal gate $TiN_x/SiO_2/p$-Si MOS structures were fabricated and evaluated with respect to the work function of the TiN_x, deposited at various nitrogen gas flow and after several annealing steps.

A significant step in extracted work function by about 0.7 eV can be realized in the reactively sputter deposited TiN_x by depositing the metal gates at various nitrogen gas flows. Analysis by XRD displays no change in crystalline orientation for the different compositions, hence no correlation between the crystalline orientation and the work function exist. RTP annealing of films deposited at low nitrogen gas flow (Γ_{N2}) are reactive due to their metallic nature while films deposited at higher Γ_{N2} show no inter-reaction with the SiO_2 gate dielectric material. Annealing above 800 °C alters the work function towards a mid-gap value for the various compositions which is described in terms of pinning of the Fermi level due to extrinsic interface states.

PAPER IV

Low-resistivity ZrN_x metal gate in MOS devices

Reactively sputter deposited nitrogen-controlled ZrN_x thin films were used as metal gate electrode in MOS capacitors with SiO_2 gate dielectric. The resistivity and work function of the ZrN_x films were determined for several deposition conditions and for different annealing temperatures.

It was found that the resistivity of ZrN_x deposited at low flow of nitrogen gas exhibits a minimum of about 70 μΩcm, which increases for films deposited at higher flow. Work function below 4.1 eV is extracted from devices with ZrN_x deposited at nitrogen flow less than 18 sccm, which is considered adequate for *n*MOS transistors. The work function for such devices increases slightly to 4.3 eV after RTP annealing at 600 °C. Devices with ZrN_x deposited at high nitrogen gas flow (20 sccm) have close to *p*MOS matching work function after RTP at 600 °C.

PAPER V

Effects of low-temperature water vapor annealing of strained SiGe surface-channel pMOSFETs with high-κ dielectric

Compressively strained SiGe surface-channel *p*MOSFETs with ALD Al_2O_3 high-κ gate dielectric and ALD TiN metal gate exhibited expected performance enhancement in drive current, as compared to conventional Si channel FETs. However, degraded subthreshold slope was detected, which is an indication of a large density of interface states. A low-temperature water vapor annealing step was applied in order to reduce these interface states. For comparison, SiGe surface-channel *p*MOSFETs with thermally grown oxide were fabricated.

No improvements in the subthreshold slope could be detected with the annealing for the *p*FETs with Al_2O_3 dielectrics, indicating low or no passivation of the interface states. This is in contradiction to water vapor annealing of thermally grown oxide where an improvement in subthreshold is clearly visible. Further, significant reduction in negative oxide charge is observed by a continuous decrease of the threshold voltage after increased water vapor annealing time. It is speculated that the negative charge may originate from non-bridging oxygen bonds (Al-O-) in the Al_2O_3 film.

PAPER VI

Low-frequency noise and Coulomb scattering in $Si_{0.8}Ge_{0.2}$ surface channel pMOSFETs with ALD Al_2O_3 gate dielectrics

Carrier mobility and low-frequency noise were investigated in $Si_{0.8}Ge_{0.2}$ surface-channel *p*MOSFETs with ALD Al_2O_3 gate dielectrics and ALD TiN gate electrode. Low-temperature water vapor annealing was applied to the devices in order to modify the charge in the Al_2O_3 and improve the device performance. The scattering coefficient that determines the strength of Coulomb scattering was characterized using two methods; it was obtained both from mobility data extracted from I_d-V_g characteristics as well as from low-frequency noise measurements.

The combined number fluctuation and correlated mobility fluctuation noise model could successfully explain the observed 1/f noise. For the un-annealed devices, which contain a negative oxide charge, it was found that the mobility fluctuations were negatively correlated to the number fluctuations. On the contrary, positive correlation was observed for water vapor annealed devices which are thought to have a small positive oxide charge. The scattering coefficient from the two extraction methods yielded similar values, which however is much lower than usually reported for *p*MOSFETs from low-frequency noise characterizations.

PAPER VII

Electrical characterization of AlN MIS and MIM structures

Aluminum nitride has interesting electrical and piezoelectrical properties and has been explored both in electroacoustic as well as microelectronic components. Reactive sputter deposited AlN thin films were grown on Si under different process conditions to attain highly textured polycrystalline films as well as close to amorphous films. MIS and MIM structures were fabricated and electrically characterized by means of standard *C-V* and *I-V* measurements, as well as high frequency measurements.

It is found that the dielectric constant is about 10 regardless of the texture of the films. In addition, high-frequency analysis with a network analyzer shows that the capacitance is constant with frequency up to 10 GHz. Further, the extracted loss tangent is relatively constant with frequency with a value of about 0.03. The electron conduction mechanism during gate injection follows the Frenkel-Poole mechanism with trap energy of 0.6 eV below the AlN conduction band.

PAPER VIII

Simulation and dielectric characterization of reactive dc magnetron co-sputtered $(Ta_2O_5)_{1-x}(TiO_2)_x$ thin films

Both a theoretical and an experimental investigation of the dual target co-sputtering process of tantalum and titanium in argon and oxygen atmosphere was carried out. Ta_2O_5 is a high-κ material that is of interest for integrated capacitor devices. For bulk ceramics, incorporation of Ti in Ta_2O_5 results in an extensive increase in κ-value, and this study examines the electrical properties of Ta_2O_5 as well as of $(Ta_2O_5)_{1-x}(TiO_2)_x$ thin films in MOS capacitors. Standard *C-V* and *I-V* characteristics were carried out for several annealing temperatures.

The simulation of the dual target sputtering process revealed a hysteresis effect on the stoichiometry of the $(Ta_2O_5)_{1-x}(TiO_2)_x$ compound, where the Ta/Ti ratio not follows a simple relation when increasing the oxygen gas flow. This makes the deposition rather complex in the hysteresis region. The dielectric constant was extracted from standard *C-V* measurements and no improvement in the dielectric constant with addition of Ti was found for annealing temperatures less than 800 °C. However, annealing at 800 °C results in a 50 % increase of the κ-value probably due to a crystallization and higher polarizability of the material. Undesirably, the leakage current in the devices increases to an unacceptable high level after the high temperature anneal. Still, a low leakage current and a κ-value of about 22 is achieved,

with or without the addition of Ti, when the temperature is kept at or below 600 °C, which makes the material useful in integrated capacitors.

PAPER IX

Patterning of tantalum pentoxide, a high epsilon material, by inductively coupled plasma etching

In order to realize an integrated capacitor structure, the materials included in the structure must be deposited and patterned. The latter was studied by monitoring the etch rate of tantalum oxide, silicon oxide, and polysilicon. Results obtained from etching in an inductively coupled high-density plasma system and a reactive ion etch system were compared. The etching chemistry was based on CHF_3, which implies that the etching is controlled by polymerizing species. Process parameters such as power, bias voltage, gas flow, pressure, and temperature were varied.

It was found that the temperature on all surfaces in the chamber is central in determining the etch rate of the various materials since the deposition of polymers depends entirely on the surface temperature. The higher the temperature, the lower degree of the polymerization. This means that with higher temperature on the chamber walls, more polymerizing species will be in the plasma which can contribute to polymerization on the wafer that result in inhibited etching. Increased bias and addition of oxygen to the feed gas will decrease the polymer on the wafer by physical sputtering and chemical reaction to form carbon-oxide species, respectively. Besides the temperature, the parameters with the strongest influence on the process were pressure and substrate bias.

B. List of Acronyms

ALD	Atomic layer deposition
CMOS	Complementary metal-oxide-semiconductor
C-V	Capacitance-voltage
CVD	Chemical vapor deposition
DIBL	Drain induced barrier lowering
EOT	Equivalent oxide thickness
ESCA	Electron spectroscopy for chemical analysis
FET	Field-effect-transistor
FGA	Forming gas anneal
HP	High performance
IC	Integrated circuit
ICP	Inductively coupled plasma
ITRS	International technology roadmap for semiconductors
I-V	Current-voltage
LP	Low power
MBE	Molecular beam epitaxy
MIM	Metal-insulator-metal
MIS	Metal-insulator-semiconductor
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect-transistor
NVA	Network vector analyzer
PDA	Personal digital assistants
PVD	Physical vapor deposition
RF	Radio frequency
RIE	Reactive ion etching
RTP	Rapid thermal processing
SCE	Short channel effect
SEM	Scanning electron microscopy
SIMS	Secondary ion mass spectrometry
SOI	Silicon on insulator
TEM	Transmission electron microscopy
UV	Ultraviolet
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

C. Metal Work Functions

Table II. Work function of various metals and metal compounds.

Metal	Dielectric	Work function	Method	Reference
Ag	-	5.05	Photoresponse	[47]
Al	-	4.10	Photoresponse	[47]
Al	Al_2O_3	3.90	Internal photoemission	[22]
Al	SiO_2	4.14	MOS capacitor V_{fb}	[22]
Al	Si_3N_4	4.06	MOS capacitor V_{fb}	[22]
Al	ZrO_2	4.25	Internal photoemission	[22]
Au	-	5.00	Photoresponse	[47]
Au	Al_2O_3	5.10	Internal photoemission	[22]
Au	ZrO_2	5.05	Internal photoemission	[22]
Cu	-	4.70	Photoresponse	[47]
Hf	-	3.95	Photoelectric effect	[22]
Hf	SiO_2	4.00	MOS capacitor V_{fb}	[22]
HfN	SiO_2	4.65-4.70	MOS capacitor V_{fb}	[66]
HfN	HfO_2	4.75-4.80	MOS capacitor V_{fb}	[66]
Ir	HfO_2	4.55-4.65	MOS capacitor V_{fb}	[67]
IrO	HfO_2	4.75-5.10	MOS capacitor V_{fb}	[67]
Mg	-	3.15	Photoresponse	[47]
Mg	Al_2O_3	3.60	Internal photoemission	[22]
Mg	SiO_2	3.45	Internal photoemission	[22]
Mg	ZrO_2	4.15	Internal photoemission	[22]
Mo	-	4.95	Photoelectric effect	[22]
Mo	SiO_2	5.05	MOS capacitor V_{fb}	[22]
Mo	Si_3N_4	4.72	MOS capacitor V_{fb}	[68]
Mo	ZrO_2	4.94	MOS capacitor V_{fb}	[69]
MoN	SiO_2	4.70-5.33	MOS capacitor V_{fb}	[70]
Ni	-	4.60	Photoresponse	[47]
Ni	Al_2O_3	4.50	Internal photoemission	[22]
Ni	ZrO_2	4.75	Internal photoemission	[22]
Pt	-	5.65	Photoelectric effect	[22]
Pt	SiO_2	5.59	MOS capacitor V_{fb}	[22]
Pt	HfO_2	5.23	MOS capacitor V_{fb}	[22]
Pt	ZrO_2	5.05	MOS capacitor V_{fb}	[22]
Ru	SiO_2	5.10	MOS capacitor V_{fb}	[71]
RuTa	SiO_2	4.30	MOS capacitor V_{fb}	[71]
Ta	-	4.25	Thermionic emission	[22]
Ta	SiO_2	4.20	MOS capacitor V_{fb}	[71]

TaN	HfO_2	4.4-4.65	MOS capacitor V_{fb}	[67]
TaN	SiO_2	4.40-4.70	MOS capacitor V_{fb}	[72]
TaN	HfO_2	4.34-4.41	MOS capacitor V_{fb}	[72]
TaSiN	HfO_2	4.4-4.5	MOS capacitor V_{fb}	[67]
Ti	SiO_2	3.91-4.17	MOS capacitor V_{fb}	[70]
TiN	SiO_2	4.15-5.10	MOS capacitor V_{fb} and FN tunneling	Paper I-III
TiN	Al_2O_3	4.85-5.2	MOS capacitor V_{fb}	Paper I
TiAlN	SiO_2	4.36-5.1	MOS capacitor V_{fb}	[73]
W	-	4.63	Field emission	[22]
W	SiO_2	4.6-4.7	Fowler-Nordheim tunneling	[22]
ZrN	SiO_2	4.0-4.9	MOS capacitor V_{fb} and FN tunneling	Paper IV

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