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High Frequency Analysis of Silicon RF MOS Transistors

JOHAN ANKARCRONA

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Abstract

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Today, the silicon technology is well established for RF-applications (f~1-100 GHz), with emphasis on the lower frequencies (f < 5 GHz). The field of RF power devices is extensive concerning materials and devices. One of the important RF-devices is the silicon LDMOS transistor. A large extent of the research presented in the thesis concerns studies of this device, which have resulted in increased understanding of the device behavior and improved performance. The thesis starts with a brief survey of the RF-field, including the LDMOS transistor, followed by a description of the methods used in the investigations; simulations, modeling and measurements. Specific results presented in the appended papers are also briefly summarized.

A new concept for LDMOS transistors, which allows for both high frequency and high voltage operation, has been developed and characterized. World-record performance in terms of output power density was obtained: over 1 W/mm at 50 V and 3.2 GHz. Further understanding and improvements of the device are achieved using simulations and modeling. For determination of model parameters a new general parameter extraction technique was developed. The method has been successfully used for a large variety of high-frequency devices, and has been frequently used in the modeling work in this thesis.

Important properties of RF-power devices are the device linearity and power efficiency. Extensive studies regarding the efficiency were conducted using numerical simulations and modeling of the off-state output resistance, which is correlated to the efficiency. The results show that significant improvements can be obtained for devices on both bulk- and SOI-substrates, using thin high-resistivity substrates and very low-resistivity SOI-substrates, respectively.

Finally a new approach to drastically reduce substrate crosstalk by using very low-resistivity SOI substrate is proposed. Experimentally, a reduction of 20-40 dB was demonstrated in the GHz range compared to high-resistivity SOI substrate.

Keywords: RF-power, LDMOS, Microwave transistor, SOI, Silicon, MOSFET

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List of papers

This thesis is based on the following appended papers, which are referred to in the text by their Roman numerals.

I. “Sub-Circuit Based SPICE Model for High Voltage LDMOS Transistors”
Johan Ankarcrona and Jörgen Olsson,
Physica Scripta, T101, 7-9, 2002

II. “1 W/mm RF Power Density at 3.2 GHz for a Dual-layer RE-SURF LDMOS Transistor”
Jörgen Olsson, Niklas Rorsman, Lars Vestling, Christian Fager, Johan Ankarcrona, Herbert Zirath and Klas-Håkan Eklund,
IEEE Electron Device Letters, vol. 23, no. 4, pp. 206-208, 2002

III. “A General Small-Signal Series Impedance Extraction Technique”
Lars Vestling and Johan Ankarcrona,
IEEE Microwave and Wireless Components Letters, vol. 12, no. 7, pp. 249-251, 2002

IV. “Analysis and Design of a Low-Voltage High-Frequency LDMOS Transistor”
Lars Vestling, Johan Ankarcrona and Jörgen Olsson,
IEEE Transactions on Electron Devices, vol. 49, no 6, pp. 976-980, 2002

V. “Simulation and modeling of the substrate contribution to the output resistance for RF-LDMOS power transistors”
Johan Ankarcrona, Klas-Håkan Eklund, Lars Vestling and Jörgen Olsson,
Solid-State Electronics, vol. 48, no. 5, pp. 789-797, 2004

VI. “Improved Output Resistance in RF-power MOSFETs using Low Resistivity SOI Substrate”
Johan Ankarcrona, Mattias Larsen, Lars Vestling, Klas-Håkan Eklund and Jörgen Olsson,
Manuscript

VII. “Low Resistivity SOI for Substrate Crosstalk Reduction”
Johan Ankarcrona, Lars Vestling, Klas-Håkan Eklund and Jör-gen Olsson,
IEEE Transactions on Electron Devices, vol. 52, no. 8, pp. 1920-1922, 2005

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Preface

This thesis is written in the field of electronics, with emphasis on device simulation, modeling and measurement. The work has been focused on silicon high voltage LDMOS transistors. Especially the high frequency properties have been of interest. The final goal has been to improve the device performance but also to increase the understanding of the device behavior to be able to provide better models.

In the first part of the thesis I there is a general description of the RF-field, which contains a variety of different devices and materials. This is in contrast to other electronics where silicon is totally dominating. The reason for this is the variety in the demands for different RF-applications. The choice of technology depends on three main issues: performance, compatibility with other electronics and cost. A general picture of pros and cons of the technologies are given. The second part describes the methods that have been used in this work: modeling, measurement and simulation. Finally, there is a summary of the appended papers.

The research presented in the thesis has mainly been conducted within the "High Frequency Silicon Program" financed by the Swedish Foundation for Strategic Research (SSF). Part of the research reported here was also performed in the context of the network TARGET – "Top Amplifier Research Groups in a European Team" and supported by the Information Society Technologies Programme of the EU under contract IST-1-507893-NOE.

Introduction- background

Semiconductor materials

During the 19th century, studies of electrical properties of different materials were started. In that work a category of materials called “poor conductors” were identified. At that time the fundamental difference between the different materials was not known, but despite that the semiconductors were identified as a group of their own. In the latter part of the century a classification found on material properties was established. It was also noticed that some properties differ between samples of the same material while others always remain the same; the effect of impurities was realized. The uncertainty that the impurities provided resulted in large variation of the results. Today the impurities have become the base in the modern semiconductor industry since the impurity level can be very accurately controlled. For example, adding dope atoms such as arsenic, phosphorus or boron will drastically change the electrical behavior of silicon.

In 1931 a complete theory of material classification was published based on quantum theory. Even then the author was not sure that silicon (Si) was a semiconductor. The first field of application for the semiconductors was as rectifiers, where in the beginning selenium and copper oxide dominated. Even though the radio wave had been demonstrated in 1888 by Hertz, the use of semiconductor devices as rectifiers in radio receivers was not utilized until 1904. This lead to an extensive investigation of semiconductor materials and two different materials were preferred; lead sulphide (galena) and Si. Later, they were replaced by thermionic tubes.

In connection with the invention of the radar and the Second World War the focus was concentrated on high frequency properties. Here once again the Si found use since no other known material could work as a rectifier at such high frequencies. The new application stimulated extensive fundamental research on Si. At that time the interest in germanium (Ge) started since it is the next element after Si in the group IV-column of the periodic system. Ge was found to have several benefits, which made it the dominating semiconducting material. The advantage mainly concerned the substrate manufacturing, such as lower melting point and it was easier to purify. In the work on Ge an important breakthrough in the development of semiconductor devices was achieved: the manufacturing of the first active semiconductor device. The bipolar junction transistor (BJT) was invented in 1947 by J. Bar-

deen, W. H. Brattain [1]. They shared the Nobel Prize in 1956 with W. Schockley.

Devices

The invention of the bipolar junction transistor (BJT) marks the beginning of the semiconductor era. Before the BJTs, semiconductor devices were only used as rectifiers, photodiodes and thermistors. BJTs are three terminal devices, the current between two of the terminals is controlled by the voltage on the third terminal. This combined with the transistor effect make them useable as amplifiers and switches. A BJT consists of two p-n junctions back-to-back. The transistor exists in two configurations, n-p-n and p-n-p, where n and p stands for negative and positive doped region. The BJT terminals (and also the different regions of the device) are emitter, base and collector, where the base is doped opposite to the emitter and collector regions. Figure 1 shows a schematically n-p-n BJT. The current is controlled by the terminal voltages and the transistor is in active mode when the emitter-base junction is forward biased and the base-collector junction is reversed biased. Bipolar transistors are fast and often used in ultra-high-speed discrete logic circuits such as emitter coupled logic (ECL), but cannot be used in large circuits due to high standby power consumption.

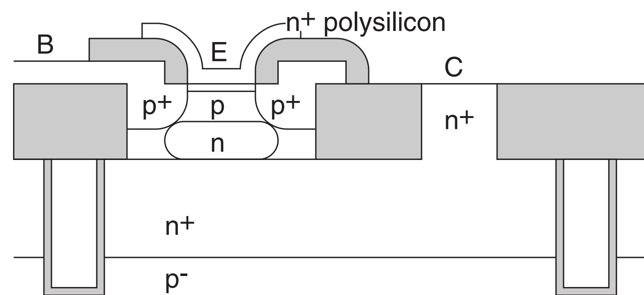

Figure 1. A modern n-p-n bipolar transistor (BJT) with trench isolation.

Besides the BJT the other major group of transistors is the field effect transistors (FET), which was fabricated for the first time in 1960. Most common of the FETs is the metal-oxide-semiconductor (MOS)FET. MOS transistors exist in two different configurations; n-channel (N)MOS and p-channel (P)MOS. In a MOSFET the current is controlled by the gate terminal voltage, which affects the channel surface potential. Figure 2 shows an NMOS and a PMOS transistor. The p-doped region under the gate is surrounded by the n-doped drain and source on either side. The gate is separated from the Si by the isolating silicon dioxide (SiO_2) layer. Changing the

potential on the gate will modulate the silicon under the SiO_2 layer. This behavior has given rise to the name field effect transistor (FET). For an NMOS transistor a positive voltage (~1 V) will invert the top layer and create an n-channel connecting the n-doped drain and source. If the channel is created and there is a voltage difference between the source and the drain, a current will flow through the channel. Since the gate electrode is isolated from the silicon by the SiO_2 layer there will not flow any current through the gate.

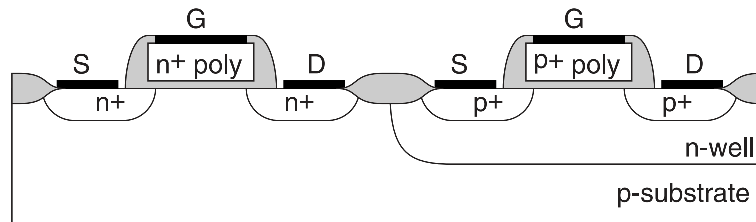

Figure 2. An NMOS and a PMOS in a CMOS configuration.

Generally MOSFETs are slower than BJTs but instead easier to manufacture and they can be packed with higher density. Single MOS circuits have also high standby power dissipation. In 1963 the complementary (C)MOS technology was invented, which utilized NMOS and PMOS transistors in the same circuit, figure 2. Standby power dissipation can be reduced to zero in CMOS technology by adding an NMOS and a PMOS in series between the power supply terminals, power dissipation will only occur at switching. Today CMOS is the totally dominating technology for large circuits.

Circuits

Devices with three terminals can be used to build logic. In these devices the voltage or current between two of the terminals is controlled by the third terminal. Each of the devices can be used as a switch and by cascade coupling them logic is built. Electrical circuits were built before the transistor was invented and at that time vacuum tubes were used. They played an important role in the early development of electronics. In the late 1940s the first computers were built using vacuum tubes. But vacuum tubes could not be used in large circuitsz due to high leakage current, short lifetime and that they required a lot of space.

The invention of the bipolar transistor provided the engineers with a device suitable for electronic circuits. At that time all devices were discrete components and circuits were built on boards. The BJTs were very suitable for building circuits, but the circuits soon become limited by the complex

couplings. The devices had the capability to build larger circuits but the technique was not prepared. Large resources were laid on developing new techniques to build circuits and in 1958 the next great invention was made, the integrated circuit (IC). The inventors were rewarded with the Nobel Prize in 2000. The invention made it possible to isolate the devices and made wiring possible by using oxide as an isolator. This means that a whole circuit could be integrated in a single piece of the semiconductor material. Ge had been the dominating material but was replaced by Si due to the attractive properties of the natural SiO_2. Integration had several positive effects; the devices could be made smaller, placed closer together and were less fragile. This made it possible to build larger circuits, while at the same time the smaller dimensions increased the maximum frequency where the transistor is able to work.

The possibility to obtain faster devices and at the same time increase the number of devices on a specific area simply through shrinking the device has been the driving force in the development of semiconductors. A prediction of the future development for the number of device on a single chip and the best economy per component was summarized by G. Moore in what has become Moore's law [2]. This prediction was made in 1965 and is still valid with some modification. In 1965 when it was formulated the most economical number of devices on a chip was ~50. The estimation was that in 1975 the number of transistors should be ~65000. The slope has been revised from a doubling every year to a doubling every 18 month but the trend is still kept, see figure 3. In 2003 the number of devices was predicted to be 410 million, which is what the Intel Itanium 2 processor has, manufactured that year [3]. Moore's law has become self-fulfilling and is expected to be valid for at least another 10 years.

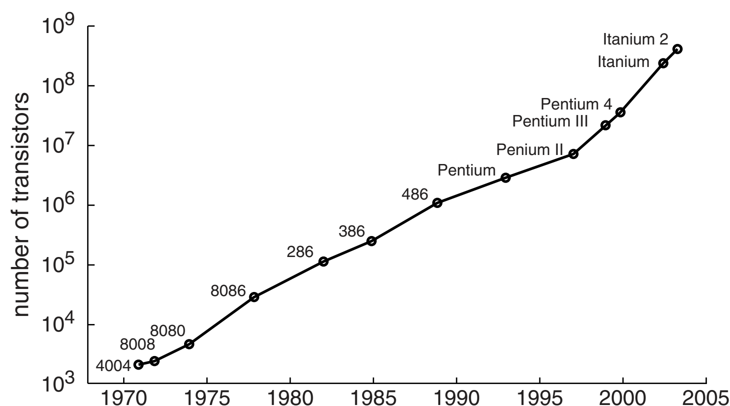

Figure 3. Moore's law, describing the progress of the most economical number of devices in an integrated circuit.

High frequency (micro wave) electronics

In all kinds of system where information of some kind is transferred the system needs to alter its signal. The simplest information system uses two discrete signal levels, such as computers and digital mobile phones where the signal length is fixed and the magnitude change between two different levels. In the other end of signal complexity is the analog system where both the magnitude and the length of the signal can vary continuously. Such system is for example radio, TV but also such a devices as the clock on the wall or.

Considering digital systems, increasing the amount of information transported is limited to the signal length since the amplitude is fixed. Shortening the signal length means increasing the frequency. This is the driving force to increase the clock frequency in the computer and one of the major benefits in changing mobile system from GSM (900 MHz) to 3G (2200 MHz).

Technologies and properties of RF-devices

General

In this work the term radio frequency (RF) refers to electromagnetic waves with frequencies around 1 GHz and above. The field contains various systems for wireless transmission, such as the first RF devices used in radar applications during the Second World War. Until the 1980s these were very expensive niche products mainly used by the military. The devices were manufactured in small quantities and the user where insensitive to price. In the 80s the first commercial product was realized, a satellite television system with an operating frequency of 12 GHz. During the last fifteen years the focus has changed and today commercial products dominate, which put new demands on the devices. This shift has been lead by the communication system especially mobile phones.

There are areas utilizing transistors with GHz operation capability but not included in the discussion of RF devices. Best known of these are microprocessors, which to a large extent has been the driving force behind the aggressive downscaling of silicon devices. The progress of these devices is totally dominated by Si CMOS and has indirect effect on the RF-field through leading the technology development.

From the invention of IC's, silicon has been the dominating material for semiconductor devices. Due to silicon's physical properties, RF-devices have been dominated by other materials, mostly compound semiconductors (III-V materials). Despite silicon's lower mobility and maximum electrical field, it is the primarily choice if possible due to low cost and superior integration level.

An overview of the material used for RF-devices and the different applications is shown in figure 4. For the lower frequencies, less than 10 GHz, group IV semiconductor (Si and SiGe) dominates while compound semiconductors dominate at the higher frequencies. For most applications and frequencies at least two different technologies are used. Since all of the semiconductors can operate at high frequencies there is a combination of demands that determine which to use. To evaluate the device some key figures of merit (FOM) are commonly used: noise figure, gain, stability, output power, power added efficiency (PAE) and mean time to failure (MTTF). Besides the performance, cost and integration level play an important role.

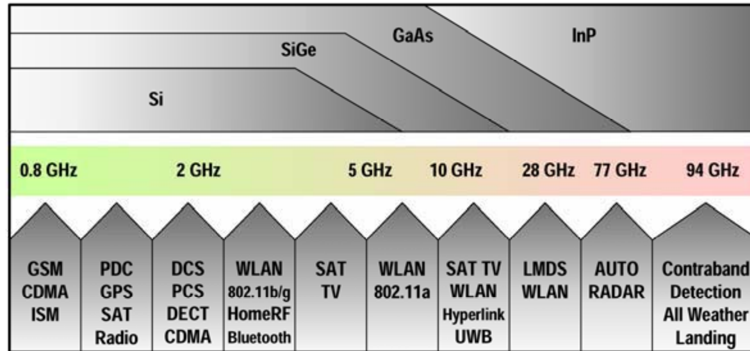

Figure 4. An application overview for the high frequency spectrum with conceivable semiconductor materials, from ITRS 2003.

FOM (figures of merit)

In this section the most frequently used FOMs will be described. These quantities are used by the circuit engineers to estimate and compare different devices and material properties. Depending on the field of application different FOMs are important. For instance the noise figure is vital for front-end amplifiers but insignificant for power amplifiers where instead the output power and linearity are very important.

Stability

To be able to work as an amplifier the transistor must be stable. The criteria for the device to be stable are that $k > 1$ and $|\Delta| < 1$, equation (1) and (2), if so the device is unconditionally stable [4].

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{1}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{2}$$

All devices are stable over a certain critical frequency f_k. Under f_k the device is conditionally stable, which means that it is dependent on the signal source and the load impedance if it will oscillate or not. Stability can be obtained by adding external admittances on the input and output in order to suppress the oscillation.

Power gain, maximum stable gain and unilateral power gain

The device's capability to amplify current and voltage is a key feature for RF-transistors. The gain is the ratio between the power delivered to the load and the power delivered to the transistor from the signal source. Maximum power gain (MAG) is obtained when the transistor is conjugate impedance matched to the source and load, respectively. Calculation of the gain is made by

$$MAG = \left|\frac{S_{21}}{S_{12}}\right| \cdot (k - \sqrt{k^2 - 1}) \; . \tag{3}$$

If the operation frequency is below f_k additional components have to be added on the input and output to prevail oscillation [5]. A stability factor (k_1) for the complete network can then be used, which is given by

$$k_1 = \frac{2 \cdot (\mathrm{Re}(y_{11}) + \mathrm{Re}(y_1)) \cdot (\mathrm{Re}(y_{22}) + \mathrm{Re}(y_2)) - \mathrm{Re}(y_{12} y_{21})}{|y_{12} y_{21}|} \; , \tag{4}$$

where y_1 and y_2 are the external admittances on the input and the output added to suppress the oscillation. If y_1 and y_2 are chosen to obtain $k_1 = 1$ then the condition for maximum stable gain (MSG) is obtained [5]. Under this condition MSG given by

$$MSG = \left|\frac{S_{21}}{S_{12}}\right| \tag{5}$$

Unilateral power gain [5, 6], U, is also a widely used quantity. The unilateral gain is defined for a device with zero output to input feedback. This is obtained by adding a network canceling the feedback, which is always present. This network will not oscillate since oscillation cannot occur without feedback. U is defined by

$$U = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2k\left|\frac{S_{21}}{S_{12}}\right| - 2\,\mathrm{Re}\left(\frac{S_{21}}{S_{12}}\right)} = \frac{|y_{21} - y_{12}|^2}{4 \cdot (\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12})\,\mathrm{Re}(y_{21}))} \tag{6}$$

The main advantage of using the unilateral power definition is that it is defined for all frequencies independent of the stability factor.

Characteristic frequencies f_T and f_{MAX}

f_{MAX} is the device maximum frequency of oscillation. The frequency states where the maximum power amplification is possible and is defined as the frequency where the unilateral power gain, U, equation (6) equals unity [7]. This is done by conjugate matching the signal source impedance to the transistor input impedance. The transistor output is treated in the same way, conjugate matched to the load. Additional network is added to cancel feedback. The name comes from the fact that this is the highest frequency, which the device would work as an ideal oscillator. The unilateral power gain decreases as a function of frequency with 20 dB/dec.

The transition frequency (or current gain cut-off frequency) f_T, is the maximum frequency where the device can amplify the current [7]. f_T is measured when the device is short circuited and is defined as the frequency where the short circuit current gain, h_{21}, is 1 (= 0 dB). h_{21} is defined as the ratio between the output and input current. h_{21} has the same behavior as U, i.e. it decreases with 20 dB/dec.

In most cases f_{MAX} is higher than f_T but the opposite exists. For BJT there is a trade off for high f_T or f_{MAX} concerning the design. Normally the transistors are used at considerably lower frequencies than the f_T and/or f_{MAX}, a factor of ten lower is a conservative margin. Since they are linked the relevance is also dependent, but for digital application f_T is said to be most important and for analog application f_{MAX} is most important.

Output power (P_{OUT}) and power added efficiency (PAE)

These FOMs are most important for amplifiers. Output power is the power delivered to the load. It is dependent on both the frequency and the amplifier class. Normally it is defined as power per mm gate width for FETs and power per μm^2 emitter area for BJTs. The power capability plays an important role considering the matching, since smaller devices are generally easier to match. When the accessible power is limited PAE is critical, it tells how much of the supplied DC power that is used as output power, equation 7 [8].

$$PAE = \frac{P_{OUT}(rf) - P_{IN}(rf)}{P_{IN}(dc)} \qquad (7)$$

PAE is normally defined at the 1 dB compression point. Another application where PAE can be of concern is when heat dissipation must be minimized.

Noise Figure (NF)

Noise is a key factor considering amplifiers and especially those amplifying very weak signals. When an input signal reaches the amplifier device it con-

tains of two parts, the signal and the noise. If the device is ideal the output signal will be a factor x higher than the input signal with the same ratio between the signal and noise. Since no ideal device exists an additional noise contribution will be added from the device itself decreasing the signal to noise ratio. The noise figure definition is

$$NF = 10\log(F) \tag{8}$$

and

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{9}$$

where SNR is the signal to noise ratio. F is the noise factor and is defined as the ratio of the input to output SNR ratio. SNR_{in} is always larger SNR_{out}, therefore the noise factor F > 1 and the noise figure NF > 0 dB [9].

A typical application where the noise is critical is the receiver's front-end amplifier. Several parameters affect the noise figure, the frequency, bias condition and input matching. Since the bias and matching condition are different from those for power gain there is a trade-off between the FOMs.

Mean time to failure (MTTF)

Reliability is an important parameter when considering which devices to use. The device is considered to fail when the current is reduced 15% (sometimes 20%) from the initial value under sustained bias condition. Tests are normally done by accelerated time test, i.e. high temperature tests. The lifetime can then be calculated from the test time and the temperature. The time is determined when half of the population has failed. There are a number of different mechanisms that reduces the device reliability. For FET devices normally the failure occurs in the channel region due to high electric field. In most cases the current gain for BJTs decline due to increased base current. There are different types of base current instability [10] caused mainly by stress-induced defects in the base.

Semiconductor materials for RF applications

In traditional VLSI technology Si is the only semiconductor material used, while RF-devices are manufactured in several different materials. The variety of materials is due to large variation in the RF-applications. That means the demands are very different regarding frequency, power, noise, operation voltage etc. The semiconductor materials can be separated into three groups, elemental (group IV) semiconductors (Si and SiGe), compound (III-V) semiconductors (GaAs, InP) and wide bandgap materials such as SiC and GaN. An overview of the semiconductor materials' field of application was shown in figure 4. Notice that for most frequencies and applications two or

more technologies co-exist. Figure 5 shows maximum power capability for different frequencies, for some of the technologies described in this section.

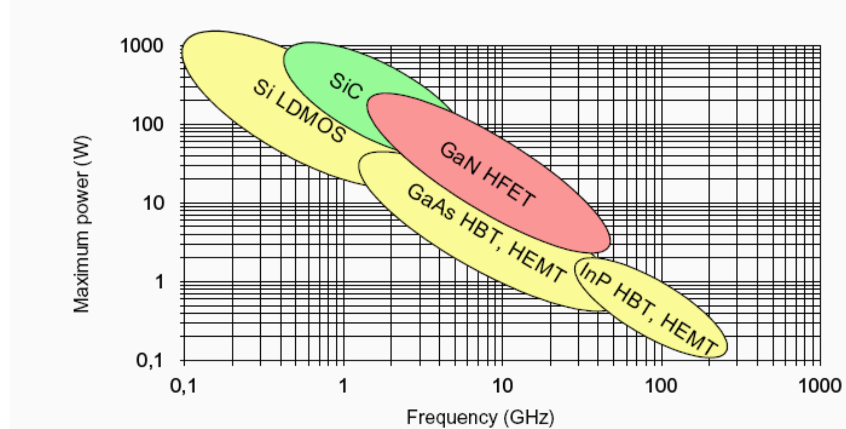

Figure 5. Maximum power vs. frequency for some different technologies.

Group IV-semiconductors

Si

Si has relatively low mobility and maximum electrical field compared to other materials used for power RF applications but superior manufacturing technology. The compatibility with other electronics, made in e.g. CMOS, makes Si RF-devices attractive for RF application. Another feature that makes Si very attractive is the low cost. Si devices have two main field of application as RF devices, as transceivers in cellular devices (low voltage applications) and as power amplifiers (high power applications) mainly in radio base stations [11]. Si devices are used in the lower part of the RF-domain, with emphasis on frequencies below 3 GHz, see figure 4 and 5. The main disadvantages of Si are the mobility and the critical electrical field. In the future, Si is believed to increase its market share in the frequency region above 3 GHz. Si and SiGe are the only possible material useable in the fast growing field system-on-chip (SoC), where all types of circuits are integrated together [12]. These systems are forced to use Si since it is the only substrate suitable for complex digital circuits. SoC means integration of almost all functions needed in a design on the same chip, such as memory, high performance/low-power logic, analog and RF circuits. Today this is the fastest growing RF area [13]. The driving force in this area is foremost consumer electronics such as DVD-player/recorder, digital-TV, digital cameras etc. The reasons for including more and more circuits on the same chip are several but the most important is the system speed. Today the wiring and connection of the circuits have become important for the performance. Even though SoC makes the design more complex and the semiconductor cost

increases, the overall benefit is larger. One of the major problems with integrating all kinds of circuits on the same chip is that the different circuits affect each other. This mainly concerns the sensitive RF circuits which can be affected by signal spread through the substrate, i.e. crosstalk. Several concepts to reduce and control the crosstalk have been investigated. The use of high-resistivity bulk silicon is commonly used for RF-circuit. Several techniques have been utilized for crosstalk suppression, for bulk Si substrate trench isolation [14] and guard rings [15]. A more effective method to suppress crosstalk utilizes Silicon-on-insulator (SOI) substrates, where in most cases the isolating layer consists of silicon oxide. The oxide layer effectively suppresses the losses for frequencies up to ~1 GHz but for high frequencies the effect is reduced [16]. Two different approaches using SOI for crosstalk reduction have been reported, combined with high resistivity (HR) substrate [15] and inserting of a ground plane under the oxide [17]. HR-SOI substrates suffer from additional charges under the oxide obtained during the manufacturing process, which heavily affects the crosstalk reduction. Another drawback is reduced performance for high voltages devices due to difficulties biasing the substrate [18]. The ground plane solution is restrained by a complicated substrate manufacturing process. In paper VII, a new simple and effective method to suppress crosstalk utilizing SOI with low resistive substrate is presented. The method has proven to be effective even for frequencies over 1 GHz.

Silicon Germanium (SiGe)

SiGe is manufactured on traditional Si-wafers allowing the use of traditional silicon process technology and fabs. This makes SiGe devices far more compatible with other circuits (Si-based) when compared to the rest of the heterojunction transistors and also more economically. SiGe is normally used in Bi-CMOS (integration of bipolar and MOS devices into a single process) allowing high performance heterojunction bipolar transistors (HBT) together with state of the art MOS transistors. Today SiGe is used in both FET and bipolar devices. The current research is focused on strain-engineering of CMOS. The lattice strain is utilized to increase the channel mobility in FETs. Channel mobility has decreased in FET due to down-scaling, so called short channel effects. HBTs are the most mature SiGe device [19-23]. In bipolar devices the differences in the valence and conduction band are used to improve the devices, band bending engineering. SiGe is also used for manufacturing high electron mobility transistors (HEMT). More details can be found in the device section.

Compound (III-V) semiconductors

GaAs

GaAs is one of the most important semiconductor material besides Si. The field of application contains both RF- and optical devices. In opposite to Si, GaAs has direct band gap, which makes it suitable for optical devices. For RF applications GaAs most important properties are high electron mobility and high saturated electron velocity [5]. That gives RF devices with low on-resistance, which saturate at low voltages. The combination of high switching speed and low power consumption (high PAE) makes GaAs devices very suitable in mobile application (battery-powered) [11, 24]. GaAs is used in heterojunction bipolar transistors (HBT) as base material often with AlGaAs as emitter [20]. Further description of the possibilities will be discussed in the device section.

InP

InP is the commercially available semiconductor with the best material properties for high frequency applications. HEMTs manufactured on InP substrates have shown to be the best performing three terminal devices concerning gain, noise and characteristic frequencies [5, 25]. InP is today used for the highest frequencies, figure 4, and show potential to increase its share of the market. There are some drawbacks to InP such as expensive and difficult substrate manufacturing and small wafer dimensions. The device manufacturing suffers from low yield due to fragile wafers and immature technology. Besides the HEMTs there have been successful tests with HBTs on InP [20], which is interesting since they normally have lower noise figure and tend to be more linear than the FETs.

Wide bandgap semiconductors

Semiconductor material with a bandgap over 2.5 eV is called wide bandgap semiconductors. These semiconductor materials have been considered very promising for over 30 years based on their physical properties. The most promising wideband gap materials today are silicon carbide (SiC) and Gallium nitride (GaN) [26-28]. Until recently, the material quality and the manufacturing technology have been insufficient to produce commercial devices in these materials. The largest problem for SiC has been micro-pipes in the substrate resulting in very low yield. Due to the large bandgap it is possible to manufacture devices with high power density working at high frequencies, while able to block high voltages. These devices can also work at high temperature, which reduces the demand of cooling. Due to their expense the use of SiC will be in high value applications where the superior performance only available with wide bandgap semiconductor is demanded. SiC is primarily used for MESFET while the focus for GaN is HBT and

HEMT. The field of application will in the beginning be in hazardous environments such as satellites and high performance applications (typically military systems) such as radar, system for electronic warfare and communication.

SiC has made significant progress but the lack of a suitable heterostructure will limit the operating frequency, gain and efficiency. A drawback for GaN has been the lack of bulk substrates, therfor GaN devices are made on SiC or sapphire substrate.

Devices

After the survey of different semiconductor materials used for RF applications the different devices will be described. Since there are several different materials there are also different devices since some material and device combinations are not suitable. In the beginning BJTs and MESFETs where used for RF applications. Today the development is focused on high performance heterojunction devices such as HBTs and different forms of HEMTs. Besides these, MESFETs are still widely used and for low frequencies under 3 GHz and high power Si LDMOS transistors have a large share of the market. This is also the part of the market with the highest turnover, since the commercial communication systems work in this region.

MESFET

In 1966, the first GaAs metal-semiconductor field-effect transistor (MESFET) was presented and it is still one of the most used RF devices [29, 30]. It was intentionally not invented for RF applications but showed already from the beginning very good high frequencies properties. At that time the only existing RF device was the Si BJT and until the early 80s these two were the only one in use.

A MESFET is a three terminal device, figure 6. The device consists of an active layer connected to the source and the drain. The control terminal, the gate, is connected to the active layer by a Schottky contact. The device is unipolar, only holes or electrons are responsible for the charge transport. Since the devices are unipolar they do not suffer from minority carrier storage effects, which make them fast. Additionally, MESFETs have high linearity and manufactured on GaAs the noise figure is low [31]. Today GaAs MESFET is considered to be a mature technology and the performance progress has leveled out even though the device is still widely used [5]. The MESFET has got a boom since it is the most suitable device for SiC, even though the breakthrough is still to come.

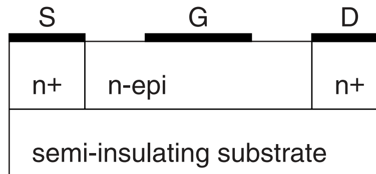

Figure 6. Cross-section of a MESFET

HBT

Heterojunction bipolar transistor (HBT) is a BJT where the device consists of two different materials. The device performance has been improved by scaling, but with new manufacturing technology developed in the late 70s the opportunities to improve the performance through the use of new materials lead to the development of new devices. These materials are chosen to obtain a larger bandgap at the base-emitter junction than for a BJT. The idea of using a heterostructure in a bipolar transistor is as old as the transistor itself and the advantages of this structure were first mentioned in 1948 and the theory was formulated in 1957 [32]. In the early 80s the molecular beam epitaxy (MBE) made it possible to grow extremely thin layers, thickness of a few nanometers, with sharp interfaces between the adjacent layers.

The basic device behavior is the same as for a BJT. Almost all RF-BJTs are of n-p-n configuration, i.e. the base is p-doped and the collector and emitter are n-doped, respectively. To turn on the transistor, the emitter-base junction is forward biased while the base-collector is reversed bias. Under these condition hole will flow from the base into the emitter causing a base current. At the same time electron will flow from the emitter into the base. Some of the electrons will recombine in the base while the other will flow to the collector moved by the electrical field, collector current. The gain is the relationship between the collector current and the base current.

In HBTs the emitter is manufactured of a different material with a wider bandgap for instance AlGaAs/GaAs. The bandgap difference between the emitter and base will suppress the base current and increase the emitter current, hence the gain is increased. This increased gain can be traded against higher base doping concentration. Reducing the base resistance will increase f_{MAX} and reduce the noise figure [5].

Another version of HBT is the SiGe device [19, 22]. The technique is the same as described for the AlGaAs/GaAs configuration, instead of increasing the emitter, the bandgap base bandgap is reduced through adding Ge creating a SiGe base. The bandgap can be additionally engineered by grading the Ge concentration added to the base. In that case the highest Ge concentration is at the base- collector junction and the lowest at the base-emitter junction. That will cause an additional electrical field in the base. The electrical field

will increase the charge transport in the base, resulting in increased device speed.

In general terms the HBTs advantages are low noise figure, high linearity, high speed and high power density. Today, the three most interesting HBTs are: AlGaAs/GaAs, Si/SiGe and InGaAs/InP. The GaAs based HBT is the most mature technology while SiGe has the advantage of being possible to integrate in CMOS technology. InP based HBTs has shown the best performance of them all [20].

HEMT

High electron mobility transistor (HEMT) is like the HBT founded on the heterostructure and utilizes the bandgap differences (ΔE_G) to obtain high performance devices. Three main versions of the device exist: lattice matched, pseudomorphic (strained) and metamorphic heterostructures [5]. In HEMTs a large difference in the conduction band E_C is desired since it stimulates the transfer of electrons from the large bandgap material, for instance n-doped AlGaAs to the narrow bandgap material GaAs in an AlGaAs/GaAs HEMT. The electron transferred is captured in a thin layer close to the junction, which is favorable concerning energy. This two-dimensional electron gas (2DEG) layer is only a few nanometers thick. The name originates from the fact that the electron can only move freely in 2-dimensions parallel to the junction. Since the 2DEG layer is separated from the donor impurity, scattering is suppressed and the electron mobility is increased. The cross-section of an HEMT is shown in figure 7. In an AlGaAs/GaAs device, the substrate, buffer and channel consist of GaAs while the barrier layer is made of n-doped AlGaAs. The current flows from the source to drain through the buried channel layer. The current is controlled by the gate Schottky contact voltage [33].

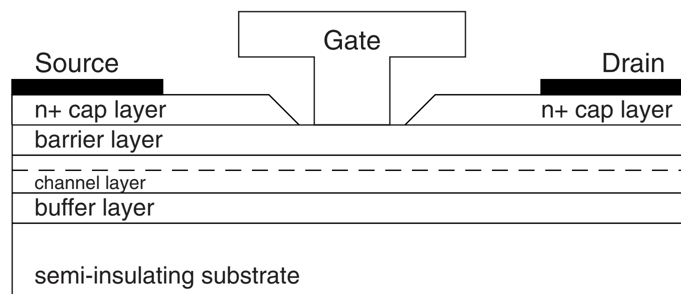

Figure 7. Cross-section of a HEMT.

In the beginning only lattice-matched structures, such as the AlGaAs/GaAs structure were of interest since only these were believed to meat the requirement of electron devices. Later it was shown that material with

different lattice constant could be used as long as the thickness of the grown layer was thinner than a critical thickness t_C. As long as the layer is thinner than t_C the layer will adopt the substrate lattice, a pseudomorphic layer has been created [34]. When the grown layer excess t_C it will relax causing a large number of dislocations in the interface. Several material combinations with large bandgap difference become possible. These devices are often InP based and have higher bandgap differences than the lattice matched. The drawback is that InP substrates are expensive, hard to work with and immature processes, leading to low yield and expensive devices.

The newest version of HEMTs is the metamorphic (mm) [35]. mmHEMTs are typically utilizing GaAs substrate where a buffer layer is overgrown, much thicker than t_C. This relaxed buffer layer will act as the substrate for the device. Since the buffer layer is much thicker than t_C the dislocations in the buffer/substrate interface will not affect the electrical properties. The main advantages with mmHEMTs are that inexpensive GaAs substrates can be used for manufacturing devices with high ΔE_C performance like InP based device without using InP substrate and at the same time be able to use the more mature GaAs processes.

HEMTs are today the most high performance devices commercially available, figure 5. Their main advantages are high f_T, f_{MAX} and very low noise figure especially for high frequencies [25].

LDMOS

The Lateral double diffused MOSFET (LDMOS) is a high voltage device based on Si MOS technology. It was invented in 1969 [36] and was first suggested in microwave applications in 1972 [37]. Today the majority of the radio base station amplifiers are made of LDMOS transistors [38]. The name can be derived from the manufacturing process where the channel is made through a double diffusion using the same mask. The channel length is determined by the difference in lateral diffusion similarly to the BJT (in depth), and in contrast to MOS devices where the channel length is determined by the gate length. The channel manufacture is mainly dependent on the process control compared to MOS transistors where lithography is the crucial process step. To be able to work at high voltages the drain needs to be separated from the gate region. This is accomplished by extending the drain with a low-doped drift region, see figure 8. The purpose of the drift region is to distribute the electrical field to prevent breakdown at the drain side of the gate. To be able to distribute the electrical field the drift region must deplete before impacted ionization take place at the drain side of the channel. The drift region doping needs to be relatively low to be able to deplete. LDMOS transistors are relatively complex devices with contradictory demands. Low doping leads to high on-resistance (R_{ON}), resulting in reduction of the saturation current (I_{DSAT}) and lowering the output power capability. While the drift

region is designed to handle high voltage, the channel region is the critical region to obtain high RF performance. Much of the device development concerns the drift region and how to optimize the current and at the same time handle high voltages, several techniques are utilized [39-41].

The Si LDMOS niche is high power devices in the lower frequency range, under ~5 GHz. The device features that LDMOS can offer are high power, high efficiency, high reliability and low cost [11].

LDMOS concept in Uppsala

As mentioned in the previous section different approaches are used to push the drain current and breakdown voltage towards higher values at the same time, such as trench gate structures, second gate structures and reduced surface field (RESURF) [42]. The drift region doping limits both the breakdown voltage and the current. The current increases with increased drift region doping while the breakdown has the opposite behavior. Using the RESURF principle the, on-resistance can be improved while maintaining the breakdown voltage. The RESURF concept means that a correct charge balance has to be obtained in order to reach the optimum trade-off between current drive (R_{ON}) and breakdown voltage. Additional improvements can be obtained by introducing a p-doping (p-top) in the drift region, figure 8 [43, 44]. The p-top is grounded outside the active transistor through the p-base and provides an additional p-n junction, which contributes to the depletion of the drift region. With this enhanced depletion of the drift region the doping can be increased with about a factor of 2, reducing R_{ON} and increasing I_{DSAT}. If the doping of the p-top layer is further increased, an n-top layer can be added for additional improvement of R_{ON} and I_{DSAT}. This approach has resulted in state-of-the-art RF performance with world record power densities, paper II.

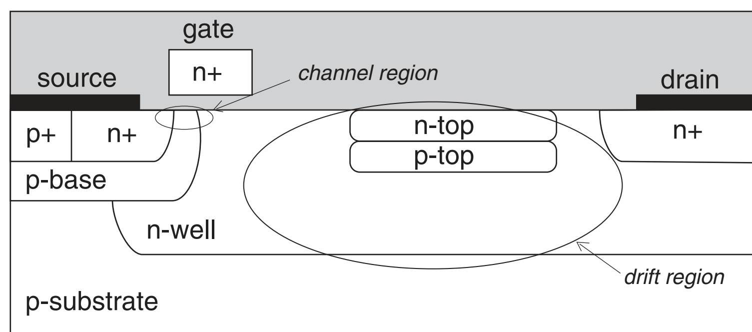

Figure 8. Schematic figure of the LDMOS transistror developed by the Uppsala group.

With those performance achieved the concept is meeting the present requirements and with continued development it is expected to be competitive to the upcoming wide bandgap materials GaN and SiC for operation under 10 GHz [45]. Other important RF properties, besides the output power capability, are the device linearity and the power efficiency of the device. Much of the results presented in the appended papers concern investigations of how to understand and improve the performance of this particular LDMOS transistor, see papers I, IV, V and VI.

Transistor Models and Parameter Extraction

Today short time to market and first time success are decisive in the semiconductor industry. To accomplish that, extensive use of simulations is the generally used method. Simulations have the advantages of being fast and inexpensive, but require considerable knowledge of the manufacturing process and device physics. Simulation of complete circuits such as SPICE requires models of the circuit elements, compact models. These models can be divided into three categories: physical, table-based and empirical models. Physical models are based on geometrical dimensions and material properties of the device while the others are based on device measurements. Other types of models are made for simulation of single devices, such as small- and large signal models.

AC-model, small-signal models

Small-signal models are made for linear AC simulation. Therefore, the applied AC-voltage must be low enough to consider the device to be linear. Since the beginning of the semiconductor era small-signal models have been extensively used for analog circuit design and device development. Small-signal models can be an attractive alternative to the large-signal model if non-linear AC phenomena do not need to be considered since the complexity is reduced. Nevertheless, small-signal models have also become complicated in many cases due to the constantly increasing frequency. A simple intrinsic small-signal model is shown in figure 9. In its simplest form, the model is quasi-static but can be refined to also include non-quasi-static effects [7]. The extraction of these parameters has become a research area of its own.

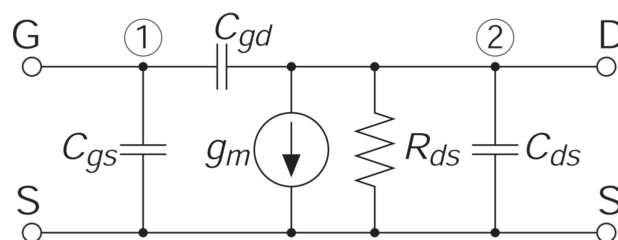

Figure 9. Small signal model for a MOSFET.

AC-model, large-signal models

No truly linear device exists. To be able to analyze quantities such as efficiency and linearity, large input signal variations are needed. Non-linear AC simulations can be divided into three categories: time domain analysis, frequency domain analysis and a combination of both. The large bias variation requires models that have voltage dependent parameters, figure 10, and handles the amplifier saturation when the input signal becomes too large. The empirical Chalmers model is an example of a large-signal model, which can be described as a small-signal model with bias dependent parameters and the current-voltage behavior included [46, 47]. This capability to handle non-linear AC behavior is what separates the true large signal models from a modern compact model. Non-linear devices create higher order harmonics. Applying a two-tone signal, f_1 and f_2, to the input, the output signal will consist of harmonics at frequencies: f_1, f_2, $2f_1$, $2f_2$, 0, $2f_1$-f_2, $2f_2$-f_1 and so on. This will affect the device in two ways, frequency independent term (f=0) will displace the bias voltage and the 3rd order harmonics will be close in frequency to the desired output signal. The difference in magnitude between the 3rd order harmonics and the desired signal must be large, in order to meet the requirements of e.g. mobile system standards. Therefore, large-signal simulation is of greatest importance for wireless communication systems. Large-signal models must be able to manage both the DC and AC parts. The model's complexity makes the parameter extraction complicated.

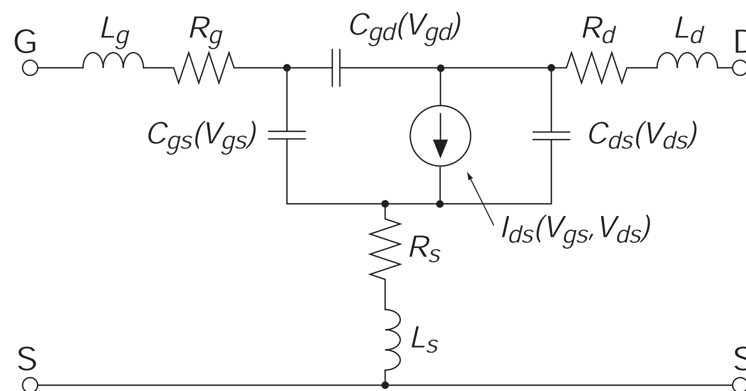

Figure 10. Example of a large signal model for a MOSFET.

Compact models

The non-linear current-voltage description is a key element in the compact model. Compact models have evolved from physical based DC-models to a

measurement based model capable of handling linear AC and transient simulations. Today accurate compact models for passive devices, MOSFETs and BJTs are available but for most other types of transistors, there are no general compact models. A simple set of equations describing the MOS transistors DC-characteristics can be found in [31] and the same equations are the base of the famous level 1 SPICE (Simulation Program with Integrated Circuit Emphasis) model from Berkeley University. Today SPICE is the dominating simulation program. There are a number of different models describing various devices. Widely used models for MOS transistors are the BSIM 3 and 4 (from Berkeley University) [48], MOS model 9 and 11 (from Philips) [49] and the EKV model [50, 51]. Still the foundation is the DC-description, which has evolved from being based on device physics (level 1) through extensive use of mathematical fitting parameters (BSIM 1 and 2) and then back towards being device physical based (BSIM 3 and 4, EKV and the Philips models) [52].

Extraction of small-signal parameters

Due to the complexity of large-signal models, small-signal models are often used. In many cases, the large-signal models are based on small-signal models [47]. This makes an accurate extraction of small-signal models even more important. Higher frequencies require more model parameters, since the capacitive contributions that for low frequency are insignificant, starts to influence the performance. Model parameters are extracted from measurements. These are in most cases two-port measurements. The two-port measurements return four admittance parameters (Y) containing a real and imaginary part, equation (10).

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \quad (10)$$

Simple models (eight parameters or less), as the example in figure 9, are usually extracted directly. This model is made for the intrinsic device, which requires that the extrinsic parts have been removed by de-embedding. The admittance matrix for the small-signal model is calculated using nodal analysis. The Y-parameter matrix for the small-signal model is shown, equation (11).

$$Y = \begin{bmatrix} j\omega(C_{gs} + C_{gd}) & -j\omega C_{gd} \\ g_m \cdot e^{-j\omega\tau} - j\omega C_{gd} & G_{ds} + j\omega(C_{ds} + C_{gd}) \end{bmatrix} \quad (11)$$

The matrix in (11) will provide the equation system needed to determine the model parameters, equations (12-17).

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \quad (12)$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{12}) + \mathrm{Im}(Y_{11})}{\omega} \quad (13)$$

$$C_{ds} = \frac{\mathrm{Im}(Y_{12}) + \mathrm{Im}(Y_{22})}{\omega} \quad (14)$$

$$G_{ds} = \mathrm{Re}(Y_{22}) \quad (15)$$

$$g_m = |Y_{21} - Y_{12}| \quad (16)$$

$$\tau = -\frac{1}{\omega}\arctan\left(\frac{\mathrm{Im}(Y_{21}) - \mathrm{Im}(Y_{12})}{\mathrm{Re}(Y_{21}) - \mathrm{Re}(Y_{12})}\right) \quad (17)$$

Since the model contains six parameters and the measurements provided eight measured parameters means that the equation system is over determined. Real parts of Y_{11} and Y_{12} are not necessary to extract the parameters and their values are assumed to be zero, if that is not true the model may need to be changed or the de-embedding has failed. The model parameter values should also be constant for all frequencies. Otherwise, the chosen model is inappropriate.

To extract parameters for models with more than eight parameters in each measured data point, figure 11, some sort of assumption must be made. Optimization is a widely used method to extract parameters for complicated models. The advantage is that a solution is usually found. The drawbacks with optimization are the need of input values, the risk of ending up in a local minimum and the problem with independent parameters obtaining nonphysical values. Due to the drawbacks, optimization is rarely the best solution.

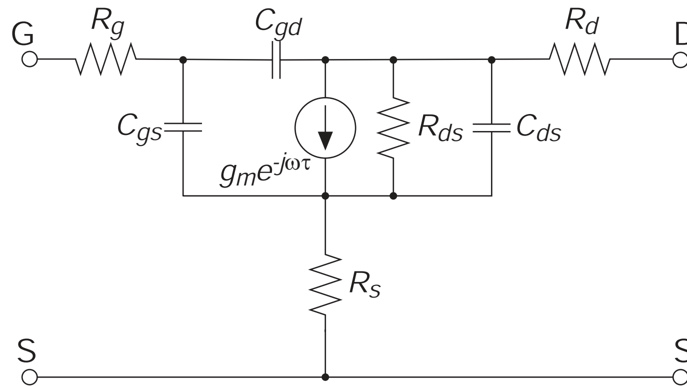

Figure 11. Small-signal circuit for a MOSFET including intrinsic parmeters and series resistances.

In most cases, the series impedances cannot be removed before extraction. Most models then need more than eight parameters to be able to describe the devices when both intrinsic and extrinsic parameters are included. Lovelace [53] suggested a method for parameter extraction of complicated MOSFET models. The method assumes that the intrinsic device is purely capacitive in off state, i.e. no applied voltage, and the series impedances to be purely resistive and bias independent. Under these conditions the series resistance is easily determined from the V_G=V_D=0 measurement, equations (18-20).

$$R_s = Z_{21} = Z_{12} \tag{18}$$

$$R_g = Z_{11} - R_s \tag{19}$$

$$R_d = Z_{22} - R_s \tag{20}$$

When the series resistances are determined at off state and subtracted, the intrinsic parameters can be extracted separately. The method originates from an extraction method for MESFET, called coldFET. The assumptions in these models are highly questionable due to the large difference between the MESFET and the MOSFET concerning the gate and the trueness of the voltage independent series impedance and the impedances to be solely resistive.

An extraction method including the parasitic inductances and resistances have been demonstrated [54]. The method is a further elaboration of [53] where the total series impedances are determined, the method is exemplified for the model in figure 12. The parameter extractions are made from a single measurement instead of using an additional measurement in off state to determine the series resistances. From mathematical expressions describing the model adjusted to the measurements, the model parameters are extracted under reasonable assumptions.

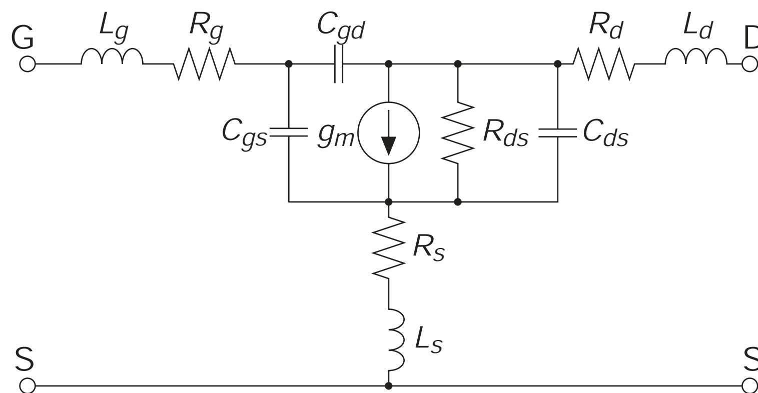

Figure 12. Small-signal circuit for a MOSFET including intrinsic parameters and series impedances.

Methods based on assumptions may work in some special cases but will always be questionable due to the validity of the assumption. A new approach to handle parameter extraction for complex models is described in paper III. The method handles fairly complex models without using any assumption or approximation. Extrinsic parameters are extracted in paper III for the small signal model in figure 12.

The proposed method in paper III will be described with a simple physical model for a capacitance shown in figure 13. All small-signal models can be analytically expressed in e.g. impedance parameters, as shown in (21) (s=jw). The impedance expression can always be written on the polynomial form shown in (21), where the coefficients are functions of the model parameters (22-24), so by knowing the coefficients the model parameters can be extracted. Then an error function is made in a similar manner as in fitting a straight line using the least square method. The result is an equation system that can be represented in matrix form as shown in (25), which is easily solved. The model parameters are then extracted by solving the non-linear equation system (22-24).

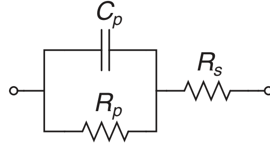

Figure 13. Equivalent circuit model for a capacitance.

$$Z = \frac{R_p + R_s + sC_pR_pR_s}{1 + sC_pR_p} = \frac{a_0 + a_1 s}{1 - b_1 s} \tag{21}$$

$$a_0 = R_r + R_s \tag{22}$$

$$a_1 = C_pR_pR_s \tag{23}$$

$$b_1 = C_pR_p \tag{24}$$

$$\begin{pmatrix} N & \sum_i s_i & \sum_i s_iZ_i \\ \sum_i s_i & \sum_i s_i^2 & \sum_i s_i^2Z_i \\ \sum_i s_iZ_i & \sum_i s_i^2Z_i & \sum_i s_i^2Z_i^2 \end{pmatrix} \cdot \begin{pmatrix} a_0 \\ a_1 \\ b_1 \end{pmatrix} = \begin{pmatrix} \sum_i Z_i \\ \sum_i s_iZ_i \\ \sum_i s_iZ_i^2 \end{pmatrix} \tag{25}$$

Complicated equivalent circuit models create a significant number of equations, for instance the scheme in figure 12 with 11 parameters generates 15 different coefficients, which implies that the system is over determined even though some of the parameters are equal. The problem is generally not to obtain under determined system. Instead, the determination of the equation system is the limiting factor for complicated equivalent circuit models.

High-Frequency Measurements

Measurements are used to evaluate circuits and devices. Devices and circuits can be measured either on-wafer or as discrete components, the equipment is the same and the techniques are similar. There are a number of different types of equipment used for high-frequency measurements depending on what the characterization is focused on, e.g. spectrum analyzers, network analyzers, frequency counters, power meters, impedance analyzers, LCR-meters (inductance, capacitance and resistance) and noise figures meters. This section will describe the on-wafer measurements of single devices utilizing the network analyzer and the impedance analyzer for small-signal analyses.

On-wafer measurements require high precision due to the size of the devices. Therefore, the measurements are carried out utilizing a probe station, figure 14. The probe station is designed to enable accurate control of the pressure applied to the probes and the alignment of the device under test (DUT). The adjustment of the DUT and the probe is visually guided through a microscope or a screen.

Figure 14. Probe station for high-frequency on-wafer measurements.

To be able to measure on single devices these must be specially designed since the size of the device is very small. Special connection to the device ports must be added to connect the probe tips to the DUT, figure 15. In figure 15 the fixture is made for two signal tips and four ground tips. The pad distance is determined by the probes' physical size, normal distance is 150 μm and pads size 50x50 μm. Probes made for these types of test fixtures with six pads and 150 μm pitches are called, GSG 150 where G stands for ground and S for signal. Air coplanar probes (ACP) are usually used up to 40 GHz. For higher frequencies waveguide technology must be used.

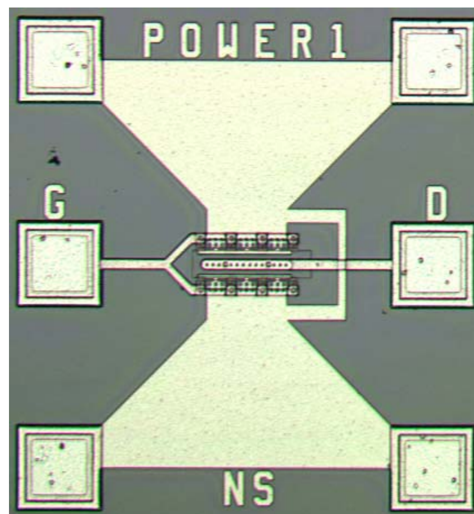

Figure 15. Schematic description of the DUT,test fixture and pads.

The network analyzer must be calibrated before the measurement. Depending of the nature of the measurement there are several different calibration methods. The calibration is made to remove the systematic errors and to remove the cable, probe and tip contribution to the result. Calibration of the system is necessary before each measurement session due to the drift errors, the system also needs to be re-calibrated after a couple of hours. After the calibration, only the DUT with pads will contribute to the result. The calibration is easiest carried out on an impedance standard substrate (ISS), which contains the structures necessary for the most common calibration methods, SOLT, LRM etc. As mentioned before, to be able to connect to a device a fixture (pads and extrinsic metal pattern) is needed between the tip and the device ports, which also will contribute to the measurement. The design of the fixture is very important to reduce its contribution to the result. Depending on the measured device the fixture's contribution to the result varies. For small devices the fixture contribution should be removed which can be done by on-wafer calibration structures containing the fixture design [55, 56].

In paper IV, measurements and modeling were used to characterize an LDMOS transistor. From the small-signal model, the high-frequency properties, power amplification and current amplification were evaluated. The influence of the different model parameters on the performance was examined using simulation of the model. The result was a design change suggested to increase f_{MAX}. The LDMOS transistor was manufactured with the new design and the evaluation showed that the redesign fulfils the expected performance improvement. The paper shows an effective use of measurements and modeling to improve device performance.

Numerical Simulation

Simulations are carried out to decrease development cost and time. In addition to the economic reason, the simulation provides information inaccessible from measurement. To be able to simulate the device performance, the device itself must be available for simulation.

Process simulation

The most accurate description of devices is obtained through physically based process simulations. These simulators predict the structure based on a specified process flowchart. This is obtained through solving the equation systems that describe the physics and chemistry in the processes [57]. Most simulations are made in 2-D, however 3-D is available but demands very large computer capacity. The equation system is solved in a pre-defined number of points, which compose a finite element method (FEM) mesh. The density of the mesh is depending on the demand for accuracy in the different parts of the device. To be able to process simulate a device, considerable knowledge of the underlying physics and manufacturing methods are necessary. The simulator needs to be initialised with the geometry, the sequence of simulation steps and the physical models. Modern process simulators are capable of handling all standard process steps for silicon.

Device simulation

Device simulators need a device structure as input. These are normally obtained from a process simulation. Physically based device simulators predict the electrical characteristics associated with the bias condition and the device structure [58]. The electrical characteristics are obtained through solving a set of differential equations in each grid point. The differential equations are derived from the Maxwell's equations, and simulate the carrier transport in the structure. The inputs to the device simulation are the device structure, the physical models and the bias conditions. From the device simulator DC, AC and time domain solutions are available [59].

In paper V and VI extensive simulation studies were made to examine the substrate's contribution to the high-frequency losses in off state for a power

LDMOS transistor. From the device simulations, the intrinsic couplings were understood and a small-signal model describing the device was developed. The simulations revealed that a feedback from the substrate to the source has a large impact on the high-frequency characteristics. The investigation was focused on substrate resistivity and thickness. Through simulation and modeling a 600 % improvement of the output resistance (=1/Real(Y_{22})) was noticed for a 100 µm thick high resistivity (1kΩcm) substrate compared to the initial structure. This investigation indicates that the efficiency of the LDMOS transistor can be improved with appropriate substrate design.

Summary

The focus in this thesis has been on silicon RF devices mainly for power applications. In the development of this type of devices traditional shrinking is not always a possible solution. Instead the improvements are rather based on the understanding of the device fundamentals than general process development. From a material properties perspective silicon is not optimal for RF-applications concerning mobility and maximum electrical field. This is compensated by the compatibility with other electronics, superior manufacturing technology and the low cost.

Since the development of e.g. LDMOS transistors are rather knowledge-based, the methods for improvements have been simulation and modeling. In the verifying process measurements have also been used.

The results in this thesis can be divided into three parts. Models and extraction (papers I and III), simulation based investigations (papers IV-VII) and device concept and performance (paper II). In paper I, a SPICE compatible LDMOS model, based on sub-circuit models and a model for self-heating, has successfully been developed. Paper III describes a parameter extraction method, which can improve the use of models. The method is very general and can be utilized if the device can be described with a nodal admittance matrix. Simulation and modeling were used in paper IV to improve a low voltage LDMOS transistor concerning its high frequency characteristics. In papers V and VI, the substrate influence on the device output resistance is studied using simulation and modeling, bulk silicon substrates were examined in V and SOI substrates in VI. Finally in paper VII, the crosstalk for bulk and silicon substrates were investigated, by modeling and simulation. The analysis indicated that a very low resistivity SOI substrate was favorably concerning crosstalk. A test structure was manufactured and the modeling and simulation results were verified by measurements. The crosstalk reduction was 20-40 dB compared to high resistivity SOI substrate for all frequencies. The results are remarkable since the general opinion has been that high resistivity SOI is the best solution for crosstalk reduction.

I would like to emphasis on two of the contributions in this thesis, papers III and VII. In my opinion these are the publications with the highest news value. And of course worth mentioning are also the world-record performance results in paper II. The crosstalk paper demonstrates that the idea, that the low resistivity SOI substrate can heavily reduce the crosstalk, is true. To prove that it can be used in circuit applications, there is a need for several

different investigations concerning the substrate influence on circuit performance. These are in my opinion excellent future research areas.

In this work process simulation, device simulation and modeling are used to understand and improve primarily high-voltage and high-frequency LDMOS transistors, suitable as power amplifiers. The work has been focused on some important parameters and has shown that device improvement indeed can be achieved with these types of investigations.

Summary of papers

I. Sub-Circuit Based SPICE MODEL for High Voltage LDMOS transistors

Simulation is a decisive part of circuit development. Each type of device used in the circuits needs to be described by a model. For the most common devices general models exist for programs like SPICE. Due to the large variation between LDMOS transistors from different manufactures, no general LDMOS SPICE models exist. In this paper a SPICE model for a double-diffused LDMOS transistor is presented. The SPICE model is of a sub-circuit type, which means it consists of a combination of standard SPICE models. The model handles variation of drift region length and also device gate width. Since power devices generate a lot of heat and the temperature affects the device performance, mobility and saturation velocity, this has to be included. Temperature dependence is normally not included in SPICE models, therefore an additional part is added which handles the temperature dependence of device width, length and voltage. Due to the device complexity the determination of the sub-circuit was dependent of device simulation. The channel behavior could be isolated and the BSIM3 model used for the channel could be adjusted to the measurements. A sub-circuit SPICE model was developed that predicts self-heating and fulfills the requirements of good accuracy and device scaling.

II. 1 W/mm RF Power Density at 3.2 GHz for a Dual-Layer RESURF LDMOS Transistor

The paper is a presentation of the unique LDMOS concept. The dual-layer RESURF is a very effective method to obtain high current while still keeping the breakdown at a high level. The RESURF is enhanced by introducing a p-doped region inside the drift region, which is grounded outside the active area. Additionally, an n-doped region is added on top of the p-top to increase the current drive capability. Combined with a short channel manufactured by diffusion, a high-power silicon RF transistor with world-record performance is obtained. The device has a 0.3 μm channel and a breakdown voltage of 110 V. The output power is more than 2 W/mm gate width at 1 GHz and

V_{DS}= 70 V, with a stable gain of 23 dB at V_{DS}= 50 V. At 3.2 GHz the power density is over 1 W/mm gate width.

III. A general small-signal series impedance extraction technique

Describing devices with small signal models is an appropriate method to understand a device. With the constantly increasing frequencies, more complicated models are necessary. Due to the limited amount of data from two-port impedance- and network analyzer measurements, direct extraction is only possible up to eight model parameters. Available extraction methods require some assumptions to be able to handle more parameters, which increases the uncertainty in the obtained values. This paper provides a method to obtain more than eight parameters without any assumption by using the entire frequency sweep for the extraction instead of making a separate extraction in each frequency point. The model is expressed in equations and the equations are adjusted to the measurements with the least square method. From the obtained equation coefficients, the model parameters can be determined. The method is particularly useful to obtain the series impedance parameters due to their simple appearance in the equations, independent of the chosen model. In the paper, the series impedances for a microwave LDMOS transistor are determined. The method can be extended to obtain all model parameters for the device. A drawback with the method is the complicated calculations for large models. On the other hand, it only needs to be done once.

IV. Analysis and design of a low-voltage high-frequency LDMOS transistor

f_{MAX} and f_T are very important figure of merits (FOM) for high frequency devices since they set the frequency limit for power- and current amplification for the device. An existing device was characterized DC and AC and an appropriate small-signal model was chosen. Even though the model was simple, the analysis of the extracted model parameters worked as an input to improve the device performance. This was done by careful analysis of each parameter's influence on the mentioned FOMs and the model parameters were connected to specific device parts. The examination showed that a redesign of the n-well would increase f_{MAX} without decreasing the f_T. The redesigned device was manufactured. Measurements showed that the f_{MAX} had increased with 30 percent with only a slight decrease of f_T. The changes corresponded to the foreseen performance.

V. Simulation and modeling of the substrate contribution to the output resistance for RF-LDMOS power transistors

For high frequency amplifiers the efficiency is vital. Since amplifiers in class AB, B and C are in off-state considerable part of the time, the off-state characteristics are of great importance for the efficiency. For the investigated silicon LDMOS most of the losses in off-state occur through the substrate. In this paper, the substrate losses are investigated by process- and device simulations. A small signal model was developed which describe the device very accurately in off-state over a large frequency range (10^6-10^{11} Hz) for all simulations of substrate doping levels and substrate thicknesses. The source-drain conductance has a phase shift with negative values for lower frequencies. This is due to two separate contributions to the source-drain conductance where one is identified to connect through the substrate, resulting in a phase shift. The consequence of the phase shift for the source-drain conductance is an increase of the output resistance (R_{OUT}) when it affects the result. The model was used to obtain an effective substrate design concerning the R_{OUT}, which imply a high phase shift frequency for the source-drain conductance. Utilizing a thin (100 µm) high resistivity (1 kΩcm) bulk substrate R_{OUT} was improved with approximately 600 % from 12 kΩ to 83 kΩ at f = 3 GHz for a 1 mm device.

VI. Improved Output Resistance in RF-power MOSFETs using Low Resistivity SOI Substrate

In paper V the effects of bulk Si substrate resistivity on the output resistance was studied, which was used as a gauge of the efficiency for high power MOS transistor. Next logical step is to introduce an isolating substrate. This was accomplished through introducing a silicon dioxide layer into the substrate. The output resistance was evaluated in the same manner as in paper V on a very simple structure, but nevertheless accurate, describing a power device in off-state. The SOI substrate introduces a capacitance between the device and the substrate contact, which means new opportunities to achieve high output resistance. Different substrate dopings were tested regarding output resistance. In opposite to the bulk substrate case where high resistivity substrate resulted in the highest output resistance, the very low resistivity SOI-substrate gave the highest output resistance among the SOI substrates. A comparison was made with the bulk substrate and an improvement in the order of 10 was noticed. Compared to medium and high resistivity SOI substrate, the improvement was about a factor 100. The high output resistance is mainly the result of the oxide capacitance. This is very positive since LRSOI

will also improve the current drive and breakdown voltage relation in a power MOSFET.

VII. Low Resistivity SOI for Substrate Crosstalk Reduction

Crosstalk has become a very important issue with the ever increasing use of System-on-Chip (SoC) solution where “noisy” digital circuits are mixed with sensitive analog circuits. Crosstalk occurs mainly through the substrate. Several methods have been suggested to reduce the signal through the substrate, guard rings for bulk substrate and for SOI ground plane or high resistivity substrates, where all of them have their drawbacks.

An effective and simple method to reduce crosstalk is presented in this paper. In the theory, modeling is used to compare different substrate resistivities concerning crosstalk. Different factors that affect the result are investigated, such as the load, pad distance and oxide thickness. Even though more current (signal) is injected into the substrate for the case with low resistivity SOI than for high resistivity SOI substrate, the current never reaches the sensitive node. Instead the signal is shunted to ground. Test structures for crosstalk measurements where manufactured for three different substrate resistivities: high resistivity (~1 kΩcm), medium resistivity (~10 Ωcm) and low resistivity (~10 mΩcm). Measurements verified the simulation results. The low resistivity SOI shows a crosstalk improvement of 20-40 dB compared to the high resistivity SOI substrate. Additionally, the low resistivity SOI substrate did not suffer from the problems associated with high resistivity SOI nor does it demand any additional manufacturing step as ground plane SOI.

Sammanfattning på svenska

Högfrekvensanalys av kisel RF MOS-transistorer

Den röda tråden i denna avhandling är LDMOS transistorn. LDMOS transistorn är en komponent som tål höga spänningar och kan dessutom arbeta vid höga frekvenser. Detta har gjort den mycket attraktiv för vissa RF-applikationer, t.ex. i basstationer för mobiltelefoni. Fokus har legat på komponentens högfrekvensegenskaper, att förstå dess beteende och kunna beskriva det med hjälp av modeller. Detta har utförts med hjälp av simuleringar, högfrekvensmätningar och modellering. Om man förstår och kan beskriva en komponent väl med hjälp av simuleringsverktyg kan man därifrån gå vidare och simulera hur eventuella förändringar av strukturen kommer att förändra dess beteende. Detta är en nödvändighet i all utveckling av halvledarkomponenter då tillverkningsprocessen är både dyr och tidskrävande. Följande verktyg för detta har använts i de delprojekt som utgör denna avhandling.

Numeriska simuleringar

Dessa består av två kategorier; simulering av tillverkningsprocessen samt simuleringar av elektriska egenskaper. Simulering av tillverkningsprocessen görs av två huvudskäl, att verifiera en tillverkningsprocess och för att erhålla en beskrivning av komponenten som används för den elektriska simuleringen. En elektrisk simulering ger information om strukturens uppförande vad det gäller storheter som strömmar, spänningar och kapacitanser men också storheter som man ej kan mäta på en tillverkad komponent t.ex. E-fältets fördelning, interna potentialer och strömriktningar. Simuleringar har använts i de flesta av de redovisade delprojekten för att undersöka hur en förändring av designen påverkar komponentens prestanda. I artikel I användes simuleringar för att öka förståelsen av komponentens interna kopplingar vilket ej kan erhållas på annat vis. Detta var grunden för förståelsen hur SPICE modellen skulle vara uppbyggd.

Högfrekvensmätningar

Simuleringar är ett nödvändigt verktyg för komponentutveckling, men det handlar ändå alltid om en uppskattning. Mätningar är de enda definitiva resultaten men är dock inte alltid möjliga att genomföra av flera anledningar. Komponenten måste finnas tillverkad. För att vara mätbar måste komponenten vara specialdesignad för detta, man kan inte mäta på godtycklig komponent i en krets. De höga frekvenserna och de små dimensionerna ställer stora krav på utrustning och kretsdesign för att undvika bidrag från omgivningarna. Högfrekvensmätningar har huvudsakligen använts i artikel II och IV.

Modeller

Två olika sorters modeller har berörts i denna avhandling. I artikel I var målet att utveckla en SPICE-modell för LDMOS transistorn, SPICE är ett kretssimuleringsprogram. Småsignalmodeller har varit viktiga verktyg för förståelse och utveckling av komponenter, vilka har använts i artikel III-VII. Modellerna är snabba och enkla verktyg för att exempelvis identifiera vilken region eller effekt som påverkar olika prestanda samt verifiera enklare antagande. Som indata till modeller används simulerings- eller mätresultat. Appliceringen på modellen görs med hjälp av parameterextraktion. Vid högre frekvenser krävs mer komplicerade modeller för att beskriva komponenten på ett riktigt sätt. Detta samt det faktum att mängden mätdata inte förändras gör parameterextraktionen mer komplicerad. Med standardmätmetoder kan endast åtta parametrar bestämmas utan antagande eller förenklingar (2-ports mätning). I artikel IV presenteras en metod för parameterextraktion av serieimpedanserna som kan användas separat eller tillsammans med existerande metoder, vilket möjliggör att mer komplicerade modeller kan nyttjas utan att några antagande behöver göras.

Uppnådda resultat presenterade i ingående artiklar

Artikel I

Beskriver framtagandet av en kretssimuleringsmodell för den högspända LDMOS transistorn. Modellen är en sk. underkretsmodell dvs. den är uppbyggd av standard SPICE modeller för vanligt förekommande komponenter, i detta fall JFETar och MOS-transistorer. Då denna transistor arbetar vid höga spänningar genereras värme vilket påverkar prestandan. Detta har inkluderats i modellen med ett tillägg då det normalt inte ingår i SPICE modeller. Resultatet var en modell som väl beskrev komponentens I-V karakteristik för givna geometrier.

Artikel II

Är en sammanställning av det LDMOS koncept som utnyttjas och där mätdata för komponenten presenteras bl.a. världsrekord vad gäller effekttäthet för högspända kiselkomponenter vid gigahertz frekvenser över 2 W per mm gatebredd vid 1 GHz.

Artikel III

Beskriver den extraktionsmetod som utvecklats för att primärt bestämma en komponents serieimpedanser. Metoden är inte beroende av några förenklingar eller antaganden. Denna metod möjliggör att fler parametrar kan bestämmas utifrån en mätning dvs. mer komplicerade modeller kan användas. Metoden är generell och kan användas på alla komponenter som kan beskrivas med nod admittanser.

Artikel IV

I denna artikel utgår arbetet från en existerande lågspänd (BV ~15V) LDMOS transistor. Från AC-mätningar extraheras modellparameter till en vald modell. Denna används som grund för en analys av de olika modellparametrarnas inverkan på den maximala effektförstärkningsfrekvensen f_{MAX}, som är ett viktigt mått på en komponents högfrekvensegenskaper. Därefter identifierades hur en designförändring för ökad f_{MAX} skulle kunna utföras. Detta verifierades genom mätningar på komponenter tillverkade med föreslagna förändringar.

Artikel V

Är en simuleringsstudie av substratets påverkan av en LDMOS transistors verkningsgrad. I studien används transistorns utresistans som mått på de förluster som uppstår under den del av cykeln då transistorn är avstängd, komponenten antas användas i en förstärkare. Med hjälp av simulering och modellering kunde en 600 procentig ökning av transistorns utresistans uppnås. Detta skedde genom att ändra substratets resistivitet från låg- till högresistivt samt att tunna ner substratet, en viss förändring av driftområdets dopning var också nödvändig.

Artikel VI

Kan beskrivas som en fortsättning på artikel V där SOI substrat har studerats. Oxidkapacitansen skapar nya möjligheter att erhålla hög utresistans utan att använda högresistiva substrat. Det visar sig att för SOI substrat skulle mycket lågresistiva substrat istället var mest gynnsamt, ungefär en faktor 10 bättre än ett högresistivt bulksubstrat och en faktor 100 bättre än ett medel- eller högresistivt SOI substrat.

Artikel VII

Detta är en studie av hur substratet påverkar överhörningen. Överhörning, dvs. att en signal sprider sig från en komponent till en annan är ett stort problem. Speciellt när hela system tillverkas på samma chip är detta ett problem då dessa system innehåller både ”brusiga” digitala kretsar och ”känsliga” analoga kretsar. Signalen går huvudsakligen genom det substrat kretsarna är tillverkade i. Den rådande bilden har varit att högresistiva SOI substrat skulle ge den största dämpningen av signalen genom substratet. I denna artikel har vi dock visat med modeller, simuleringar och slutligen mätningar att ytterligare reducering med 20-40 dB kan uppnås med lågresistiva SOI substrat vilket tidigare ej uppmärksammats. Detta samtidigt som problem uppkomna vid användandet av högresistiva substrat undviks.

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