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# Efficient Solid-State Power Amplifiers for RF Power Source Applications

RENBIN TONG



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**Abstract**

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Radio Frequency (RF) power sources are extensively applied in various fields. *Radioisotope production*, i.e., the production of short-lived radioactive isotopes, for positron emission tomography (PET) is one of the most important applications in the medical and healthcare domains. Full-time operation and substantial maintenance of such systems lead to high operating expenses. Hence, the development of more efficient and reliable RF power amplifiers, which are the main contributors to the energy consumption and maintenance costs of the RF power sources, is a high priority. Solid-state technology has emerged as a viable alternative to conventional vacuum tube based high-power RF/microwave systems, offering advanced control, reliability, and ease of use. Power amplifiers based on solid-state technology enable dynamic adjustment of power to optimize the transmitted energy. Furthermore, solid-state power amplifiers (SSPA) technology shows a longer lifetime leading to increased uptime and lower maintenance costs. Concisely, with the introduction of solid-state technology in high-power RF sources, RF energy can be generated more efficiently and more controllable in a smaller form factor, allowing for more compact systems with less downtime and less maintenance. This thesis is one step further toward demonstrating the feasibility of such systems.

The thesis first introduces the RF measurement setup. It implements automation for quick measurements and supports the evaluation of the high-power RF performance of the developed SSPA modules. Moreover, a novel thru-only de-embedding approach is developed to address the calibration difficulties under multi-port excitation conditions. The second part of the thesis deals with the development and analysis of efficient kilowatt SSPA modules. A *multimode* SSPA with quasi-static supply control for power regulation is implemented. It achieves more than 90% efficiency over a 5 dB output power back-off range. Another compact and efficient SSPA, implemented in push-pull architecture, adopts harmonic load-pull integrated with the same quasi-static supply modulation which also achieves 90% efficiency over a 5 dB output power back-off range. The implemented SSPAs improve the state-of-the-art in these frequency bands and power ranges.

This thesis broadens RF SSPA theoretical research to the kilowatt power range and provides a new understanding of high-power SSPAs from circuits, design methodologies, and analytical approaches. And it leads to new methods and tools to improve the energy efficiency of high-power RF sources. The knowledge gained and technology developed is not limited to RF power sources in radioisotope production applications, it can also be applied in the communication industry, such as radar systems, and other RF energy systems in industrial, scientific, and medical (ISM) fields, such as particle accelerators, welding, drying, heating, and many more.

*Keywords:* back-off efficiency, high efficiency, power source, RF energy, RF measurements, radioisotope production, solid-state power amplifiers

*Renbin Tong, Department of Electrical Engineering, Solid-State Electronics, Box 65, Uppsala University, SE-751 03 Uppsala, Sweden.*



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*To my beloved family,*
*to my dear friends*
*and to myself*

# List of Papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I **Renbin Tong**, Zhijiang Dai, Jörgen Olsson, Isabelle Huynen, Roger Ruber and Dragos Dancila, "Taper Transmission Line Based Measurement—An Thru-Only De-embedding Approach," *IEEE Transactions on Microwave Theory and Techniques*, 2022. DOI: 10.1109/TMTT.2022.3187981.

II **Renbin Tong**, Jörgen Olsson, and Dragos Dancila, "An improved analytical model for broadside coupled transmission line used on planar circuit," *AEU-International Journal of Electronics and Communications*, vol. 138, 153873, 2021. DOI: 10.1016/j.aeue.2021.153873.

III **Renbin Tong**, Olof Bengtsson, Jörgen Olsson, Andreas Bäcklund, and Dragos Dancila, "Kilowatt Power Amplifier With Improved Power Back-Off Efficiency for Cyclotron Application," *IEEE Transactions on Microwave Theory and Techniques*, vol. 70, no. 2, pp. 1401-1409, 2022. DOI: 10.1109/TMTT.2021.3134957.

IV **Renbin Tong**, and Dragos Dancila, "Compact and Highly Efficient Lumped Push-Pull Power Amplifier at Kilowatt level with Quasi-Static Drain Supply Modulation," *in 2020 IEEE/MTT-S International Microwave Symposium (IMS)*, pp. 29-32. IEEE, 2020. DOI: 10.1109/IMS30576.2020.9224091.

V **Renbin Tong**, Olof Bengtsson, Andreas Bäcklund, and Dragos Dancila, "Compact and Highly Efficient Kilowatt Lumped Push-Pull Power Amplifier for Cyclotron in Radioisotopes Production," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 1, pp. 723-731, 2021. DOI: 10.1109/TMTT.2020.3035353.

# Author's Contributions

I Conceived the presented idea, developed the theory, performed the formula derivation, designed and carried out the experiments, analyzed the data, and wrote and corresponded to revise the manuscript in accordance with the comments from the reviewers.

II Performed the formula derivation and EM field simulations, designed and carried out the experiments, verified the numerical results, and wrote and corresponded to revise the manuscript in accordance with the comments from the reviewers.

III Conceived the presented idea, developed the main part of the theory, evaluated the theory by simulations, fabricated the corresponding design, carried out the measurements, conducted the main processing and analysis of the data, and wrote the main part of the manuscript which was revised in cooperation with the co-authors in accordance with the comments from the reviewers.

IV Evaluated the architecture by simulations, fabricated the corresponding design, carried out the measurements, processed and analyzed the data, and wrote the manuscript and revised it in accordance with reference comments.

V Conceived the presented idea, evaluated the design by simulations, fabricated the corresponding design, carried out the measurements, processed and analyzed the data, and wrote the manuscript and conducted the major part of the revision in accordance with the comments from the reviewers.

# Publications not included in this thesis

I **Renbin Tong**, Andreas Bäcklund, and Dragos Dancila, "Ultra-compact and Simple Kilowatts level Multi-Way Resonant Cavity Power Combiner," Manuscript completed and to be submitted to *IEEE Microwave and Wireless Components Letters*.

II **Renbin Tong**, and Dragos Dancila, "Highly Efficient Kilowatt Power Amplifier Modules for Cyclotron Applications," *in IEEE MTT-S International Microwave Workshop Series On Advanced Materials and Processes for RF and THz Applications (IMWS-AMP 2021)*, November 15-17, Chongqing, China, 2021.

III **Renbin Tong**, Stefan Book, Long Hoang Duc, and Dragos Dancila, "A Planar Single-ended Kilowatt-level VHF Class E Power Amplifier," *in 49th European Microwave Conference (EuMC)*, September 29 - October 4, Pairs, France, 2019.

IV **Renbin Tong**, Stefan Book, and Dragos Dancila, "Kilowatt-level Power Amplifier Modules," *in ARIES Workshop on Energy Efficient RF*, June 18-20, Uppsala, Sweden, 2019.

# Contents

# Abbreviations and Symbols

## Abbreviations

| | |
|---|---|
| CW | Continuous Wave |
| DUT | Device Under Test |
| EM | Electromagnetic |
| GaAs | Gallium Arsenide |
| GaN | Gallium Nitride |
| HB | Harmonic Balance |
| HBT | Heterojunction Bipolar Transistor |
| HEMT | High Electron Mobility Transistor |
| HFSS | High Frequency Structure Simulator |
| IC | Integrated Circuit |
| IMN | Input Matching Network |
| LDMOS | Laterally Diffused Metal Oxide Semiconductor |
| LF | Low Frequency |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| OMN | Output Matching Network |
| OSL | Open Short Load calibration method |
| PA | Power Amplifier |
| PAE | Power Added Efficiency |
| PCB | Printed Circuit Board |
| PET | Positron Emission Tomography |
| PUF | Power Utilization Factor |
| RF | Radio Frequency |
| Si | Silicon |
| SiC | Silicon Carbide |
| SOLT | Short Open Load Through calibration method |
| SSPA | Solid-State Power Amplifier |

| | |
|---|---|
| Thru-Only | Through Only calibration method |
| TRL | Through Reflect Line calibration method |
| UHF | Ultra High Frequency |
| VHF | Very High Frequency |
| VNA | Vector Network Analyzer |
| VSWR | Voltage Standing Wave Ratio |

# Symbols

| | |
|---|---|
| $ABCD$ | Transmission Parameters or Matrix |
| $C_{(e,o)}$ | Capacitance under Even or Odd Mode |
| $C_{ds}$ | Drain-Source Capacitance of Semiconductor |
| $C_{gd}$ | Gate-Drain Capacitance of Semiconductor |
| $C_{OSS}$ | Output Capacitance of Semiconductor |
| $C_{pkg}$ | Parasitic Capacitance of Package |
| $f$ | Frequency |
| $f_0$ | Operating Frequency or Resonant Frequency |
| $G_p$ | Power Gain |
| $G_t$ | Transducer Gain |
| $I$ | Current |
| $I_{d,n}$ | $n$ th harmonic component of $i_D(t)$ |
| $I_{DQ}$ | Drain Quiescent Current |
| $i_D(t)$ | Drain current waveform at time domain |
| $I_{max}$ | Maximum drain current of $i_D(t)$ |
| $IL$ | Insertion Loss |
| $K/W$ | Kelvin per Watt |
| $L_j$ | Inductance of Bond-Wire Jumper |
| $P_{3dB}$ | Output RF Power at 3 dB Gain Compression |
| $P_{in}$ | Input RF Power |
| $P_{out}$ | Output RF Power |
| $P_{sat}$ | Saturated Output Power |
| $R_{opt}$ | Optimal Impedance |
| $RL$ | Return Loss |

| | |
|---|---|
| $S$ | Scattering Parameters or Matrix |
| $S_{nn}^{Diff}$ | Differential reflection response at port $n$ |
| $t$ | Time |
| $V$ | Voltage |
| $V_{d,n}$ | $n$ th harmonic component of $v_D(t)$ |
| $V_{DD}$ | Drain Bias (Supply) Voltage |
| $v_D(t)$ | Drain voltage waveform at time domain |
| $V_{knee}$ | Knee Voltage |
| $Y$ | Admittance Parameters or Matrix |
| $Z$ | Impedance Parameters or Matrix |
| $Z_{0(e,o)}$ | Characteristic Impedance under Even or Odd Mode |
| $Z_0$ | Characteristic Impedance |
| $Z_{nf_0}$ | $n$ th harmonic impedance |

| | |
|---|---|
| $\Delta\varphi$ | Phase Difference |
| $\eta_D$ | Drain Efficiency |
| $\Gamma$ | Reflection Coefficient |
| $\omega$ | Angular frequency, the rate of change of angular displacement, i.e., $d\theta/dt$. |
| $\phi$ | Phase |
| $\theta$ | Electrical Length or Angular Displacement |
| $c_v$ | Velocity of Light Propagation in Free Space |

# 1. Introduction

Radio Frequency (RF) power sources are extensively applied in various fields such as Industrial, Scientific and Medical (ISM) applications, RF/Microwave heating, communication systems, etc. ***Radioisotope production*** for positron emission tomography (PET) [1] is one of the most important applications in the medical and healthcare domains. PET is a functional imaging system that uses short-lived radioactive isotopes to visualize and measure variations in metabolic processes and is widely used in hospitals for medical diagnosis of diseases. The acquisition process of PET and the scheme for radioisotope production are depicted in Figure 1.1.

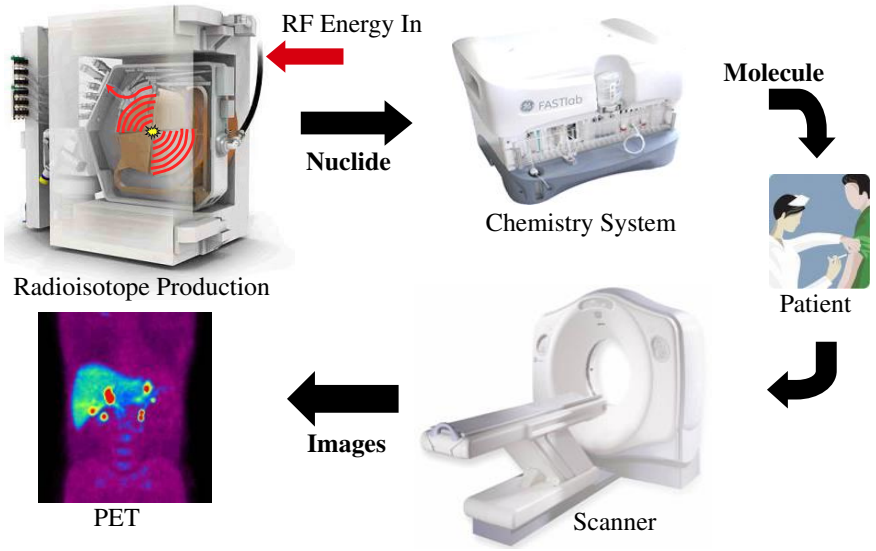



*Figure 1.1. Schema of radioisotope production for a PET acquisition process. Courtesy of GE.*

Radioisotope production operations require significant RF energy. The manufacture and maintenance of such systems result in high initial and ongoing operational costs [2]. Providing a low-cost, stable and effective solution is important for the promotion and widespread use of PET technology.

## 1.1 Outline of RF Power Sources

RF power sources, providing RF energy to radioisotope production, are designed to efficiently convert DC energy to RF energy and transmit this RF

energy as electromagnetic (EM) waves. The RF energy in a cyclotron is used to accelerate charged particles (protons) in a magnetic field. The RF sources are the most energy-consuming parts and substantially contribute to the considerable RF energy expense in 24 hours operation a day, 7 days a week (24-7). Therefore, it is imperative to develop high-efficiency RF power sources aimed at energy-saving. A general very high power RF source system is illustrated in Figure 1.2.

Vacuum tube technology is the dominant technology in power sources but is poorly adapted to output power control. And it requires costly regular maintenance due to the limited lifetime of vacuum tubes. Furthermore, vacuum tube systems are bulky and require additional high voltage supplies leading to very large systems [3].

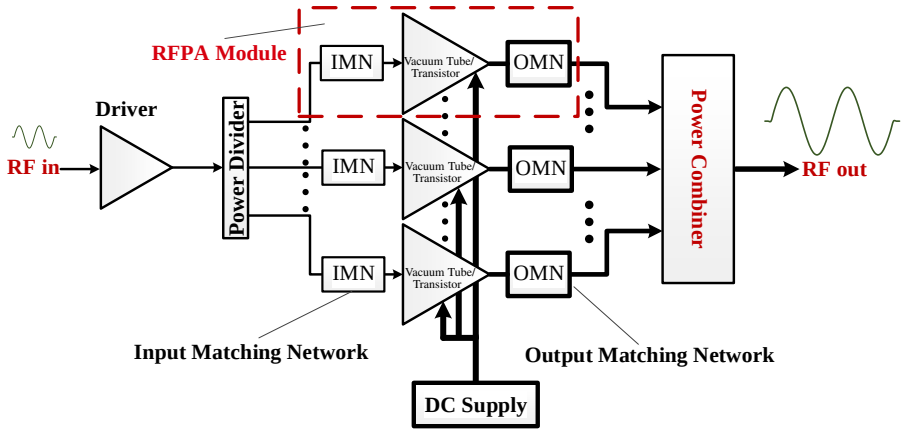



*Figure 1.2. RF power source system.*

Meanwhile, the solid-state transistor alternative as seen in Figure 1.2 is based on a multitude of power modules and can be made more compact and more adjustable. Each module is limited to kilowatts level in a single chip if adopting current solid-state technologies and the output power can be adjusted by supply voltage control. Power combining allows breaking the technology limitation of the single RFPAs. This can be accomplished in fully isolated combining systems that allow hot-swap of malfunctioning RFPA units during system operation which adds to the robustness and uptime of the system.

## 1.2 Solid-State RF Power Transistors

RF solid-state technology is an excellent alternative to traditional vacuum tube-based RF/microwave systems. This technology offers advanced control, reliability, and ease of use. The ability to dynamically adjust power and frequency helps to optimize transmitted energy. When designing high-performance high-power solid-state PAs, the appropriate RF power transistors

must be employed. RF power transistors can be categorized according to the semiconductors they are built on. Early military use transistors were made from gallium arsenide (GaAs) but nowadays commercial solutions are based on silicon (Si) and more recently gallium nitride (GaN) [4, 5]. Gallium nitride on silicon-carbide (GaN-on-SiC) is utilized recently because GaN has the ability to maintain a high field for a small geometry and SiC has better thermal performance.

### 1.2.1 RF Power Transistor Technologies

An RF power transistor is a special type of transistor designed to handle significant levels of power. Mainly the dimensions of the transistor are scaled up to be able to handle the high fields for operation at fairly high voltages. Targeting RF applications, the parasitic drain-to-source capacitance must be low to allow high-frequency operation. Hence, an RF power transistor favors a semiconductor with a high breakdown field, high mobility, and high velocity saturation. This is known as Johnson's limit or Johnson's figure of merit [6]. The silicon power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is the world's most widely used power semiconductor device because of its low gate drive power, fast switching speed, simply extended paralleling capability, wide bandwidth, ruggedness, easy drive, simple biasing, ease of use, and most importantly affordable [7, 8]. In particular, it is the most widely used low-voltage switch (less than 200V), and can be found in a variety of applications such as power supplies, DC-to-DC converters, low-voltage controls, and many other applications.

Silicon-based laterally diffused metal oxide semiconductor (Si-LDMOS) has found widespread use in CW amplifiers and communication applications under modulated signals. It's also a good choice for pulsed applications up to L-band (1 GHz to 2 GHz). LDMOS is well suited for long pulse applications due to its very low thermal resistance, which also contributes to its excellent VSWR characteristics. GaN HEMTs (High-Electron-Mobility Transistors) are the most recent RF and microwave power transistor technology. GaN is a wide-bandgap material with high breakdown voltage. It can thus sustain a high field for very small dimensions making it a very fast technology for RF power devices. In addition, the current transport is conducted in a 2-dimensional electron gas (2DEG) with very high-velocity saturation which all leads to a large power density. Because of their high gain and high power levels, they are rapidly gaining popularity for many applications in S-band (2 GHz to 4 GHz) and above. GaN power transistors are mostly fabricated on SiC substrate, which offers excellent heat dissipation for improved long-term reliability [7]. GaN HEMTs are ideal for high power pulsed applications and their power density requirements (compared to CW applications) as the ability to design on a SiC substrate allows for optimal cooling. Because of the

small geometries, the output capacitance per watt becomes much lower even for high-power transistors. This allows more flexibility for harmonic tuning on the matching network to target higher efficiency operations. Properly exploited, this efficiency can have a big impact at the system level in commercial RF energy applications. Additionally, the much lower capacitance per watt also enables these devices to operate at much higher frequencies than LDMOS [9, 10, 11]. Furthermore, the high breakdown voltage enables VSWR rugged designs that can operate under severe mismatch conditions. However, GaN is still not a mature technology and suffers from inherent dispersion effects from the gate and drain lag generated by buffer and surface traps that are charged and discharged in dynamic operation. At present GaN is entering the kilowatt operating range, but is not cost-competitive in the MHz and sub-GHz range where LDMOS dominates, as LDMOS offers the same performance but much lower cost.

Moreover, several materials and technologies are being evaluated for future RF power applications. Some are lateral technologies like the standard GaN but with an alternative heterostructure, such as AlN. Other alternatives include GaO and vertical GaN. These technologies are not expected to be mature in the coming years but may be available in a 5-10 year perspective. A summary of some technologies and their figure of merits for RF power applications is given in Table 1.1.

**Table 1.1.** *The figure of merit comparisons of semiconductor material properties.*

| Material | Silicon | GaAs | SiC | InP | GaN | AlN | $\beta - Ga_2O_3$ [12] |
|---|---|---|---|---|---|---|---|
| $v_{sat}$ * ($\times 10^5$ m/s) | 1 | 1.5 | 2 | 0.67 | 2.5 | 1.6 | 1.5 |
| $V_{Breakdown}$ ‡ (MV/cm) | 0.3 | 0.4 | 3.5 | 0.5 | 3.3 | 1.5 | >7 |

* $v_{sat}$ represents the saturation velocity.

‡ $V_{Breakdown}$ represents the breakdown electric field.

All the developed SSPA modules in this work are based on Si-LDMOS technology. At present, it is the only technology that can reach these high power levels in this frequency range. It's also the most inexpensive technology with the best price-performance ratio. While it is likely that high-power GaN will enter this space in the future and this will push the state-of-the-art even further by enabling alternative switch-mode RFPA solutions with better RF performance.

### 1.2.2 Importance of $C_{OSS}$ / $C_{ds}$

In a power MOSFET, the gate is insulated by thin silicon oxide. Therefore, a power MOSFET has capacitances between the gate-drain, gate-source, and

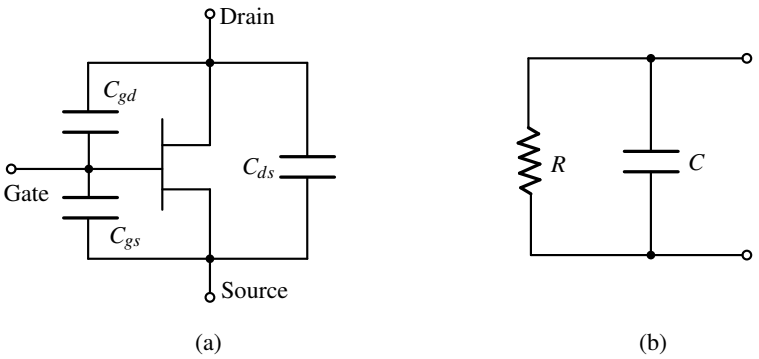



*Figure 1.3. (a) Equivalent capacitance circuit. (b) Linear RC model for transistor output network.*

drain-source terminals [13]. The capacitances are often named $C_{iss}$ (input capacitance, drain and source terminal shorted), $C_{oss}$ (output capacitance, gate and source shorted), and $C_{rss}$ (reverse transfer capacitance, source connected to ground). Manufacturers prefer to quote $C_{iss}$, $C_{oss}$ and $C_{rss}$ because these capacitors can be directly measured on the transistor. However, as $C_{gs}$ (gate-to-source capacitance), $C_{gd}$ (gate-to-drain capacitance) and $C_{ds}$ (drain-to-source capacitance) denoted in Figure 1.3 (a) are closer to the physical meaning, they are used more frequently in matching network analysis and synthesis [14]. The relationships between these capacitances are described below:

$$C_{iss} = C_{gs} + C_{gd} \tag{1.1a}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{1.1b}$$

$$C_{rss} = C_{gd} \tag{1.1c}$$

For power amplifier design, output matching network (OMN) design is more important than input matching network (IMN) design if it meets good input return loss, thus the parasitic capacitor $C_{ds}$ is obviously crucial as it enormously impacts the frequency response of RF transistor. Furthermore, $C_{oss}$ becomes important as it almost determines $C_{ds}$, since $C_{gd}$ or $C_{rss}$ is much lower than $C_{ds}$, usually around one-tenth of $C_{ds}$.

The $C_{oss}$ of a MOSFET depends on the applied drain-source voltage $V_{ds}$. For simplicity, the transistor output network can be simplified to a linear RC model [15], see Figure 1.3 (b), it has also been referred to as the small-signal model. $C_{oss}$ or $C_{ds}$ is not considered voltage-dependent in this linear model but instead, for the high power model the voltage dependence of the output capacitance $C_{oss}$ is modeled by the voltage dependence of $C_{gd}$ and $C_{ds}$. The dynamic and voltage dependence $C_{oss}$ is more accurate and crucial in high-power (large-signal) simulations. Therefore, the linear model of the transistor is mainly used for conceptual understanding and small-signal field analysis.

Furthermore, as seen in Figure 1.3 (b), the linear RC model consists of *RC* elements connected in parallel, the capacitance *C* is mainly determined by $C_{ds}$, the resistance *R* is the matched impedance or on-resistance $R_{on}$, from the Bode-Fano criteria [16, 17] given below:

$$\int_0^\infty \ln \frac{1}{|\Gamma(\omega)|} d\omega < \frac{\pi}{RC} \tag{1.2}$$

where $\Gamma(\omega)$ is the reflection coefficient seen looking into the arbitrary lossless matching network. Applying (1.2) to the matching reflection coefficient $\Gamma_m$ gives

$$\int_0^\infty \ln \frac{1}{|\Gamma(\omega)|} d\omega = \int_{\Delta\omega} \ln \frac{1}{\Gamma_m} d\omega = \Delta\omega \ln \frac{1}{\Gamma_m} \leq \frac{\pi}{RC} \tag{1.3}$$

As *R* and/or *C* ($C_{ds}$ or $C_{oss}$) increases, the quality of the match (bandwidth $\Delta\omega$ and/or $1/\Gamma_m$ ) must decrease. Thus, higher-Q circuits are intrinsically harder to match than are lower-Q circuits [18]. Too large $C_{oss}$ prevents transistors from operating in the high frequency range and also implies that they cannot operate at a wide bandwidth $\Delta\omega$ by (1.3).

It's especially for solid-state LDMOS transistors in the kilowatt range, the $C_{oss}$ can assume up to hundreds of pF due to the large periphery, while GaN is around tens of pF thanks to its good power density that allows for reduced size. But the low-cost LDMOS technology is still the better choice for VHF (Very High Frequency, 30 MHz to 300 MHz) and low UHF (Ultra High Frequency, 300 MHz to 3 GHz) band applications since it still enable harmonic tuning for the high efficiency pursuit.

## 1.3 Efficient RF Power Amplifiers

Energy efficiency simply means using less energy to accomplish the same task, i.e., avoiding wasting energy. Energy efficiency brings a multitude of benefits: reducing the demand for power supply and lowering operating and cooling costs. Decreasing energy consumption reduces energy costs and can result in financial cost savings if the energy savings outweigh any additional costs of implementing energy-efficient technology.

As shown in Figure 1.2, the core of an efficient RF power source consists of high-efficiency PA modules. The efficiency definition usually has two forms: drain efficiency ($\eta$) and power added efficiency (*PAE*).

Drain efficiency, also called output efficiency or simply efficiency, is defined as the ratio between the output power[1] ($P_{out}$) at the ***fundamental frequency*** and the supplied DC power ($P_{dc}$) [19], is given by:

[1] Unless stated otherwise, $P_{out}$ represents the RF output power at fundamental frequency in this thesis.

$$\eta_D = \frac{P_{out}}{P_{dc}} = \frac{V_{ds} \cdot I_{ds}}{2 \cdot V_{dc} \cdot I_{dc}} \tag{1.4}$$

Regularly, the DC component[2] $V_{dc}$ for drain-source voltage $v_{DS}(t)$ is exactly the DC bias voltage $V_{DD}$. While $I_{dc}$ is the DC component for drain-source current $i_{DS}(t)$ using a Fourier transformation into the frequency domain.

Moreover, taking into account the input driving power ($P_{in}$) required, which is quite substantial with RFPAs. An alternative definition called *PAE* [19] is defined as follows:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{1.5}$$

*PAE* is affected by the RF power gain (defined as $Gp = P_{out} - P_{in}$ in dB). Generally speaking, *PAE* is close to $\eta$ with sufficiently high power gain, but when the RF power gain is less than 10 dB, the drive power will seriously impact *PAE*. Regardless of both definitions, a high degree of efficiency always requires less DC power and/or higher RF output power.

### 1.3.1 Efficiency in the Full Power Region

At full power drive or in saturation power region, the most important aspect for operation mode identification is the intrinsic voltage and current waveforms, i.e., $v_{DS}(t)$ and $i_{DS}(t)$. High efficiency can be achieved if the overlap of current and voltage waveform is minimized as low losses in the transistor. This indeed belongs to the waveform engineering category [20, 21, 22]. These waveforms vary with circuit impedance settings, which means that the SSPAs can achieve high efficiency through proper impedance matching settings, this involves load-pull technologies.

For high-efficiency operation modes, such as Classes D, E, F, etc., most of them are associated with switching and/or harmonic tuning technology. Class-E operation mode is basically classified as a switching mode that replaces the previously used active device characteristics with a simple, theoretically perfect switch. At the high-power level, the process of making a transistor behave like a switch requires some tricks involving the use of knee range as well as the threshold of the device characteristics. The switch is shunted by a capacitor, which in turn is shunted by a series resonant circuit. The shunt capacitor can directly utilize the parasitic capacitor $C_{ds}$, but a large capacitance of $C_{ds}$ might prevent this mode as the shunt capacitor is already determined to

[2]Voltage and Current signals are denoted as follows. Lower case with upper case subscript plus a hint $(t)$ means the **time domain** signal, e.g. $v_{DS}(t)$. Upper case with subscript $dc$ represents DC component, e.g. $V_{dc}$. Upper case with lower case subscript means fundamental frequency component, e.g. $V_{ds}$, while when it comes plus a number $n$ after a comma in the subscript, it means the $n\,th$ harmonic frequency component, e.g. $V_{ds,2}$.

a proper value [23, 24]. Class-D operation mode or Class-S mode at higher frequencies is in the category of pulse width modulation (PWM) technique. The PA is driven by a constant amplitude of the PMW signal, the amplitude is sufficient to drive the device into a full rail-to-rail Class-B state. The device current waveform therefore consists of a series of half-wave rectified sinusoidal pulses of amplitude $I_{max}$ during the ON part of the PWM cycle, and of course, both the RF and DC components of the current are zero during the OFF part of the cycle [25]. Moreover, harmonic control modes like Class-F and Class-$F^{-1}$ are discussed in Chapter 3. And it can be expected that more amplifier classes will be explored as transistor technology improves.

### 1.3.2 Efficiency in the Back-off Power Region

Compared to vacuum tube technology, SSPAs have the advantage that they can work well at various output power levels. But the efficiency is significantly reduced in the lower power range compared to the saturated power region when running in a single transistor.

The RF power sources, such as for the radioisotope productions, are not always running at full power, most of the time they are running at reduced power levels, therefore, increasing this part of efficiency is also very crucial. Efficiency enhancement technology aims to maintain an efficiency level over a wide power range not limited to saturation region only. Therefore, to achieve high efficiency at different power levels or sufficient back-off power ranges, several different efficiency enhancement technologies could be considered, such as bias modulation [26, 27, 28], load modulation [29, 30, 31, 32, 33], and both technologies mixed [34, 35]. Their theoretical principles are concisely summarized in Figure 1.4. In the following principle analysis, the class-B bias condition is assumed.

**Load Modulation**

Both at full and low power drive the bias voltage or DC component is $V_{DD}$, but at low power drive, with load modulation, the slope of load-line becomes flatter, implying that it generates a significantly higher voltage as indicated in Figure 1.4, i.e., from $V_{ds2}$ to $V_{ds1}$, with the same DC voltage and same current value. From (1.4), $\eta$ at low power drive can be improved to the same level as full-power drive by means of increased $V_{ds}$ or $P_{out}$ since having the same DC power. Meanwhile, this also implies that the matching impedance (determined by the load-line slope) increases to a higher level, which requires a matching adjustment. This can be implemented by e.g. the Doherty architecture [36, 37, 38, 39], out-phasing architectures [40, 41, 42], load modulated balanced amplifier [43, 44], and the more recent varactor-based dynamic load modulation [45, 46, 47], etc.

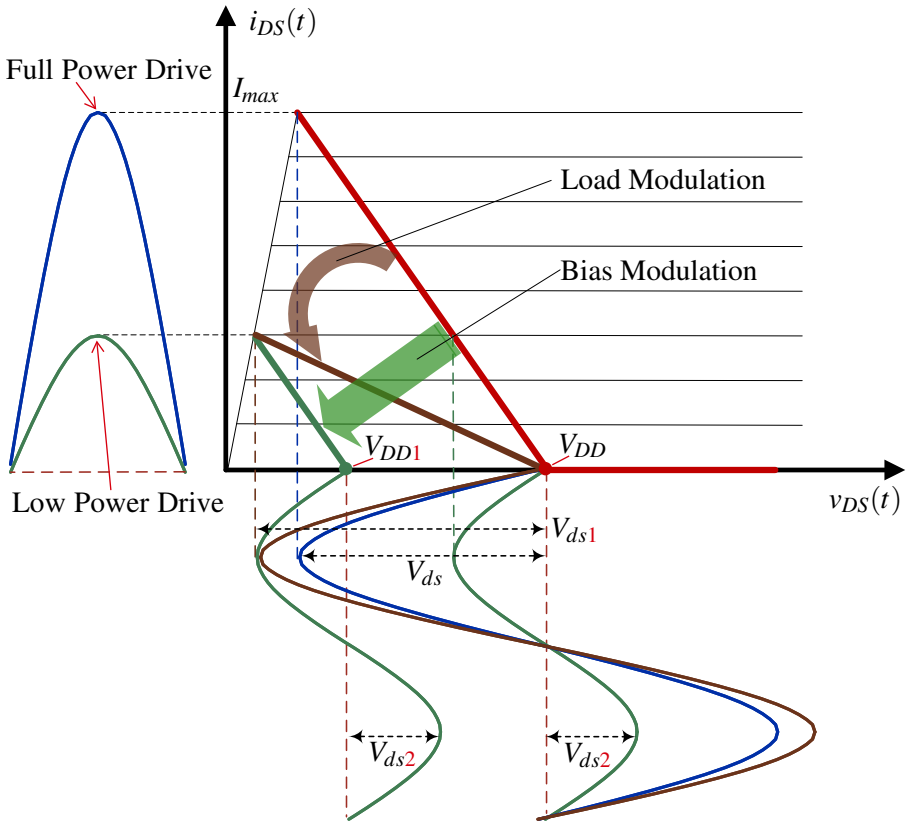



*Figure 1.4. Diagram for load modulation and bias modulation with load lines under class-B bias condition.*

**Bias Modulation**

Generally, bias modulation is also known as supply modulation. Similar to load modulation as shown in Figure 1.4, the bias voltage at full power drive is $V_{DD}$ but reduces to $V_{DD1}$ at low power drive when bias modulation is applied. It can be observed that the slopes of load-lines are the same regardless of full and low power drive, this indicates that the voltage keeps constant, i.e. $V_{ds2}$, which also means that the amplifier outputs the same $P_{out}$ but reduces DC power considerably. Then from (1.4), $\eta$ at low power drive improved and can be achieved at the same level as full drive. The advantage of bias modulation is that the slope of the load-line shows no change, indicating that no change is required for the matching impedance from all power ranges. Most bias modulation is about drain bias as discussed above, but it also includes gate bias [48] as well as dual gate and drain bias modulation [49, 50]. Bias modulation is not limited to the circuit module, it can also be applied to load-pull technologies [51].

With high-bandwidth bias modulation, the bias voltage for the PA is modulated with the instantaneous envelope of the signal. When the bias continuously tracks the input envelope, the concept is known as Envelope Tracking (ET) [19, 52]. Another way to achieve higher modulation bandwidths is to modulate the bias in discrete steps, which is known as discrete level bias modulation, or Class-G [53, 54]. For applications that do not require fast dynamic output power change, a simple quasi-static drain bias adjustment with limited bandwidth for different output power levels is easier to implement [20, 55].

In a nutshell, the core of load modulation is to increase RF output power, while the core of bias modulation is to reduce DC power. These back-off efficiency enhancement technologies come with different cons and pros, and are suitable for different applications.

Overall, on the one hand, highly efficient PA can improve the efficiency of RF power usage, save RF energy, and save on electricity costs, while on the other hand, high efficiency means less dissipated power, which in turn also reduces the requirements for high specification thermal management.

## 1.4 Power Combining Considerations

An interesting question for back-off efficiency to consider is if it would be an option to enable back-off power efficiency by shutting down some SSPAs in the cluster. This solution reduces the overall combined output power and keeps the remaining SSPAs running at high efficiency status since the remaining SSPAs are running at full power, i.e., saturation. This also ties in with another interesting and important question: what would happen if one or/and a few of the operated transistors fail or break? These two questions look different but are actually essentially the same as both refer to the power combining principles.

The associated answers are divided into two classes depending on whether the combiner is isolated or not. For isolated power combiners, e.g., [56, 57, 58], assuming that each transistor or SSPA module can deliver the same power $P_o$, when $x$ paths of transistors fail in an $N$-way combiner, the total residual output power $P_{o\_total}$ is derived and given as:

$$P_{o\_total} = \frac{(N-x)^2}{N} P_o \tag{1.6}$$

As observed it's not the simple $(N-x)P_o$ as thought, the reason is that part of the delivered power is dissipated at the isolated resistor(s). Therefore, powering down some SSPAs in the cluster cannot achieve high efficiency in the back-off power region if adopting the isolated combiner. But the rest of the SSPAs will not be affected by the broken SSPAs because the SSPAs are isolated from each other, with no coupling between them, which also implies that the matching conditions are not changed.

While things become much more complicated in the non-isolated cases, such as [59, 60, 61], because the coupling affects the matching impedance for the rest of the SSPAs, a chain reaction can occur when the mismatch makes the transistors operate in a dangerous area on the Smith chart, causing all transistors to fail. However, there still is an accessible and trustworthy solution to check the behavior response if some SSPAs fail if adopt the active S-parameters and the S-parameter to S-parameter conversion which will be present in (2.12). First, the measured S-parameter of combiner can be converted to the case when reference impedance of corresponding ports in the *Open* condition, since the failed transistor can be treated as an *Open* state, and then the active S-parameter to verify the frequency response ca be calculated when other SSPAs are still active.

Moreover, due to most RF source applications being narrow band, the combiner can be designed for very low loss, but sometimes sacrifices bits of combining efficiency for compactness. Considering that the combiner delivers up to tens, hundreds of kilowatts, even if the combiner efficiency increases to 98%, in other words, around 0.1 dB loss, it still results in 200 W and 2000 W dissipated power respectively by the combiner itself, the thermal issues cannot be ignored under such conditions and need further attention.

## 1.5 Challenges and Scientific Contributions

As is known, high-power RF sources have wide applications in radar, RF heating, RF energy, communication system, etc., particularly in the HF, VHF and UHF bands [62]. While the study and research of solid-state RF power sources continued for many decades with the rapid development of semiconductor technologies and the demands of a variety of applications. The cost of high-power RF sources comes primarily from thermal management and operational costs, e.g., a tens kilowatt RF source consumes a large amount of electrical energy, meanwhile, the cooling systems must work in real-time to reduce the temperature impact from power dissipation. Thus it is imperative to develop high efficient RF power source as low energy efficiency leads to high running costs, large heat dissipation and increased ecological footprint[3]. Most importantly, as shown in Figure 1.2, the efficiency of the RF power source is determined by the power amplifier modules. Thus it can be said that the success of the RF power source depends on the SSPA used.

In summary, the RF power source development encompasses the following three main challenges:

[3]The ecological footprint is a method promoted by the Global Footprint Network to measure human demand for natural capital, i.e., the amount of nature needed to feed people or an economy [63].

- **High Power**: The required power level is up to kilowatt for a single SSPA module and goes up to several tens or hundreds of kilowatts for the power source system. Such high power requirements pose numerous challenges for power combining technology and lead to inevitable thermal complications due to power dissipation.
- **High Efficiency**: High efficiency not only benefits running costs but also reduces the requirements on the thermal management system due to the reduction of dissipated power. But the use of large periphery transistors might prevent the enhanced efficiency technology such as higher-order harmonic tuning, while efficiency improvements in the back-off power region also need to be explored considering the significant power consumption in this region.
- **Measurement Set-up**: It is also a great challenge to measure in the kilowatt or even tens of kilowatt power ranges, which definitely exceeds the power level of measurement instruments. To evaluate the RF performance of design and protect instruments, a secured and dedicated RF measurement bench is required.

Based on the above considerations, the overall research goal of this thesis is to develop core technologies for high efficient RF power sources and meanwhile provide new understandings of the SSPA architecture from circuits, design methods, and analytical approaches. These analytical approaches allow for a better understanding of the fundamental workings of a given architecture/circuit and provide insight into its capabilities and limitations. Overall, the thesis presents promising architectures and techniques for improved RF performance in saturation and back-off power region, such as *multimode* PA and quasi-static supply modulation, etc. methodology.

***The relevant research in this thesis has a direct benefit for industry and leads to new methods and tools to improve energy efficiency and thus reduce the environmental impact. The knowledge gained and technologies developed are not limited to the thesis focus, i.e., radioisotope production applications, they can also be applied to other RF energy systems.***

## 1.6 Scope of this Thesis

This thesis aims at a comprehensive understanding of the novel efficient RF power source from theoretical perspectives to practical implements, in particular on the efficiency improvements as well as their measurements. The tree structure of this thesis is summarized in Figure 1.5 and its detailed contents are organized as follows:

Chapter 2 focuses on measurement technologies from small-signal to large-signal measurement. The calibration procedure is briefly introduced in the part on small-signal measurement, i.e., S-parameter measurement in RF/microwave

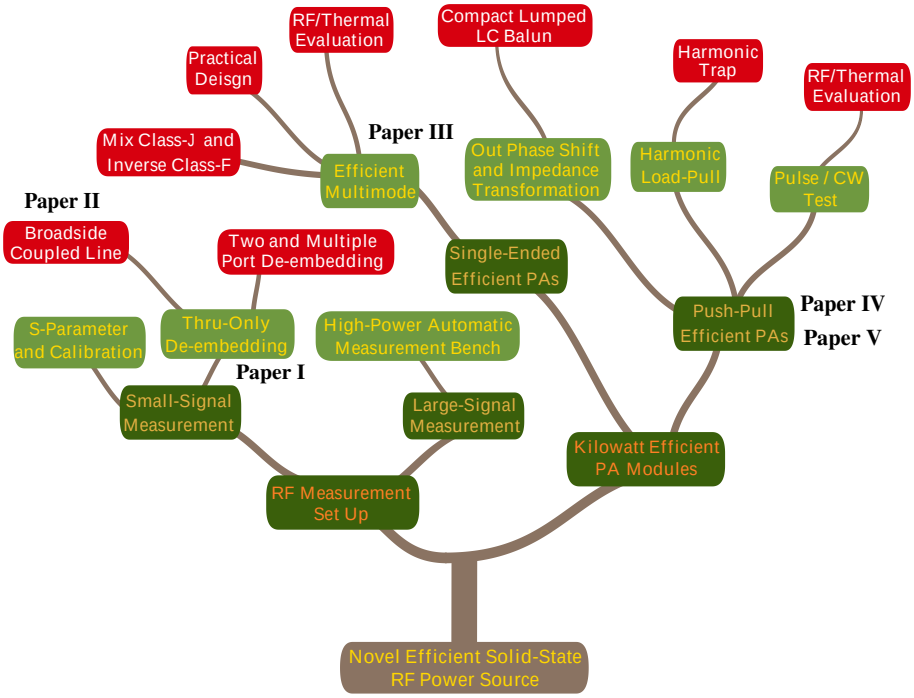



*Figure 1.5. Structure tree of works in this thesis.*

field, and introduces a novel thru-only de-embedding approach (**Paper I**) to characterize the devices or modules, on multiple ports conditions, such as coupled line or broadside coupled lines (**Paper II**). While high power measurement as the large-signal measurement to support the kilowatts power range is developed, and further realized as an automatic measurement bench.

Chapter 3 presents an efficient *multimode* PA (**Paper III**) which combines class-J and class-$F^{-1}$ operation modes. Its internal waveform is analyzed based on waveform engineering technology, RF performance trade-offs are investigated, and practical design is also evaluated.

Chapter 4 introduces a compact and efficient lumped push-pull PA module and covers the second harmonic load-pull technology (**Paper IV**) as well as its design as well as RF and thermal evaluation (**Paper V**). Moreover, the lumped balun design methodology is introduced and efficiency at both saturation and back-off region is investigated and analyzed by applying quasi-static supply modulation technology.

Finally, Chapter 5 goes to the conclusion of this thesis and discusses future perspectives.

# 2. RF Measurements

The essence of measurements is to quantify an unknown property by comparing it to a known or standard quantity. This also applies to RF measurements, where the standard properties to be characterized, such as output power and gain, are measured using traceable standards and ever-improving methods, developed and verified in international collaborations and monitored by national institutes. RF measurement not only serves to check the final performance of RF devices or RF modules but also in the design process for tuning and for optimizing a design in order to achieve the given goals. Accurate testing is important as it plays a key role in evaluating whether a design to a certain degree of accuracy can be verified to meet the specifications or not. Inaccurate measurements, however, can result in additional costs through extended design cycles and even impact theoretical analysis if conclusions are drawn from erroneous results. Accuracy should always be considered in RF measurement but practically it is difficult to achieve 100% accurate measurements. Hence, measurements cannot be assumed to be completely error-free but they should be conducted using best practices based on established methods to assure that the results are within acceptable and known error tolerances. RF measurement is a broad and complex subject and this chapter only provides some key aspects that have been required for the RF coaxial test-fixture measurements, and SSPA modules that have been conducted in the kilowatts range.

## 2.1 Small-Signal Measurement

Small-signal measurements refer to measurements conducted under conditions where the device under test (DUT) experiences linear behavior. This means that the output signal is a linear replica of the input signal, possibly altered in amplitude by a fixed loss or gain and shifted in phase but for small-signal measurements, the gain and phase shift is independent of the signal amplitude. In the RF/microwave range, the wavelength is short and gets close to the dimensions of the conductor that carries the signal, i.e., the transmission line. Therefore, the voltage and current change along the line and over time which makes them difficult to measure. Instead, the concept of scattering or S-parameters has been developed. These parameters are based on the relationships of impedance normalized voltage waves along the transmission line. They can be readily characterized using a vector network analyzer (VNA). Using the VNA the magnitude and phase of the incident, reflected and transmitted

signals can be measured relative to each other at calibrated reference planes. This gives the set of S-parameters of the network that completely describes the linear behavior of the network. The other sets of network parameters like admittance or impedance can be deduced if needed. With additional information about the power at the reference plane, the voltage and current waves can also be deduced if some properties of the transmission lines are known. The $n$-port scattering matrix or [S] matrix is defined in terms of incident $a$ and reflected $b$ voltage waves as

$$\begin{bmatrix} b_1 \\ \vdots \\ b_N \end{bmatrix} = \begin{bmatrix} S_{11} & \cdots & S_{1N} \\ \vdots & \ddots & \vdots \\ S_{N1} & \cdots & S_{NN} \end{bmatrix} \begin{bmatrix} a_1 \\ \vdots \\ a_N \end{bmatrix} \tag{2.1}$$

For higher frequencies, the VNA is the dominating test system that enables RF and microwave devices to be characterized in terms of network scattering parameters [64] but its capabilities extend much further today with capabilities to conduct multi-tone and wideband non-linear large-signal measurements. With the development of high-frequency oscilloscopes, it is also possible to use an oscilloscope as a receiver to measure the voltage of the incident and reflected wave in a certain reference plane. This has advantages since the oscilloscope immediately captures the time-domain signal including possible harmonics. In any case, the calibration, i.e., the method to establish the reference plane for the measurement is based on frequency domain correction of each harmonic component.

### 2.1.1 Classical Calibration Methods

Instrument calibration in general refers to the verification that certain equipment meets its specification and this has to be conducted regularly. How and how frequent is a decision for each lab and often regulated in a quality management system (QM). The calibration here does not refer to the verification of the equipment, instead, it refers to the routine of establishing the reference plane for the RF measurement. This is a regular routine that needs to be conducted every time something is changed in the test set or if any of the instruments has drifted due to time or possible temperature changes. Establishing the reference plane can be solved by involving a system error model mathematically to move the electrical reference planes from the instrument ports, or in reality some virtual interface at the receivers of the VNA, to the calibration planes. For a two-port system, several error models including the 8-term, the 12-term, and the 16-term have been developed [65]. The 8-term and 12-term models are the most used methods and the extraction of the parameters can be made using the well-known TRL and SOLT methods. Thus TRL and SOLT being the two main methods they are summarized below.

**SOLT**: acronym for Short, Open, Load, Through (Thru), is suitable for coaxial measurements as well as on-wafer measurements. As the name suggests, this requires access to known standards Short, Open, precision Load (typically 50 Ω) and a Thru. The standards do not have to be ideal but known. It is best if the test ports are of the same connector type (such as N, SMA, or K, etc.) but of different genders, so the Thru just requires the test ports are connected together. If not the Thru has to be defined to the length and loss. The SOLT calibration method is less suitable for waveguide measurements where obtaining an Open standard or Load standard is difficult. It is also less suitable for measurements on non-coaxial test fixtures, where the same problems exist in finding suitable standards. For some non-coaxial cases simply contain additional coaxial connectors that connect instruments, SOLT is still an easy method when connectors can be de-embedded. Keysight provides a method that builds connector model to de-embed the connectors [66], which is much easier at low frequency range since losses can be omitted and a phase shift only can be assumed for the Thru. And this also only applies to measurements without high precision requirements.

**TRL**: acronym for Through, Reflect, Load, is a useful method for microwave, non-coaxial environments such as fixtures, on-wafer, or waveguides. TRL uses a transmission line that is significantly longer in electrical length than the Thru and has a known length and impedance as one standard. TRL also requires a high reflection standard (usually Short or Open) which impedance does not need to be well characterized but they must be electrically the same for both test ports [67]. The condition of the known length of the Line is not absolute, and in reality, the length can be measured during the calibration but it has to be significantly different than the Thru standard length, and for wideband measurements, several Lines may have to be used.

### 2.1.2 Active S-Parameters

In a normal S-parameter measurement, only one port is excited and the reflection at that port as well as the transmission to all other ports in the network is measured. It is assumed that all ports are terminated with 50 Ω. Each port is then excited and finally the values for all S-parameters are found. Active S-parameters characterize the performance of a network when more than one port is excited simultaneously. The signal propagating from any port consists of the superposition of its own passive self-reflection and the coupled signals from the other ports [68]. Thus, the definition of the active scattering parameter is given as

$$activeS_{mn} = \frac{\sum_{i=1}^{N} S_{mi} a_i}{a_n} \tag{2.2}$$

where $S_{mi}$ is the general usage of standard passive S-parameters measured directly by the VNA.

This parameter is commonly used in large array antennas due to the mutual coupling of different radiating elements, while it is also a very useful tool and concept for power combining in high power RF applications due to active excitation on multiports, such as the balun, multiport power combiners, etc. Therefore, this parameter is presented here in its own section for introductory purposes. A brief introduction to the concept, more details, and a particular example will be developed in Section 4.2.1.

### 2.1.3 Thru-Only De-embedding Approach

For compact purposes, coupled lines or broadside coupled lines [69] in planar circuits are widely used in high-power RF applications, such as planar balun, but most of these structures are hard to characterize because of massive calculations for their complicated multiports, thus, test fixtures must be employed because of non-coaxial environments. Therefore, a newly thru-only approach is proposed in **Paper I** to characterize this type of structure and significantly simplify the de-embedding process.

The classic coupled line and broadside coupled line in **Paper II** are first briefly introduced in this subsection, after which the detailed process of the proposed thru-only de-embedding approach is further proposed.

**Broadside Coupled Line**

Coupled transmission lines can support two distinct propagating modes, and this feature can be used to implement a variety of practical directional couplers, hybrids, balun, filters, etc. Generally, coupled transmission lines can be implemented using microstrip, stripline, or even coaxial lines.

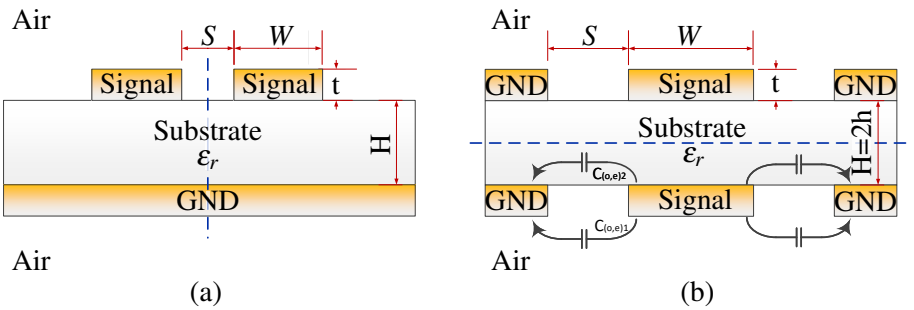



*Figure 2.1. Cross-sectional view of (a) conventional coupled microstrip line, and (b) broadside coupled transmission line. Where the dashed line represents the E- wall or H-wall.*

The cross-sectional view of the conventional coupled microstrip line is shown in Figure 2.1(a). The two signal lines (Signal) are on the same side, i.e.,

on the top, while the ground plane (GND) is on the opposite side. The electrical properties of such coupled microstrip lines can be entirely determined by the effective capacitances between the lines. Such a structure is successfully used in the design of filters and power dividers, etc. While the cross-sectional view of the broadside coupled transmission line is shown in Figure 2.1(b). It can be seen as two coplanar waveguide (CPWs) transmission lines combined back to back with no ground. It can also be viewed as a broadside coupled stripline with no cover but with the suspended ground [70]. Due to its simplicity and compactness, this structure can be easily implemented on printed circuit boards (PCB).

The classical coupled line in Figure 2.1(a) is fully investigated in [18]. While a formula-based brief study is explored to analyze the broadside structure in Figure 2.1(b), the following formula fully describes this structure by considering the even/odd characteristic impedance and is given by

$$Z_{0(e,o)} = \left[ c_v \sqrt{C_{(e,o)} C^a_{(e,o)}} \right]^{-1} \tag{2.3}$$

where $c_v$ is the velocity of propagation in free space. $C_{(e,o)}$ is the even or odd-mode capacitance per unit length, $C^a_{(e,o)}$ is the capacitance when the substrate dielectric is replaced with air. The lower case subscript "$e$" and "$o$" stands for "even" and "odd" mode respectively. To express $C_{(e,o)}$ effectively, the structure can be modeled as two symmetrical half-planes separated by magnetic/electric walls (dashed line in Figure 2.1(b)). Due to the symmetric distribution of the E/H field, the total capacitance $C_{(e,o)}$ in even or odd mode can be considered as the sum of two components $C_{(e,o)1}$ and $C_{(e,o)2}$ representing the capacitance in air and in dielectric respectively, their corresponding symbols are depicted in Figure 2.1(b).

$$C_{(e,o)} = C_{(e,o)1} + C_{(e,o)2} \tag{2.4}$$

And $C_{(e,o)1}$ and $C_{(e,o)2}$ are formulated as follows

$$k_{(e,o)1} = \frac{W}{W+2S} \tag{2.5}$$

$$k_{e2} = \sinh\left(\frac{\pi W}{4h}\right) / \sinh\left(\frac{\pi (W+2S)}{4h}\right) \tag{2.6a}$$

$$k_{o2} = \tanh\left(\frac{\pi W}{4h}\right) / \tanh\left(\frac{\pi (W+2S)}{4h}\right) \tag{2.6b}$$

$$C_{(e,o)1} = 2\alpha_{(e,o)} \varepsilon_0 \frac{K\left(k_{(e,o)1}\right)}{K\left(k'_{(e,o)1}\right)} \tag{2.7}$$

$$C_{(e,o)2} = 2\varepsilon_0\varepsilon_r \frac{K\left(k_{(e,o)2}\right)}{K\left(k'_{e(e,o)2}\right)} \tag{2.8}$$

where $K(k)$ and $K(k')$ are the complete elliptic integrals of the first kind and their complements, and $k' = \sqrt{1-k^2}$.

More details and the verification can be found in **Paper II**.

**Basic Principles of Tapered Line Based Thru-Only De-embedding**

Literally, "Thru-Only" means that only the Through standard (THRU) is preserved during the de-embedding process. Considering the symmetrical characteristic of a two-port passive THRU, i.e., $S_{22M} = S_{11M}$, $S_{21M} = S_{12M}$, the directly measured scattering parameter $S_M$ is given by VNA as follows:

$$S_M = \begin{bmatrix} S_{11M} & S_{12M} \\ S_{12M} & S_{11M} \end{bmatrix} \tag{2.9}$$

While due to reciprocal properties, the scattering matrix of the left half of THRU $S_{Lh}$[1] can be described as follows:

$$S_{Lh} = \begin{bmatrix} S_{11} & S_{12} \\ S_{12} & S_{22} \end{bmatrix} \tag{2.10}$$

Since THRU consists of the left half of it and its mirrored right half, solving (2.9) and (2.10) leads to:

$$S_{11M} = S_{11} + \frac{S_{22}S_{12}^2}{1-S_{22}^2} \tag{2.11a}$$

$$S_{12M} = \frac{S_{12}^2}{1-S_{22}^2} \tag{2.11b}$$

As observed, $S_{Lh}$ with three unknowns ($S_{11}$, $S_{12}$ and $S_{22}$) cannot be obtained mathematically from the two independent equations (2.11a) and (2.11b). Reasonably, it could have a solution if eliminating an unknown or adding a new independent equation by making some functional correspondence between any two of the three unknowns. But before exploring this idea further, a very important conversion between S-parameters should first be developed.

**S-parameters Convert to S-parameters**: $S_n$ is defined as an n-port scattering matrix where all port reference impedance is $Z_0$. $Z_0$ is the environmental system impedance, generally, it is specified to 50 Ω. While $S'_n$ is also defined

[1]The word "*Lh*", "*Rh*" and "*THRU*" in the subscript stands for "Left Half" of THRU standard, "Right Half" of THRU standard and THRU standard respectively, which also applies to the following named symbols.

as an n-port scattering matrix but where the reference impedance of port $N$ is $Z_{xN}$. The functional relationship between $S_n$ and $S'_n$ is given as

$$S_n = \frac{D_x^{-1} - D_x + \left(D_x^{-1} + D_x\right) S'_n}{D_x^{-1} + D_x + \left(D_x^{-1} - D_x\right) S'_n} \tag{2.12}$$

where

$$\begin{aligned} D_x^{-1} &= \begin{pmatrix} \sqrt{R_{x1}} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & \sqrt{R_{xN}} \end{pmatrix} \\ &= \operatorname{diag}\left\{\sqrt{R_{x1}}, \cdots, \sqrt{R_{xN}}\right\} \end{aligned} \tag{2.13}$$

The derivation procedure for (2.12) is given in Appendix A. $R_{xN}$ in (2.13) is the impedance ratio between $Z_0$ and reference impedance $Z_{xN}$ at port N, which is defined as $R_{xN} = Z_{xN}/Z_0$.

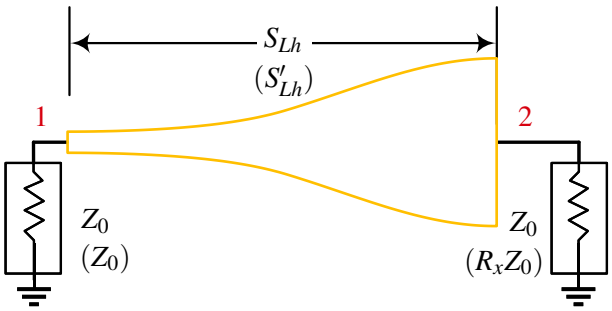



*Figure 2.2. Two-port left half of tapered THRU. $S_{Lh}$ will convert to $S'_{Lh}$ (where $S'_{22} = -S'_{11}$) when reference impedance of port 2 changes from $Z_0$ to $R_x Z_0$.*

When it conducted to two-port network as shown in Figure 2.2, $Z_{x1} = Z_0$ and $Z_{x2} = Z'_0 = R_x Z_0$, then

$$D_x^{-1} = \operatorname{diag}\left\{1, \sqrt{R_x}\right\} = \begin{bmatrix} 1 & 0 \\ 0 & \sqrt{R_x} \end{bmatrix} \tag{2.14}$$

Taking them into (2.12) to calculate $Z'_0$, and letting $S'_{22} = -S'_{11}$, gives

$$R_x = \frac{1 + S_{11} - S_{12}S_{21} + S_{22} + S_{11}S_{22}}{1 - S_{11} - S_{12}S_{21} - S_{22} + S_{11}S_{22}} \tag{2.15}$$

$R_x$ will act as a critical coefficient in this approach to account for the inherent physical properties of the transmission network.

As noted, a new independent equation $S'_{22} = -S'_{11}$ is derived when the reference impedance is properly $R_x Z_0$. $S_{Lh}$ now has mathematical solutions as three unknowns with three independent equations. But during the process, an unknown $R_x$ is involved, so stepped transmission lines are examined next to look for possibilities to physically solve $R_x$ from the only standard THRU.

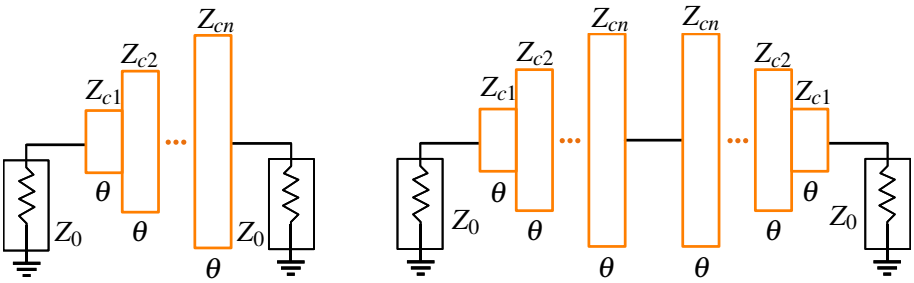



*Figure 2.3. (a) A n-section stepped transmission line, each line with the same length $\theta$ but with different characteristic impedance $Z_{cn}$; (b) Two n-section stepped transmission line of (a) connected symmetrically as THRU.*

**Stepped Transmission Line**: A n-section stepped transmission line is depicted in Figure 2.3(a). Every separate line has the same electrical length $\theta$ but with different characteristic impedance $Z_{cn}$. For exponential and triangular tapered transmission lines that are used in general (their "continuous" form can be found in [18]), their corresponding "distributed" $Z_{cn}$ are given as:

$$Z_{cn\_exp} = Z_c \cdot \alpha_{exp}^{n-1} \tag{2.16a}$$

$$Z_{cn\_tri} = \begin{cases} Z_c \cdot \alpha_{tri}^{2(\frac{n-1}{N-1})^2}, 1 \le n \le \frac{N+1}{2} \\ Z_c \cdot \alpha_{tri}^{4\frac{n-1}{N-1}-2(\frac{n-1}{N-1})^2-1}, \frac{N+1}{2} \le n \le N \end{cases} \tag{2.16b}$$

Where $Z_c$ is the characteristic impedance, coefficient $\alpha_{exp}$ and $\alpha_{tri}$[2] are positive real number, represents the ratio of an adjacent section of the transmission line.

The coefficient $R_{x\_Lh}$ for exponential and triangular tapers are derived from (2.15) and is given by:

$$R_{x\_Lh\_exp} = \frac{\alpha_{exp}^{n-1} {Z_c}^2}{{Z_0}^2} (n \in \mathbb{N}^+, \alpha_{exp} \in \mathbb{R}^+) \tag{2.17a}$$

$$R_{x\_Lh\_tri} = \frac{\alpha_{tri} {Z_c}^2}{{Z_0}^2} (\alpha_{tri} \in \mathbb{R}^+) \tag{2.17b}$$

Regardless of both taper structures, $R_{x\_Lh}$ is independent of the electrical length $\theta$, which implies that $R_{x\_Lh}$ is kept constant with frequency for stepped transmission lines.

Figure 2.3(b) gives two n-section stepped transmission line connected symmetrically as a THRU module. To have a simplified expression form of $R_{x\_THRU}$

[2]The word "*exp*" and "*tri*" in the subscript stands for "exponential" and "triangular" structure respectively, which also applies to the following named symbols.

for the corresponding type of THRU, non-zero coefficients $\kappa$ and $\gamma$ are employed. With the similar derivation process of $R_{x\_Lh}$, $R_{x\_THRU}$ for both taper are given by:

$$R_{x\_THRU\_exp}=\frac{{Z_c}^2}{{Z_0}^2}\cdot\frac{\alpha_{exp}^{n-1}\cos^4\theta+\kappa_1\cos^2\theta\sin^2\theta+\kappa_2\sin^4\theta}{\cos^4\theta+\gamma_1\cos^2\theta\sin^2\theta+\gamma_2\sin^4\theta} \tag{2.18a}$$

$$R_{x\_THRU\_tri}=\frac{{Z_c}^2}{{Z_0}^2}\cdot\frac{\alpha_{tri}\cos^4\theta+\kappa_3\cos^2\theta\sin^2\theta+\kappa_4\sin^4\theta}{\cos^4\theta+\gamma_3\cos^2\theta\sin^2\theta+\gamma_4\sin^4\theta} \tag{2.18b}$$

Assuming the electrical length $\theta$ is short enough, and taking $\sin\theta = 0$, $\cos\theta = 1$ into (2.18), the form then reduces to (2.17). It implies that the desired $R_{x\_Lh}$ can be obtained from $R_{x\_THRU}$ by ensuring a small $\theta$. This can be achieved by two methods: a) design the physical length of the test fixture as short as possible; b) measure the low-frequency characteristics since the frequency is proportional to electrical length $\theta$.

Although different characteristic impedances (or different widths) in the adjacent transmission lines will inevitably cause discontinuities, a good solution is to make the stepped transmission line smooth or streamlined to minimize the discontinuity effect.

In summary, $R_x$ can now be obtained from $R_{x\_THRU}$ (THRU standard only) in the low frequency band. But it has to meet two requirements: a) $R_x$ remains constant or has a small variation with frequency; b) $R_x$ and $R_{x\_THRU}$ are related at some specific frequency points. Fortunately, it has been found that the general used exponential and triangular taper satisfies the two conditions perfectly.

**Two-port Thru-Only De-embedding**

In order to verify the proposed thru-only approach in the two-port network, TRL standards shown in Figure 2.4 are established and measured, compared to the thru-only standard shown in Figure 2.4(b).

According to the proposed methodologies described in the last section, the de-embedding procedure goes as follows:

**1) Calculate** $S'_{Lh}$: As mentioned above, when the reference impedance of port 2 in Figure 2.2 changes from $Z_0$ to $R_xZ_0$, the corresponding scattering matrix changes from $S_{Lh}$ to $S'_{Lh}$, and the new independent equation $S'_{22} = -S'_{11}$ can be derived under this condition. Then $S'_{Lh}$ is rewritten as:

$$S'_{Lh} = \begin{bmatrix} S'_{11} & S'_{12} \\ S'_{12} & -S'_{11} \end{bmatrix} \tag{2.19}$$

As observed, only two unknowns remain in (2.19), and incorporating them into the independent equations (2.11a) and (2.11b), the solution is given as:

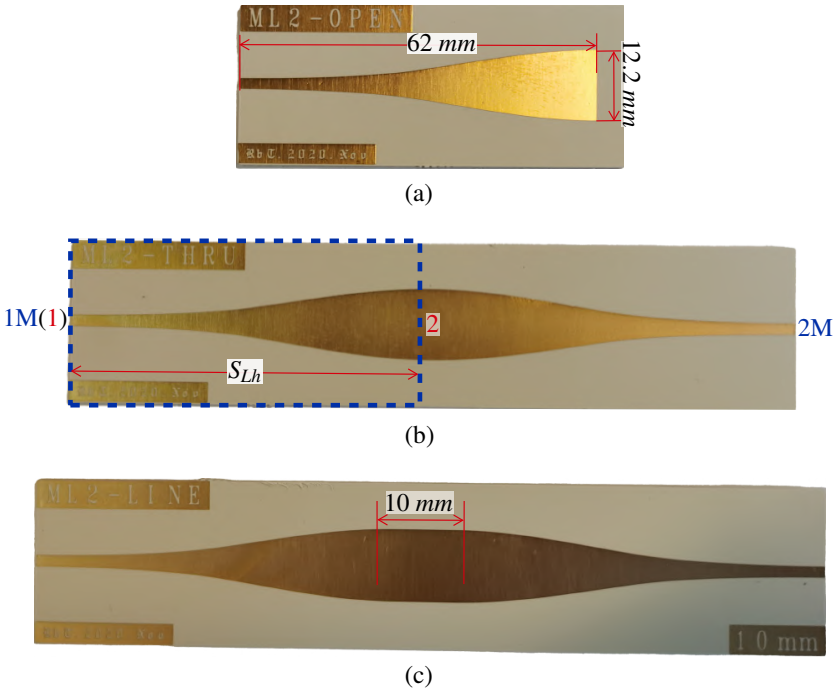



*Figure 2.4. Photograph of fabricated standards with dimensional markings. (a) Reflection: Open; (b) THRU; (c) Line. Measured (a), (b), and (c) data are used for the TRL method, while only measured data from (b) is used for the thru-only method. Additionally, port numbers are also specified for clarification.*

$$S'_{11} = \frac{S_{11M}}{1 - S_{12M}} \tag{2.20a}$$

$$S'_{12} = \pm \frac{\sqrt{S_{12M} - S^2_{11M} S_{12M} - 2S^2_{12M} + S^3_{12M}}}{\sqrt{1 - 2S_{12M} + S^2_{12M}}} \tag{2.20b}$$

While $S_{Lh}$ can be converted from $S'_{Lh}$ through (2.12). This implies that $S_{Lh}$ can be obtained from this thru-only method if $S_M$ and $R_x$ are determined.

$S'_{Lh}$ in (2.19) is obtained from (2.20a) and (2.20b) once $S_M$ is measured directly by VNA. Naturally, the phase of $S'_{12}$ is gradually changed with frequency increase, so the sign of "+" or "-" (180° phase shift) in (2.20b) can be determined by the phase of its adjacent frequency points.

**2) Select $R_{x\_THRU}$ in the low-frequency band for $R_{x\_Lh}$**: Figure 2.5 gives $R_{x\_THRU}$ which is calculated from (2.15) based on the measured $S_M$. In the low-frequency range, this means that the corresponding electrical length $\theta$ is

very small, from (2.18) $R_{x\_THRU}$ in this low-frequency range is the chosen value for $R_{x\_Lh}$.

As verification for the conclusion in (2.17) and (2.18), Figure 2.5 also shows $R_{x\_Lh}$ calculated from $S_{Lh}$ using the TRL method as blue dotted line. It can be observed that $R_{x\_Lh}$ and $R_{x\_THRU}$ overlap in the low-frequency range, and the blue dotted line has a small variation over wide frequency bands. This is exactly in line with the theoretical speculation in the last subsection.

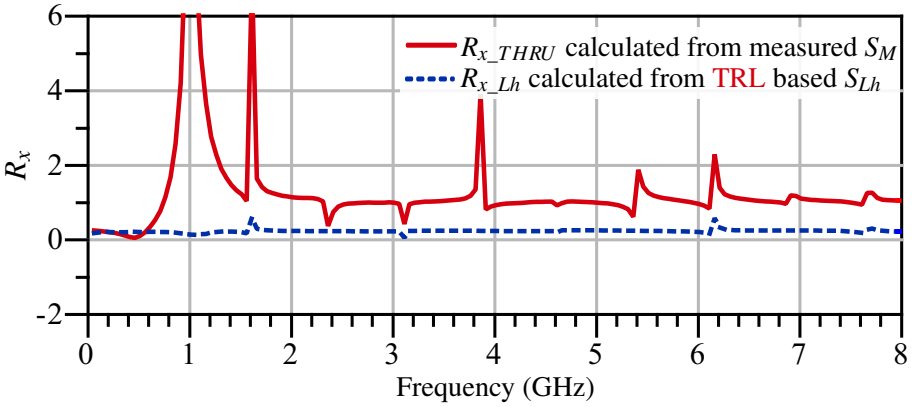



*Figure 2.5. The frequency response of $R_x$.*

**3) Calculate the desired** $S_{Lh}$: As known above, the calculated $S'_{Lh}$ in step 1) is the scattering matrix when the reference impedance of port 2 is $R_x Z_0$. Then an S-parameter conversion is required to target $S_{Lh}$ where the reference impedance of port 2 is $Z_0$. Such a conversion is revised from (2.12) as follows:

$$S_{Lh} = \frac{D_x^{-1} - D_x + \left(D_x^{-1} + D_x\right) S'_{Lh}}{D_x^{-1} + D_x + \left(D_x^{-1} - D_x\right) S'_{Lh}} \tag{2.21}$$

where

$$D_x^{-1} = \text{diag}\left\{1, \sqrt{R_x}\right\} = \begin{bmatrix} 1 & 0 \\ 0 & \sqrt{R_x} \end{bmatrix} \tag{2.22}$$

$R_x$ has already been figured out in step 2) by choosing the value of $R_{x\_THRU}$ in the low-frequency band. Finally, the desired $S_{Lh}$ is calculated back from the conversion in (2.21).

Then $S_{11}$, $S_{12}$ ($S_{21}$) and $S_{22}$ of $S_{Lh}$ are calculated based on the proposed thru-only method. In fact, several noisy points are observed from the initial data, hence an algorithm applying interpolation methods is used to filter out the noisy points, the corresponding processed results are shown in Figure 2.6. Meanwhile, as a comparison and benchmark, the calculated results based on the TRL method are also shown as a blue dotted line in Figure 2.6. As observed, the results of the proposed thru-only method and the TRL method agree very well.

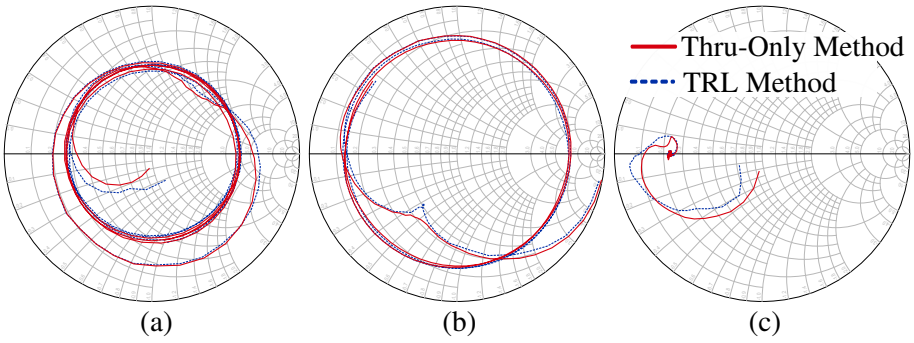



*Figure 2.6. Calculated (a) $S_{11}$, (b) $S_{12}$ ($S_{21}$) and (c) $S_{22}$ results based on proposed thru-only method as a comparison to TRL method in Smith chart at 10 MHz∼8 GHz frequency range.*

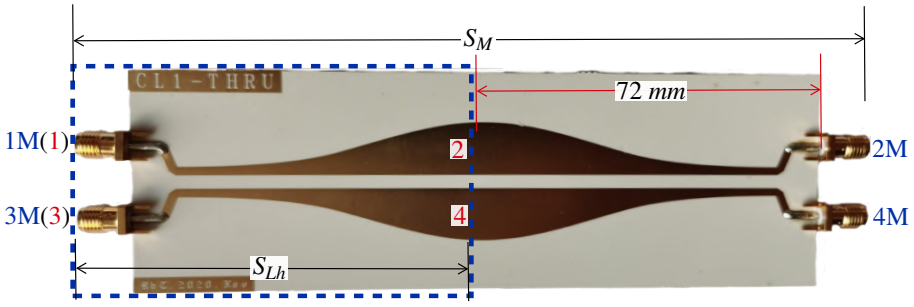



*Figure 2.7. Photograph of fabricated four-port THRU standard. Port numbers are also specified for clarification.*

**Four-port Thru-Only: Even- and Odd-Mode Methodology**

A four-port THRU standard, as shown in Figure 2.7, is fabricated to verify this thru-only method. As depicted in Figure 2.7, due to the symmetry features, the measured 4x4 scattering matrix $S_M$ with four known quantities is given by

$$S_M = \begin{bmatrix} S_{11M} & S_{12M} & S_{13M} & S_{14M} \\ S_{12M} & S_{11M} & S_{14M} & S_{13M} \\ S_{13M} & S_{14M} & S_{11M} & S_{12M} \\ S_{14M} & S_{13M} & S_{12M} & S_{11M} \end{bmatrix} \tag{2.23}$$

While because of the reciprocal features, the desired $S_{Lh}$ with six unknowns is simplified as:

$$S_{Lh} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{12} & S_{22} & S_{14} & S_{24} \\ S_{13} & S_{14} & S_{11} & S_{12} \\ S_{14} & S_{24} & S_{12} & S_{22} \end{bmatrix} \tag{2.24}$$

In general, a four-port network consists of even and odd mode networks. Furtherly, any $2N$-port network can be turned into an alternative representa-

tion with the same idea as the four-port network. Thanks to the symmetrical feature, the final processed $S_{M\_even}$ and $S_{M\_odd}$ are given by:

$$S_{M\_even} = \begin{bmatrix} S_{11M}+S_{13M} & S_{12M}+S_{14M} \\ S_{12M}+S_{14M} & S_{11M}+S_{13M} \end{bmatrix} \tag{2.25}$$

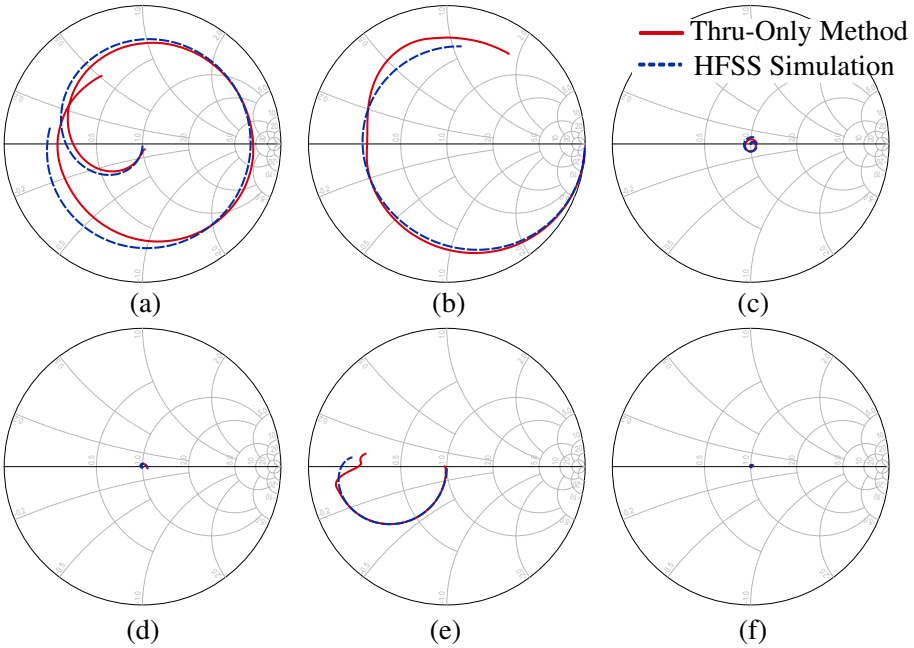



*Figure 2.8. Calculated (a) $S_{11}$, (b) $S_{12}$, (c) $S_{22}$, (d) $S_{14}$, (e) $S_{22}$ and (f) $S_{24}$ results based on proposed the thru-only method as a comparison to 3D EM simulation in Smith chart at 10 MHz∼2 GHz frequency range.*

$$S_{M\_odd} = \begin{bmatrix} S_{11M}-S_{13M} & S_{12M}-S_{14M} \\ S_{12M}-S_{14M} & S_{11M}-S_{13M} \end{bmatrix} \tag{2.26}$$

$S_{Lh\_even}$ and $S_{Lh\_odd}$ can be obtained separately from $S_{M\_even}$ and $S_{M\_odd}$ by performing the same procedure for the two-port as described in the last subsection respectively, after resolving the $R_x$ in even and odd mode. Finally, the form of $S_{Lh}$ is simplified as follows:

$$S_{Lh}=\frac{1}{2}\begin{bmatrix} S_{Lh\_even}+S_{Lh\_odd} & S_{Lh\_even}-S_{Lh\_odd} \\ S_{Lh\_even}-S_{Lh\_odd} & S_{Lh\_even}+S_{Lh\_odd} \end{bmatrix} \tag{2.27}$$

Finally, the calculated $S_{11}$, $S_{12}$, $S_{13}$, $S_{14}$, $S_{22}$ and $S_{24}$, which are required to fully describe $S_{Lh}$ in (2.24), are depicted in Figure 2.8. Meanwhile, the 3D EM simulation results on the left half of THRU are also presented in Figure 2.8 for a comparison. As observed, the calculated results based on the proposed thru-only method are in very good agreement with the EM simulations.

Moreover, **Paper I** also provides another method for de-embedding this four-port test fixture, and also gives more equations derivation processes in the appendices.

## 2.2 Large-Signal Measurement

Large-signal measurements mostly refer to measurements conducted under operating conditions where the DUT is no longer behaving linearly. This work refers to high-power measurement since the power level extends into the kilowatt range. The demand for accurate high-power RF and microwave measurements is higher than ever and increasing with the increasing demand for high-power RF and microwave modules. Low uncertainty in high-power RF measurement is particularly important for the industries involved in high-power applications to ensure repeatable, accurate measurements [71]. An example of a high-power RF testbench is shown in Figure 2.9. Such a high-power RF test bench typically consists of signal generators and linear amplifiers to achieve the required power; couplers and splitters to separate the signals and a measurement receiver in the form of a power meter and oscilloscope. It is necessary to deliver test signals with low distortion at the measured power level and over the full frequency range. The high-power RF measurement system differs fundamentally from the small-signal measurement in many aspects:

- It covers high power ranges that require instruments with high voltage and/or high current handling capabilities, so this is a human safety issue.
- The signals are captured in the time-domain using oscilloscopes because they capture the full spectrum and are financially favorable.
- Considerable heat is generated during the measurement process, which must be taken into account when cooling DUT and dummy loads, etc.

### 2.2.1 RF Pulse *vs*. CW Measurement

The incident signal in high-power measurement is usually RF pulsed or continuous waves (CW). The high-power test bench shown in Figure 2.9 can support both RF pulse and CW measurement. The pulsed RF signal in this work is not indicative of the pulse modulated signal of use in radio communications, which is beyond the scope of this thesis. In fact, the envelope of the pulsed RF signal is simply a square shape, which means that the pulse width is long enough to accommodate many periods of the RF signal. The typical pulse width is 3.5 ms for tens or hundreds of MHz tests. Therefore, the RF pulse test can well reflect the CW test albeit at lower average thermal conditions if other impacts are not considered.

In high-power ranges, the thermal budget is a major factor that in operation differs a lot between pulse and CW operation. The thermal resistance has a

temperature dependence and therefore to some extent depends on pulse width and duty cycle which affects the operating temperature but mainly the thermal resistance depends on device size, technology, and packaging technology. The bigger the device and the cooling surface, the lower the thermal resistance. Thermal performance directly affects the reliability quantified in the MTTF (Mean Time To Failure). For a kilowatt transistor, it is around 0.1 K/W for LDMOS [72] as well as GaN on SiC [73].

Assuming a high-power transistor or module in high efficiency mode with 90% efficiency and 1 kW output power, the dissipated power would be about 100 W resulting in a maximum temperature rise of $10°C$ with limited impact on RF performance, but reduced efficiency can fast lead to temperature problems. In pulsed operation, the average dissipated power is reduced, but for longer duty clycle, the channel temperature can rise to CW depending on the thermal time constant defined by the thermal capacitance. A 3.5 ms pulse for transistor therefore fully reflects the expected CW performance. An example between RF pulse and CW measurement can be found in Section 4.3 later. In summary, many high-power applications work in CW mode, but the RF pulse test is good protection for the instruments while reducing the rigorous power requirements of every component involved.

### 2.2.2 High-Power Measurement Set-Up

The most concerning specifications in kilowatts high-power applications are output power $P_{out}$, gain $G_p$, drain efficiency $\eta_D$, etc. $\eta_D$ cannot be measured directly, it would be post-processed after DC power is resolved as indicated in (1.4), while DC current is detected from the current sensor when in pulse or CW mode, but can only be read from DC supplier in CW mode. An oscilloscope is used to capture the DC current waveform in pulse mode to seize the DC component of drain current $i_{DS}(t)$.

As can be seen, all measurements involved are scalar. A power meter is applied to measure the input and output power. Meanwhile, to access the harmonic components, an oscilloscope with four channels (CH1, CH2, CH3, and CH4 in Figure 2.9) is used to view the input/output waveform in the time domain. The collected waveform data with its harmonic components can be analyzed by using an FFT (Fast Fourier Transform) algorithm. Naturally, it can also be replaced by a spectrum analyzer that handles the frequency response and can check the harmonics level directly.

The highest measured power levels, e.g., +60 dBm (1 kW), cannot be measured directly with the power meter or oscilloscope, since the maximum input power level is only +23 dBm, therefore couplers or attenuators, e.g., 40 dB kilowatts couplers as in Figure 2.9, are required to reduce the power for power meters to a tolerable level.

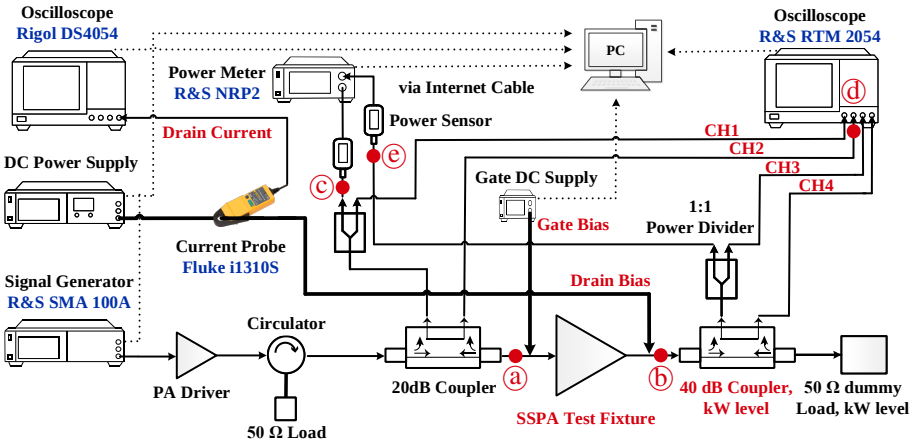



*Figure 2.9. High power measurement setup.*

When all necessary instrumentation is in place as in the final measurement setup depicted in Figure 2.9. A calibration methodology must be developed to shift the reference plane for the measurements to the RF module.

### 2.2.3 High-Power Calibration

Although it is suggested to calibrate the environment to the power level to be measured, this is unrealistic as achieving such high power is a problem with a signal generator even with a kilowatt range power driver. Normally it is set to +20 dBm since the maximum input power for the power meter is +23 dBm, but an alternative is to use an attenuator in front of the benchmark power meter, but it requires that the attenuator is known. All of these components (e.g., coupler, splitter, etc.) are supposed to have limited variations in different power ranges. Thus the calibration is linear since all the elements involved are linear passive components. When the power measurement setup is ready, the calibration procedure can be performed as follows, where the nodes ⓐ, ⓑ, ⓒ, ⓓ and ⓔ are stated in Figure 2.9.

*Power calibration procedure:*

1. Input power $P_{in}$ correction: As seen in Figure 2.9, node ⓐ first connects to the *benchmark power meter* to correct the input power at node ⓒ. Then a list of power values versus frequency with frequency sweep is obtained.
2. Reflect power $P_{ref}$ correction: Node ⓐ connect to a *Short* standard, then node ⓒ and node ⓓ get the same power since full reflection, using the corrected power at node ⓒ to correct the reflect power at ⓓ. Likewise, a frequency sweep list is obtained after this step.
3. Output power $P_{out}$ correction: Node ⓐ connects to note ⓑ with a *Thru* standard, then node ⓒ and node ⓔ get the same power since standard Thru

is supposed to have no loss. Using the corrected power at node ⓔ to correct the output power at ⓔ. A frequency sweep list is also obtained.

Then, after the calibration procedure, the reference plane at node ⓒ, ⓓ and ⓔ is shifted to the direct measurement plane at node ⓐ and ⓑ.

### 2.2.4 MATLAB based Automatic Measurement

For a small amount of measurement, testing power and a frequency point, manual testing and manual recording are possible, but for large amounts of data, such as power sweeping, frequency sweeping, or module tuning, such cases are very time-consuming and prone to recording errors manually. Therefore, automatic measurement is necessary. Additionally, the control platform for automatic measurement can process the data instantly, such as the indirect efficiency $\eta_D$ can be determined immediately, and make it more visible with graphics and/or tables. A MATLAB-based automatic measurement system is built and shown in Figure 2.9, while other written languages, such as Python and LabVIEW, are also good platforms to perform the automatic measurement. The connection or communication between instruments and PC can be via GPIB (General Purpose Interface Bus), USB, LAN, etc. interface. The control codes are written based on the instrument manual, but the control methodology for the instruments themselves and the instrument sequences should be developed, and here two cases concern RF pulses and CW tests, which play a very important role in automatic measurement, for example, are specified in Appendix B.

## 2.3 Chapter Summary

This chapter concerns the RF measurements from small-signal to large-signal. It proposes a new thru-only de-embedding technique applied to symmetrically tapered transmission lines, and a detailed theoretical analysis is provided. Moreover, a high-power measurement test bench is established for pulsed and CW measurements. It supports the high-power measurement of SSPA modules described in Chapter 3 and Chapter 4. Automatic measurement is also established for rapid measurement and data processing.

# 3. Efficient *Multimode* Power Amplifier Module

The term *multimode* was introduced in [74] to account for the combination of modes of operation typically present in real amplifier implementations. This mode of operation is defined by a combination of fundamental and harmonic terminations that generate certain voltage and current waveforms at the intrinsic current generator plane [75, 76], the corresponding voltage and current waveforms are often designed to generate minimized overlap between them to achieve low losses in the transistor which thereby operate at high efficiency. This includes the well-known class-F with a square-waved voltage and sinusoidal current established through short-circuited even harmonics and high impedance odd harmonics and its complementary class-$F^{-1}$ with square-wave current and sinusoidal voltage established through short-circuited odd harmonics and high impedance even harmonics. Other high-efficiency waveforms like class-J include non-resistive fundamental impedances with an intrinsic non 180° phase shift between the current and voltage [77]. This graphic representation of specific voltage and current waveforms over time is referred to as waveform engineering, which is useful in analyzing SSPA performance. This chapter presents a *multimode* PA that can be seen as a mix of class-J and class-$F^{-1}$, it incorporates efficiency improvements both in full power and back-off power regions with quasi-static supply modulation.

## 3.1 High Efficiency PA Operation Mode: *Multimode*

In this section, given the boundary conditions of the device size and package, three typologies are examined as a comparative study from ideal conditions to more real-world conditions that take into account the knee effect. Their simulated RF performance will be demonstrated to show the pros and cons of these operation modes.

### 3.1.1 Comparative Study Based on Waveform Engineering Technique

To simplify the waveform study derivation process for Class-J and Class-$F^{-1}$, a Class-B bias is applied to all case analyses in the following. The multimode is then proposed based on the waveforms of Class-J and Class-$F^{-1}$ modes.

**Basic Principles for Class-F$^{-1}$**

The ideal Class-F$^{-1}$ assumes open-ended even harmonics and short-circuited odd harmonics that produce nearly a square-wave current waveform and a sinusoidal voltage waveform at the intrinsic reference plane, i.e., the current generator plane (I-gen Plane) of transistor. This intrinsically enables good zero voltage crossing with very low transistor losses. The square-wave current has a large fundamental current component that produces high output power in the load.

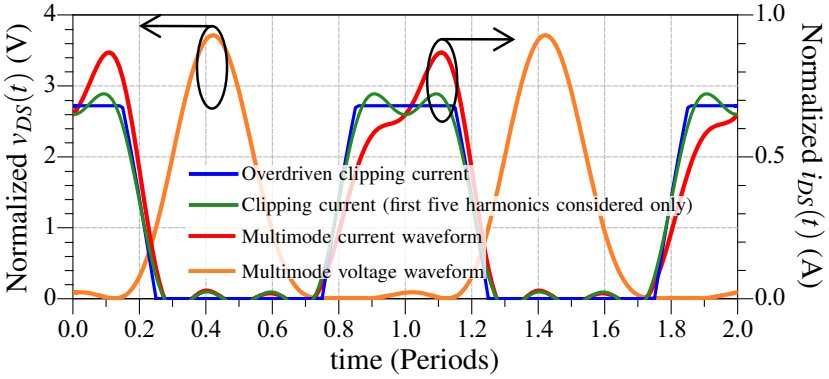



*Figure 3.1. Normalized $v_{DS}(t)$ and $i_{DS}(t)$ for the identification of the waveform formula for the multimode operation. Note: $v_{DS}(t)$ is normalized to the DC bias supply $V_{DD}$, while $i_{DS}(t)$ is normalized to the maximum drain current $I_{max}$.*

Under overdrive conditions, the transistor generates a clipped half-cosine wave, shown as the blue curve in Figure 3.1. With proper adjustment, the voltage can be allowed to dip into the knee region, thus the clipping current such that becomes an approximation of a square wave [74]. On the other hand, the reduced current cannot reach the maximum drain current $I_{max}$ due to the low voltage at that moment near the knee voltage ($V_{knee}$) region. When processed with the Fourier transform and only the first five harmonics are considered, it will generate the waveform as the green curve shown in Figure 3.1, which is exactly the current waveform of Class-F$^{-1}$, where the corresponding expression is given by

$$\begin{aligned} i_{DS}(t) = & I_{max} \cdot [0.274 + 0.406\cos(\omega t) + 0.117\cos(2\omega t) \\ & - 0.075\cos(3\omega t) - 0.077\cos(4\omega t) \\ & + 0.003\cos(5\omega t) + \cdots] \end{aligned} \tag{3.1}$$

Meanwhile, to maximize the fundamental component of the drain voltage $v_{DS}(t)$, the voltage waveform shown as the red curve in Figure 3.2 is defined as:

$$v_{DS}(t) = V_{DD} \cdot \left[1 - \sqrt{2}\cos(\omega t) + 0.5\cos(2\omega t)\right] \tag{3.2}$$

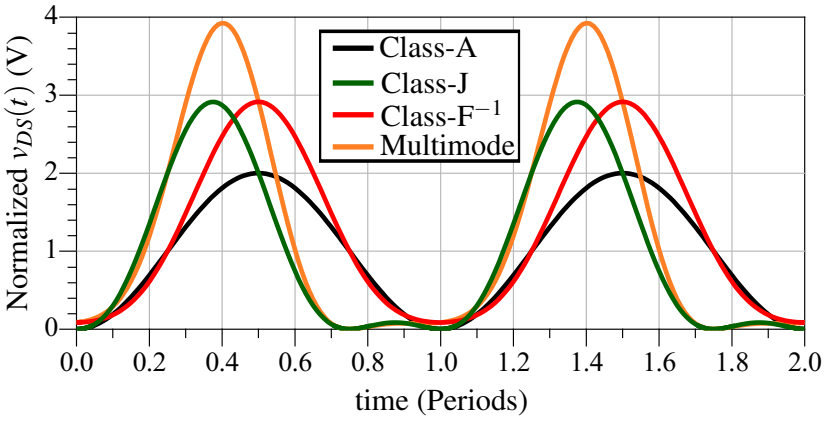



*Figure 3.2. Normalized $v_{DS}(t)$ for different PA configurations.*

This mode shows a higher fundamental voltage, which means a higher output power is delivered, meanwhile, a higher peak voltage $V_{pk}$ is generated. A high $V_{pk}$ requires a high breakdown voltage of the transistor, which contributes to the ruggedness or reliability attributes of the circuit design.

**Basic Principles for Class-J**

Class-J is a mode of operation where it is not assumed that the current and voltage are 180° out of phase over the transistor at the I-gen plane. Instead of a purely resistive load, the fundamental matching is deliberately targeting a considerable reactive part. In combination with a reactive second-order harmonic loading, it is possible to generate a number of equally highly efficient modes of operation [78, 79, 80, 81]. This has predominantly been investigated for wide-band applications, the so-called *continuous mode* amplifiers where the efficiency is high over a large frequency range and the mode of operation continuously shifts with frequency from one efficient mode to another. The investigation normally includes only non-saturated operations where the waveform is not reaching into the knee region.

The voltage waveform of Class-J is shown as the green curve in Figure 3.2, and its expression is given as

$$v_{DS}(t) = V_{DD} \cdot [1 - \cos(\omega t)] \cdot [1 + \sin(\omega t)] \tag{3.3}$$

While its half-wave rectified cosine current waveform is derived after using Fourier transform as follows:

$$\begin{aligned} i_{DS}(t) = & I_{max} \cdot [0.318 + 0.5\cos(\omega t) + 0.212\cos(2\omega t) \\ & - 0.0\cos(3\omega t) - 0.042\cos(4\omega t) \\ & + 0.0\cos(5\omega t) + \cdots] \end{aligned} \tag{3.4}$$

Because the second harmonic components of $v_{DS}(t)$ are in quadrature with the cosine current, they do not contribute to the power. Therefore, such modes show the same efficiency as class-B PA, but the harmonic voltage components imply that the transistor is not terminated with a Short at each harmonic, and in this case, the harmonic terminations are fully reactive.

**Investigation of *Multimode***
Allowing reactive fundamental matching and saturated mode of operation suggests an option to find some mixed-mode where the efficiency under the given boundary conditions can be even higher.

The target multimode voltage waveform is shown as the orange curve in Figure 3.1, which adds a reactive part as Class-J based on Class-F$^{-1}$ voltage, i.e., mixing (3.2) and (3.3), it gives as

$$v_{DS}(t) = V_{DD} \cdot \left[1 - \sqrt{2}\cos(\omega t) + 0.5\cos(2\omega t)\right] \cdot [1 + \sin(\omega t)] \tag{3.5}$$

Furthermore, continues with the Class-F$^{-1}$ current shown in Figure 3.1, i.e., equation (3.1), but with an additional reactive part, the multimode current waveform becomes

$$\begin{aligned} i_{DS}(t) = & I_{max} \cdot [0.274 + 0.406\cos(\omega t) + 0.117\cos(2\omega t) \\ & - 0.075\cos(3\omega t) - 0.077\cos(4\omega t) \\ & + 0.003\cos(5\omega t) + \cdots] \cdot [1 + 0.34\sin(\omega t)] \end{aligned} \tag{3.6}$$

The corresponding curve is shown in red in Figure 3.1, the waveform curves or formulas of this mode show the difference from other known PA configurations. In addition, the number "0.34" on the reactive part in (3.6) is calculated from the minimized power of the second harmonic.

Moreover, when the voltage and current waveforms are determined, their corresponding impedance at each harmonic component can be derived by:

$$Z_{nf_0} = -\frac{V_{ds,n}}{I_{ds,n}} \tag{3.7}$$

where $V_{ds,n}$ and $I_{ds,n}$ indicates the $n\ th$ harmonic component from $v_D(t)$ and $i_D(t)$ separately after processing by Fourier transformation.

### 3.1.2 RF Performance Trade-Offs

When comparing different PA configurations, one of the most important concepts is the so-called power utilization factor (PUF) [19, 82]. This term is basically the ratio of the RF power delivered in a given considered mode to the power it would deliver as a simple Class-A.

According to Figure 3.2, based on the Class-A mode, a comprehensive summary shows the $V_{pk}$ and fundamental component as follows:

- Class-F$^{-1}$ achieves the fundamental amplitude of factor $\sqrt{2}$ as Class-A, and $V_{pk}$ reaches a factor of $(1.5+\sqrt{2})/2$ of Class-A.
- Class-J shows the same fundamental amplitude as Class-A, but $V_{pk}$ also reaches a factor of $(1.5+\sqrt{2})/2$ of Class-A.
- Multimode achieves the fundamental amplitude of factor $\sqrt{2}$ of Class-A, but $V_{pk}$ reaches a high factor of $(2.5+\sqrt{2})/2$ as Class-A.

Thus, the PUF is 0.971, 0.686, and 0.723 for Class-F$^{-1}$, Class-J and Multimode respectively when the current is considered the same for these three modes. In practice, however, due to the knee effect, a current reduction must take place for all three modes. Additionally, from the ideal waveform formulas derived in Section 3.1.1, Class-F$^{-1}$ and multimode can achieve high efficiency of more than 90%, and Class-J achieves the same 78.5% efficiency as Class-B. So, from the waveform formulas, it can be concluded that Class-F$^{-1}$ has the best efficiency and delivered power, class-J has the lowest efficiency and poor delivered power, and multimode has good efficiency but poor delivered power. However, it does not take the current reduction into consideration, to make it more suitable for the real-world case, a more practical mathematical model [19] to account for the knee effect is included and is given as

$$i_{DS}(t) = v_g \cdot g_m \cdot I_{\max}\left(1 - e^{-\left(\frac{v_{DS}(t)}{V_{knee}}\right)}\right) \tag{3.8}$$

where $v_g$ is the input gate voltage, $g_m$ is the transconductance. Equation (3.8) shows the modified ideal transistor I-V characteristics, which include a realistic turn-on region. And the knee voltage $V_{knee}$ is normalized to the DC bias supply $V_{DD}$.

To calculate the response of the nonlinear formula (3.8), the harmonic balance (HB) method is applied to calculate the steady-state from a chosen number of harmonics in the frequency domain [83]. Finally, the calculated load impedance from (3.7) as well as its RF performance are presented in Table 3.1. Where $R_{opt} = (V_{DD} - V_{knee})/I_{max}$.

According to Table 3.1, the fundamental impedance of *multimode* shows a mixture of Class-F$^{-1}$ and Class-J, and *multimode* also shows the best efficiency but with the aforementioned sacrifice in output power. This is consistent with the analysis of the ideal waveform mentioned above. Moreover, the key requirement emphasized by Class-F$^{-1}$ is short circuit termination at odd harmonics and an open circuit at even harmonics, which poses the greatest challenge in the circuit design. While since no demands on open-circuit impedance termination at harmonics as Class-F$^{-1}$, Class-J and *multimode* significantly increase matching network design flexibility.

**Table 3.1.** *Summary of Class-F$^{-1}$, Class-J, Multimode RF performance using the harmonic-balance method.*

| Specification | | Operation Mode | | |
|---|---|---|---|---|
| | | Class-F$^{-1}$ | Class-J | Multimode |
| $Z_{nf_0} = \begin{cases} Z_{f_0} \cdot R_{opt}\ (\Omega) \\ Z_{2f_0} \cdot R_{opt}\ (\Omega) \\ Z_{3f_0} \cdot R_{opt}\ (\Omega) \end{cases}$ | $Z_{f_0}$ | $3.29 + j0$ | $2.0 + j2.0$ | $3.1 + j2.4$ |
| | $Z_{2f_0}$ | $Inf$ [*] $+ jInf$ | $0 - j2.36$ | $0 - j6.0$ |
| | $Z_{3f_0}$ | $(0 + j0)^*$ | $(0 + j0)^*$ | $0 - j2.8$ |
| Efficiency,$\eta_D$ (%) | | **90** | 78 | **91** |
| Output Power (dBm) | | $P_o$ [‡] | $P_o - 0.3$ | $P_o - 1$ |
| Matching complexity | | Hard | **Easy** | **Easy** |

[*] "*Inf*" means infinity large impedance here, i.e, open circuit. While $(0 + j0)$ represents "short circuit".

[‡] $P_o$ represents the output power for Class-F$^{-1}$ as a benchmark for other modes.

## 3.2 Practical Design of *Multimode* PA Module

In order to examine the multimode theory and analysis, a practical design presented in **Paper III** evaluates the waveform at I-gen plane of transistor based on a large-signal model, as well as the RF performance both in the full-power and back-off power region.

Even though this work is a VHF band application, the nonlinear relatively large output capacitance $C_{OSS}$ of high power LDMOS devices limits options, and poor packaging can also prevent the possibility of tuning the higher order harmonics. Therefore, a non-pre-matched or unmatched device is a good option as the jumper wire inductance and package capacitance have a limited effect on harmonic tuning.

### 3.2.1 Large-Signal Model Based Topology Evaluation

The manufacturer provides a large-signal model for the robust transistor with intrinsic ports to monitor waveforms at I-gen plane. These intrinsic ports are used to verify alternative highly efficient waveforms that also take the knee region into consideration.

**Matching Impedance Selection**

In this work, the transistor is specified to deliver a typical output power of 60 dBm. From the manufacturer's datasheet, the DC bias $V_{DD}$ is selected at 45 V, and the maximum current $I_{max}$ is around 20 A, $V_{knee}$ is around 5 V, then $R_{opt}$ gets about 2 Ω from the formula $R_{opt} = (V_{DD} - V_{knee})/I_{max}$. Taking the $R_{opt}$ into Table 3.1 to get the initial design values for load impedances.

**Schematic Setup and RF Simulation**

Due to the practical high-power transistor model being dynamic and nonlinear, the load impedance (at I-gen plane) calculated above can only be adjusted from the package plane, but the impedance at I-gen plane is visible

thanks to the intrinsic current and voltage waveform is monitored. After impedance tuning at the package plane and considering practical conditions, the final load impedance at I-gen plane is listed in Table 3.2 for the three topologies considered above, i.e., Class-F$^{-1}$, Class-J, and multimode.

**Table 3.2.** *Intrinsic impedances and corresponding RF performance for the three investigated topologies. The three modes have the same bias status, i.e., $V_{DD} = 45\,V$, $I_{DQ} = 100\,mA$.*

| Specification | | Operation Mode | | |
|---|---|---|---|---|
| | | Class-F$^{-1}$ | Class-J | Multimode |
| $Z_{nf_0}$@ I-gen plane | $Z_{f_0}$ ($\Omega$) | $6.6+j0.1$ | $4.0+j4.0$ | $6.6+j4.0$ |
| | $Z_{2f_0}$ ($\Omega$) | $165-j75$ | $0.3-j4.3$ | $0.2-j11.5$ |
| | $Z_{3f_0}$ ($\Omega$) | $0.2+j0.2$ | $0.0-j1.6$ | $0.1-j4.3$ |
| $G_p$ (dB) | | 19.1 | 19.5 | 21.4 |
| *PAE* (%) | | 87.5 | 79.5 | 91 |
| $P_{out}$ (W) | | 1150 | 1020 | 970 |

As can be observed in Table 3.2, the Open circuit termination at the second harmonic for Class-F$^{-1}$ cannot be set infinitely high as the theoretical definition. Practically, it can only be reached in a relatively high impedance range and is found to be very sensitive and difficult to achieve. Because of this, it can be said that the design for this mode is very demanding due to the complexity of the required harmonic matching network.

Moreover, according to Table 3.2, the impedance at I-gen plane as well as the RF performance in accordance with the theoretical analysis in Section 3.1, the simulated efficiency in multimode operation can be as high as 90% at the kilowatts level. Compared to class-F$^{-1}$ the multimode simulations show a substantial reduction by 15% in maximum output power. However, the PAE is about 4%-points better over the saturation range and the required impedances are higher which implies less transformation losses and an easier matching network design.

### 3.2.2 Output Power Back-Off Considerations

As mentioned in Section 1.3.2, the solid-state transistor has the important advantage that it can work well at various output power levels compared to the classic vacuum tube technology, but its efficiency is reduced considerably in the lower power region compared to the saturated power region. Improving efficiency at back-off power is also an important specification as more and more applications operate at different power levels.

In general, load modulation and bias modulation are the two main efficiency enhancement technologies to improve the back-off power efficiency, which were already introduced in Chapter 1. The work in this section focuses on

**Table 3.3.** *Intrinsic impedances and corresponding RF performance for multimode at various supply voltages.*

| $V_{DD}$ (V) | Impedance @ I-gen Plane (Ω) | | | $P_{out}$ (W) | PAE (%) | $G_p$ (dB) |
|---|---|---|---|---|---|---|
| | $Z_{f0}$ | $Z_{2f0}$ | $Z_{3f0}$ | | | |
| 50 | 6.5 + j4.0 | 0.3 - j11.5 | 0.1 - j4.4 | 1200 | 89.5 | 21.8 |
| 45 | 6.6 + j4.0 | 0.2 - j11.5 | 0.1 - j4.3 | 970 | 91 | 21.4 |
| 40 | 6.7 + j4.0 | 0.1 - j11.5 | 0.1 - j4.3 | 760 | 91.5 | 21.3 |
| 35 | 6.8 + j3.9 | 0.1 - j11.3 | 0.1 - j4.2 | 580 | 92 | 20.6 |
| 30 | 6.9 + j3.8 | 0.1 - j11.0 | 0.1 - j4.0 | 420 | 92 | 20.2 |
| 25 | 7.1 + j3.6 | 0.1 - j10.6 | 0.0 - j3.6 | 285 | 91.5 | 19.6 |
| 20 | 7.4 + j3.3 | 0.1 - j10.0 | 0.0 - j3.2 | 175 | 90.8 | 18.5 |
| 15 | 7.9 + j2.9 | 0.1 - j9.2 | 0.0 - j2.7 | 90 | 89.5 | 17.2 |

bias modulation. In particular, since the RF power source application in radioisotope production has no modulation speed requirements, for simplicity and cost consideration, quasi-static bias modulation or various supply control technology is adopted to improve the back-off efficiency.

In order to show the full potential of quasi-static supply modulation, it is crucial to obtain the RF performance at different various voltages first. Therefore, harmonic load-pull simulations at various supply voltages using the large-signal model yield the achievable impedance conditions from 15 V to 50 V supply for multimode operation, which is shown in Table 3.3 together with their RF responses. The impedances at the package plane for the transistor used are fixed at $Z_{f_0} = (1.6 + j2.2)\ \Omega$, $Z_{2f_0} = (0.6 + j11.6)\ \Omega$, $Z_{3f_0} = (0.2 - j22.8)\ \Omega$. The obtained impedances show a much higher real-part at the fundamental intrinsically and in addition large $2^{nd}$ and $3^{rd}$ harmonic reactive parts. These are achieved by much higher reactive impedances in general at the package plane. And it can be observed that even for the fixed impedance at the package plane, the intrinsic impedance remains constant above the 40 V bias supply while changes occur in the lower bias ranges. This was caused by the nonlinear voltage-dependent $C_{ds}$, as $C_{ds}$ flattens in the high voltage range but rises sharply in the low voltage range. The intrinsic dynamic load-lines and the time-domain waveforms are shown in Figure 3.3. For more details on simulated high-power RF performance and waveforms for Class J and Class $F^{-1}$ topologies, see Tables I and II, Figures 2 and 3 respectively in **Paper III**.

As can be seen from the intrinsic waveforms, the current-voltage overlap is extremely reduced, resulting in very high peak PAE values in excess of 90%. The drain peak voltage $V_{pk}$ is more than 160 V at 50 V drain bias, which is already above the breakdown voltage at 135 V. Therefore the PA should not be operated with 50 V bias. The very high PAE is maintained even for a lower supply voltage, and it can be observed from the dynamic load-line that the reduced supply voltage pushes the waveform further into the low-

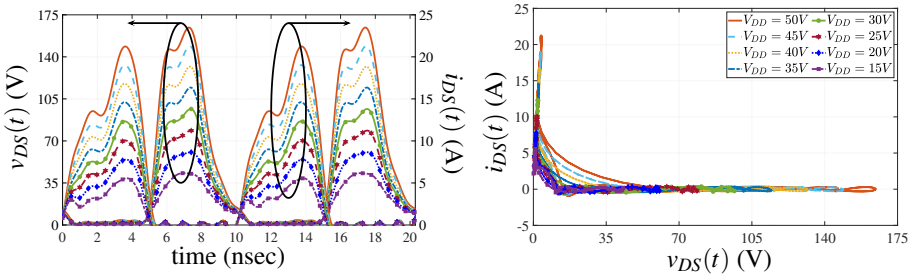



*Figure 3.3. (a) Time-domain waveforms and (b) their corresponding dynamic load-lines at the intrinsic current generator plane for the multimode topology. The legends in (b) are also valid for (a).*

loss leftmost lower corner of the output characteristic leading to even higher back-off efficiency. This multimode shows great potential for highly efficient operation under various output power conditions even though the maximum output power is decreased.

### 3.2.3 Matching Circuit Design

The selected high-power transistor is a pre-matched dual-chip device. In the single-ended configuration, the identical chips are directly connected to each other at the package plane. To implement the proposed multimode PA, the simulated impedances at 45 V bias in Table 3.3 are chosen as a start point for the matching network design. Where the bond wire jumper inductor $L_j$ and the parasitic package capacitor $C_{pkg}$ are already considered, and the drain-source capacitance $C_{ds}$ of the semiconductor also includes the voltage dependency of $C_{oss}$ normally attributed to the gate-drain capacitance $C_{gd}$ part of $C_{oss}$ as explained in Section 1.2.1.

Since the two chips with identical performance are connected in parallel in the single-ended structure, the desired impedance for the output matching network (OMN) at the package plane with two chips combined is half of the value for a single chip, i.e., $Z_{f_0} = (0.8 + j1.1)\ \Omega$, $Z_{2f_0} = (0.3 + j5.8)\ \Omega$, $Z_{3f_0} = (0.1 - j11.4)\ \Omega$.

Given it's a VHF band application, the solution is implemented with a combination of lumped components and low impedance distributed transmission line (TL) elements to achieve a compact design, making it possible to bundle with other modules in a small form-factor.

Finally, a three-stage matching network based on ideal components shown in Figure 3.4 is proposed, its corresponding fundamental and harmonic impedance trajectories are depicted in Figure 3.5. The small capacitances close to the transistor enable large tuning of the harmonics. The $3^{rd}$ harmonic response is much influenced by the C3 capacitor, which transforms the trajectory all the

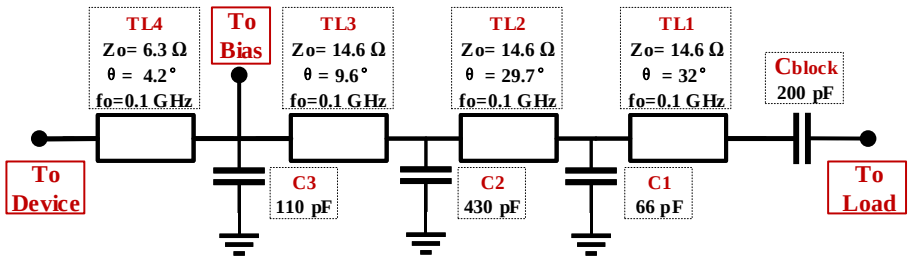



*Figure 3.4. Matching network with ideal components.*

way around to the negative phase range. And the C2 capacitor has the same function for the $2^{nd}$ harmonic with the trajectory depicted in green. They provide a certain tuning possibility for the $2^{nd}$ and $3^{rd}$ harmonics. Drain supply is provided over an inductor that effectively separates the RF from the DC path.

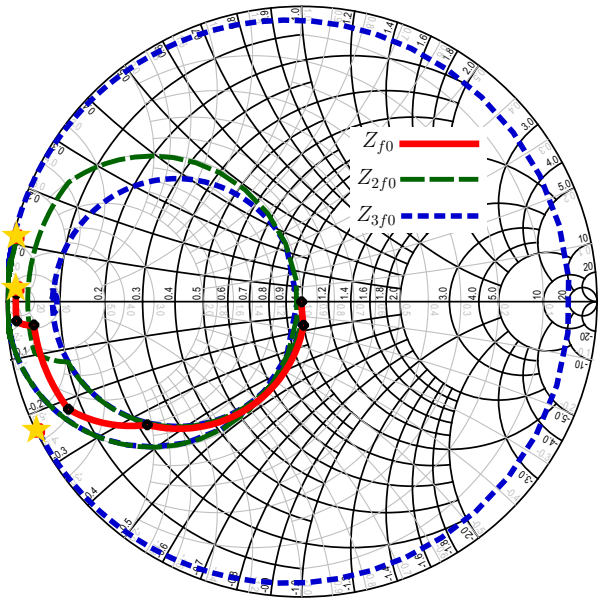



*Figure 3.5. Fundamental and harmonic impedance trajectories for OMN in Figure 3.4. The star symbol means the matching target.*

At the input, the implementation was conducted in a similar manner with low impedance transmission lines and lumped capacitors but only the fundamental impedance $Z_s = (0.8 - j2.2)\ \Omega$ was considered. A resistor was used for RF isolation and LF stability on the DC feed. Then practical circuit implementation was made on a low loss substrate, the Rogers' TMM10i [84] ($\varepsilon_R$ = 9.8, tan($\delta$)= 0.002, 35 $\mu$m copper thickness).

The ideal components were first replaced by real values and the matching networks were transferred to a realizable design using meander lines to reduce

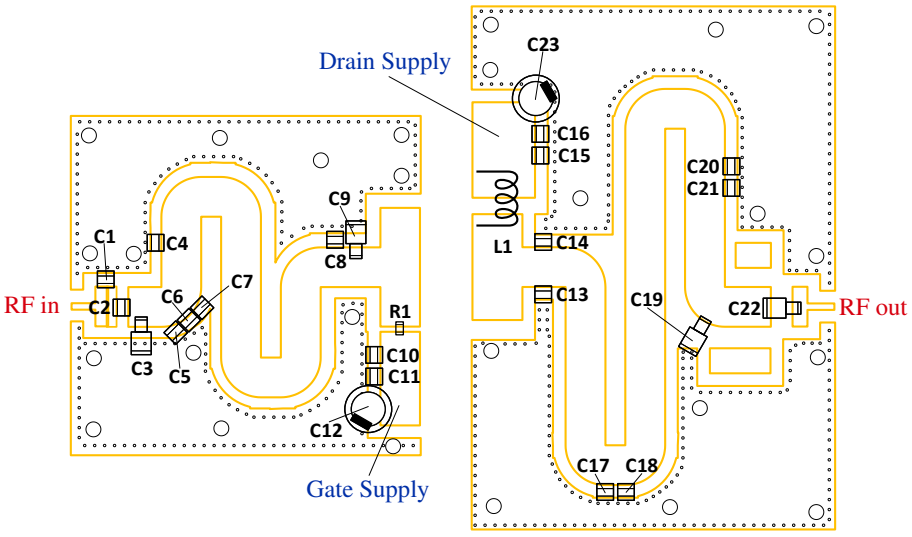



*Figure 3.6. Finalized matching network layout with components.*

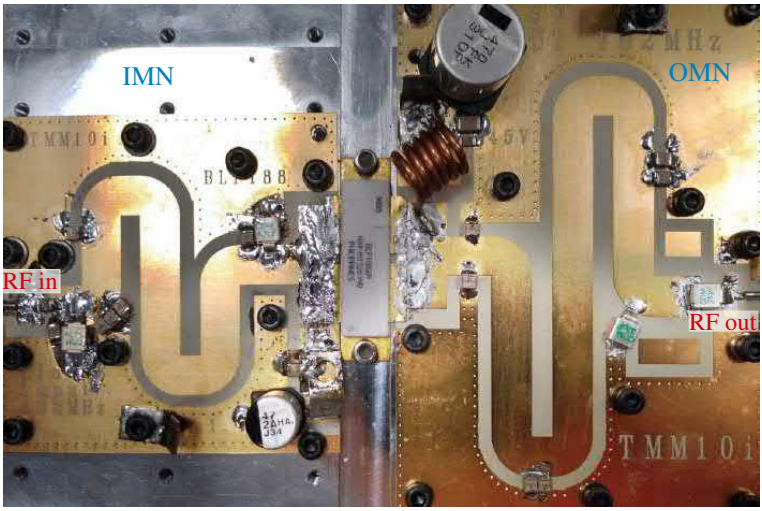



*Figure 3.7. Photograph of the fabricated SSPA.*

the board size. Co-simulations with the RF momentum method verified PCB layouts and lumped component models from the vendors were evaluated and optimized to ensure matching close to the required impedances. The finalized layout is presented in Figure 3.6, where C13 and C14 correspond to the $3^{rd}$ harmonic tuning capacitor (C3 in Figure 3.4) and C17 and C18 correspond to the $2^{nd}$ harmonic tuning capacitor (C2 in Figure 3.4). To slightly move them along the meander microstrip line or replace them with another slightly

different value enable tuning for targeted RF performance. The photograph of the fabricated tuned circuit is shown in Figure 3.7.

### 3.2.4 Load Mismatch Exploration

The waveform investigations in the co-simulation assume matched output conditions, i.e., the uniform system impedance is 50 Ω. Given the high-power application, the amplifiers may not be equipped with isolators and could be exposed to weak mismatch conditions that may affect the RF performance. To explore the impact of low mismatch load conditions, loads with an equivalent return loss of 20 dB (VSWR 1.22:1) and 15 dB (VSWR 1.43:1) were simulated and their respective mapped intrinsic load impedances are depicted in Figure 3.8. As can be seen, the transformation map is limited to a very small area at the intrinsic plane for the transistor.

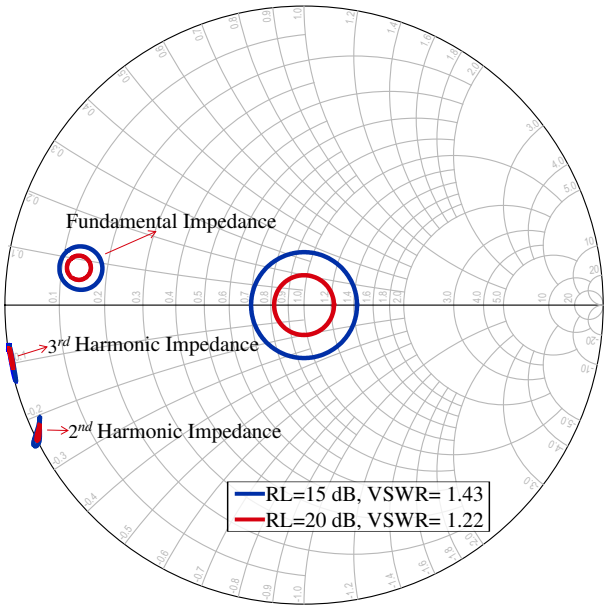



*Figure 3.8. PA module load mismatch of 15 dB and 20 dB and their respective intrinsic impedance transformation for the fundamental, $2^{nd}$ and $3^{rd}$ harmonic through the package and output matching network.*

The RF performance variation from mismatch is shown in Figure 3.9 where the output power $P_{out}$, efficiency $\eta_D$, power gain $G_p$, and the peak drain voltage $V_{pk}$ are plotted versus the phase of the load impedance.

According to the co-simulation, it shows that $P_{out}$ of the multimode solution may vary ±20% and an efficiency drop by 3%-points depending on the phase of the reflection for a low VSWR mismatch of 1.22:1, i.e., 20 dB return loss.

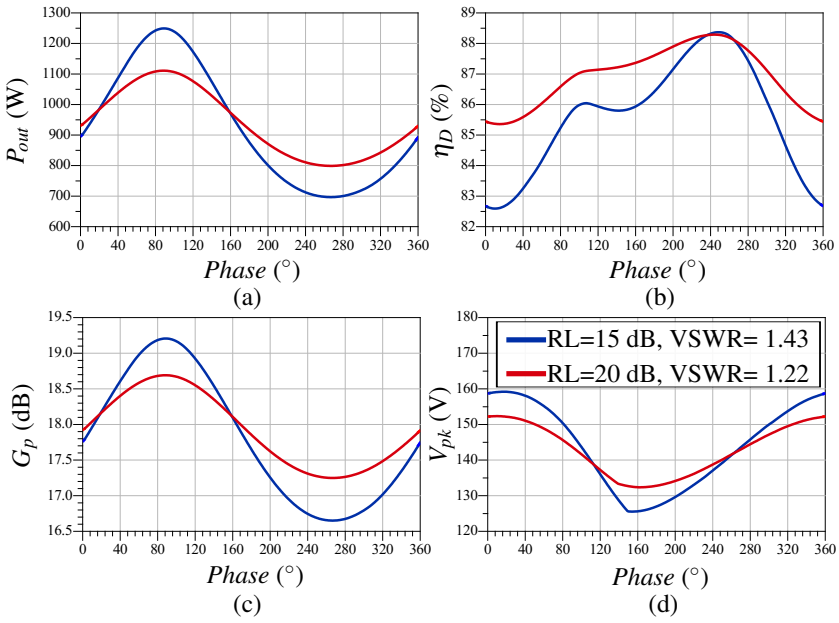



*Figure 3.9. PA module load mismatch of 15 dB and 20 dB and their respective impact on (a) output power $P_{out}$, (b) efficiency $\eta_D$, (c) power gain $G_p$, and dynamic peak drain voltage $V_{pk}$.*

The mismatch can also lead to $V_{pk}$ exceeding the breakdown voltage by a maximum of 10%.

## 3.3 RF and Thermal Performance Evaluation

For high-power amplifiers, thermal management, i.e., handling the generated heat in the operating device, is critical since RF performance is highly impacted by temperature. A heat-conducting compound between transistor and cooling plate creates excellent thermal contact with the cooling plate. During the measurements, a water cooling system with a water flow rate of 8 L/min is operated to cool down the heatsink plate. The assembled SSPA can be seen in Figure 3.7, where the aluminum heatsink plate located below the transistor, has a void with continuous flow of cold water. The heatsink is used for cooling purposes, but also to fix the circuit board. The measurement methodology is presented in Chapter 2, and the associated RF measurement bench for high-power test is shown in Figure 2.9.

**High-Power RF Measurement**

The RF measurement bias was conducted in a class-AB quiescent point with $I_{DQ}$ = 200 mA, $V_{DD}$ = 45 V and a pulsed RF signal with 3.5 ms pulse width

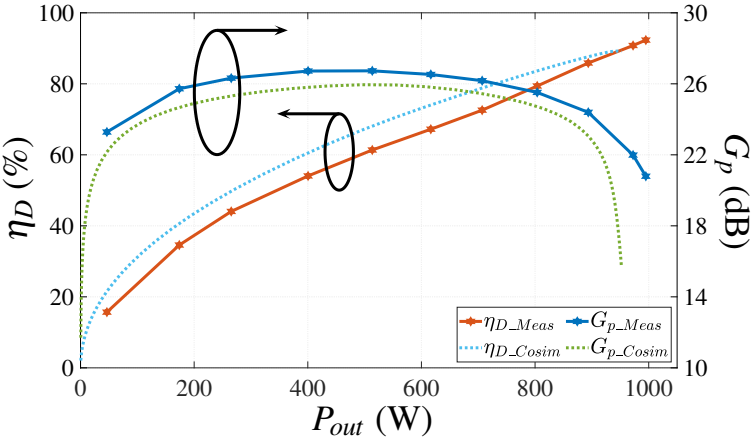



*Figure 3.10. Simulated and measured power sweep results.*

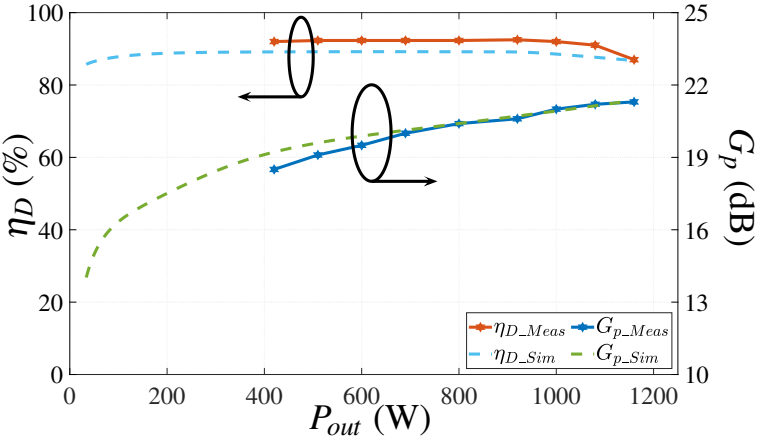



*Figure 3.11. Simulated and measured RF performance for the implemented SSPA at $I_{DQ}$ = 200 mA at 98.5 MHz. Output power back-off is evaluated using drain supply control. For simulation, $V_{DD}$ varies from 10 V to 50 V, while for measurement, $V_{DD}$ varies from 30 V to 50 V).*

and 70 ms pulse period. Hence, the duty cycle is 5%. Figure 3.10 depicts the simulated and measured results at 98.5 MHz with 45 V drain supply. The measurements show good consistency with simulations. A maximum measured drain efficiency at 93% at an output power of 980 W is obtained. The power gain $G_p$ is 21.5 dB, and the input matching is better than -12 dB.

**Output Power Variation**

The amplifier was evaluated in power back-off operation with reduced drain supply voltage. The measured results presented in Figure 3.11 show more

than 90% drain efficiency over a 5 dB power back-off range, and are also very consistent with the expected results from simulations.

Additionally, the application neither requires speed, nor high resolution in the power control. Therefore, the supply voltage can be controlled using a multitude of efficient power supplies operating at various voltages. In the future, a highly efficient power supply modulation with a limited number of output voltages could be implemented.

**Thermal Evaluation**

For this very efficient amplifier where the transistor shows very low power dissipation, it is important to identify other sources of power dissipation that might affect the overall efficiency. Very high power leads to high RF currents and fields that may exceed safe operating specifications for passive devices. For this purpose, a thermal image was taken with the amplifier operating under steady-state conditions. In steady-state conditions, the cooled SSPA was operated with an output power of around 1 kW for 20 minutes then the thermal image was recorded by using a FLIR ONE Pro IR camera. The picture shown in Figure 3.12 verifies that the cooling of the transistor is very efficient and keeps the transistor flange well below 30°$C$ when the SSPA delivers 1 kW output power in pulsed operation.

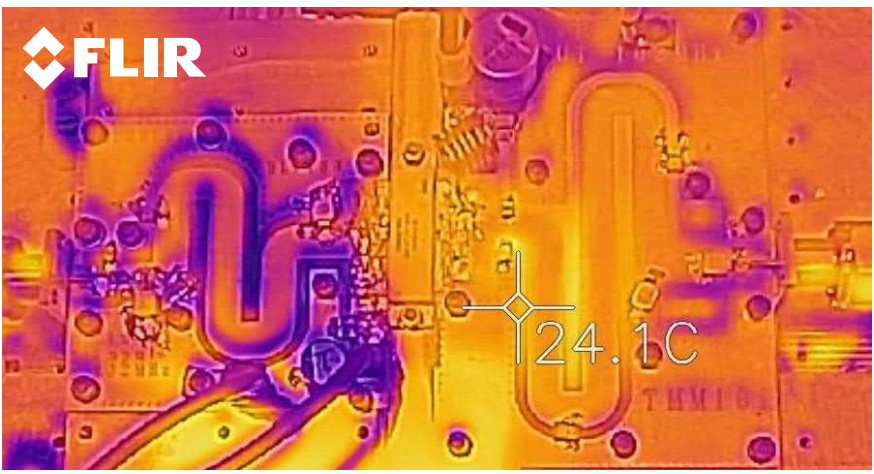



*Figure 3.12. Thermal image during RF measurements in pulsed mode with pulse width=3.5 ms and pulse period= 70 ms at 1.0 kW using water flow with 8 L/min.*

Moreover, the thermal resistance of LDMOS from junction to base is around 0.1 K/W. With the high efficiency of this PA module, the dissipated power even for CW mode would be below 100 W at kilowatt output power leading to a maximum temperature increase of 10°$C$ which would not have an effect on the RF performance of the transistor. Hence, the long 3.5 ms pulse fully reflects the expected CW performance.

## 3.4 Chapter Summary

This chapter demonstrated a kilowatt level solid-state amplifier module that is intended to be used in a power source for radioisotope production, where the power of multiple SSPA modules is to be combined. Waveform engineering has been conducted to compare three operation modes theoretically and identify the most efficient mode for this kilowatt design. Multimode operation with Class-J and Class-$F^{-1}$ properties is identified that this mode delivers an almost constant efficiency over a considerable power back-off using drain supply modulation. The realized SSPA module, based on the proposed multimode operation implemented in LDMOS technology, shows 93% peak drain efficiency with 980 W output power. It also shows around 90% drain efficiency over a 5 dB back-off power region, which is verified in operation employing variable drain supply control from 30 V to 50 V.

# 4. Efficient and Compact Push-Pull Power Amplifier Module

In the kilowatt SSPA module design, with a relatively low supply voltage in the several tens of volts range, the output current is high and thus the transistor output impedance is only a few ohms or even less. Hence, the output matching network requires a very large impedance transformation ratio to generate current into a 50 Ω load. The push-pull configuration is therefore well suited as it allows the input and output impedance of the transistors to be connected in series for RF operation, increasing the impedance by a factor of two. This chapter introduces the classic push-pull SSPA architecture at the kilowatt level. By using lumped LC balun and components to compact the overall design, and incorporating harmonic tuning in a lumped harmonic trap to improve the efficiency of entire SSPA modules. Meanwhile, back-off efficiency is improved by adopting quasi-static drain supply modulation or variable drain supply control technology used in Chapter 3.

## 4.1 Overview of Push-Pull PAs

When two separate but identical transistors are in Class-B operation but with 180° phase difference, if one of the transistors pushes the current to the output during the positive half cycle of the input signal, then the other transistor pulls the current to the output during the negative half cycle of the input signal. This is how this amplifier architecture has the name "Push-Pull".

Although often referred to as push-pull, the two transistors can be combined in a variety of configurations driven by external components such as 180° splitter/combiners, i.e., baluns, 3 dB quadrature couplers (e.g., branch-line or Lange couplers ), and in-phase couplers (e.g., Wilkinson couplers). Push-pull configurations are used extensively for high power for relatively narrow-band commercial applications. Additionally, the push-pull configuration also offers other advantages as follows:

- Lower impedance transformation is required for matching networks compared to single-ended configurations with the same output power level, which makes matching easier and also achieves wider bandwidths according to (1.3) in Chapter 1.
- A virtual ground in the symmetry plane can be used for more compact and simple matching structures.
- Cancellation or reduction of even harmonic products.

## 4.2 Practical Design of Push-Pull PAs

The theoretical analysis for a very compact *LC* balun transformer given in **Paper V** is presented at the start of this section. The compact balun is employed to meet both the 180° phase shift and high impedance transformation requirements. In addition, harmonic tuning as well as quasi-static drain supply modulation technology, as described in **Paper IV** and **Paper V**, are adopted to achieve higher efficiency at saturation and back-off power regions. Finally, a manufactured SSPA prototype based on the proposed methodology will be demonstrated.

### 4.2.1 Lumped *LC* Balun Transformer

Balun is the critical element in push-pull configuration, it stands for the balanced to the unbalanced transformer that generates the phase shift between the split signals, and can incorporate a part of the impedance transformation and further reduce the impedance transformation ratio of the matching network [85]. It can provide other advantages for push-pull topologies like wider bandwidth and lower losses [86]. One practical advantage of this work is the replacement of heavy, costly, and less repeatable ferrite transformer balun by implementing with a lumped *LC* balun, not only for its compact nature but also for its low loss features. Lumped *LC* baluns have been verified as good solutions for balanced filters in the low power region in integrated circuit applications [87, 88, 89], and derivations with theoretical analysis of a modified lumped LC balun can be found in [90].

Baluns are very useful passive components in high-frequency circuit designs. The most frequently used application is connecting unbalanced or single-ended circuits to balanced or differential circuits[91]. Baluns are required components in e.g. push-pull amplifiers [92], balanced mixers, balanced frequency multipliers, phase shifters, balanced modulators, dipole feeds, and numerous other applications.

Symmetrical transistors are required for the SSPA push-pull configuration, it is necessary to provide the ground-related unbalance-to-balance transformation both at the input and output of the power amplifier. An established method to solve this problem at RF and microwave frequencies is to use transmission line baluns [93]. But for the low VHF band application, a quarter-wavelength microstrip will occupy a very large area, preventing a compact design. Therefore, the lumped LC balun is preferred and implemented with two inductors and two capacitors. Originally introduced in the early 1930s as an antenna balun [94], the LC lumped lattice balance balun converts the balanced input to an unbalanced output by shifting the phase of one input port by $+90^\circ$ and the second input port by $-90^\circ$.

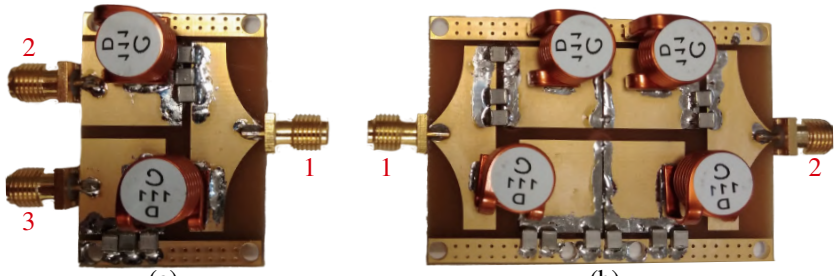
### Circuit Implementation

As mentioned above, a high impedance transformation ratio in the balun makes the high power transistor matching easier. Thus, in this work, the unbalanced impedance is set to environmental system load, i.e., $R_u = 50\ \Omega$, and the balanced impedance is set to $R_b = 9\ \Omega$ considering the matching network complexity. With the targeted design frequency at $f_0 = 27$ MHz, the component values of the LC balun can be derived from (4.1) as: $L_i = 125$ nH and $C_i = 278$ pF. Available and realizable values are $L_i = 111$ nH and using a sum of parallel capacitors gives $C_i = 280$ pF. The finalized and fabricated lumped LC balun is presented in Figure 4.1(a).

$$\begin{aligned} L_i &= \frac{\sqrt{R_u \cdot R_b}}{\omega_0}, \\ C_i &= \frac{1}{\omega_0 \sqrt{R_u \cdot R_b}}. \end{aligned} \tag{4.1}$$

where

| | |
|---|---|
| $\omega_0$ | $=2\pi f_0$; |
| $f_0$ | operating frequency; |
| $R_u$ | unbalanced resistance; |
| $R_b$ | balanced resistance. |




(a) (b)

*Figure 4.1. (a) Photograph of fabricated lumped LC balun with specified port number. (b) Photograph of two identical LC baluns connect symmetrically.*

### S-Parameter Measurements

The balun shown separately in Figure 4.1(a) is a 3-port passive device and its response can be fully described by the 3-port scattering parameters in (4.2) if all ports are accessible to measure, as described in Section 2.1.

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix} \tag{4.2}$$

where $a$ represents an incident signal, and $b$ represents the scattered signal from the S-parameter definition.

The balanced port 2 and 3 specified in Figure 4.1(a) are not externally accessible as they are internally connected to the amplifier via microstrip (MS) connections. However, the response of the balun itself can be evaluated by inserting additional coaxial connectors to perform measurements on the MS ports. The effect of the connectors at the operating frequency in this work, i.e., 27 MHz, could have been neglected or de-embedding was conducted using a model of the coaxial connectors based on the physical dimensions and properties of the connectors.

In addition, the balun is intended to be used with balanced signals of equal amplitude and signals that are 180° out of phase, these signals are incident at port 2 and port 3. Using a method sometimes referred to as active multi-port injection, it is possible to calculate a novel set of "active" parameters for the behavior of the 3-port for the particular conditions of a differential input signal on the balanced port 2 to port 3. This method, as shown in (4.3), is often used in 3D simulators [68], such as Ansys HFSS, and can be used to measure active parameter sets for the excitation of multi-port antenna systems where multi-port excitation is required, in order to achieve sufficient power at the receiver [95]. The definition of the active scattering parameter is already given in Section 2.1.2 and is copied below for the sake of simplicity.

$$activeS_{mn} = \frac{\sum_{i=1}^{N} S_{mi} a_i}{a_n} \tag{4.3}$$

where $S_{mi}$ is the general standard "passive" S-parameters measured directly by VNA. From the theoretical perspective in (4.3), it's clear that all "active" S-parameters can be achieved through "passive" S-parameters. Therefore, it's more of a post-processing result.

Considering that this is a particular 3-port design with the differential input signal, an easier-to-understand alternative that uses the differential method can also use the standard S-parameters to calculate the transmission, reflection, and losses for the balun.

From the measured 3-port S-parameters the ideal differential reflection response as output balun combiner for port 2, $S_{22}^{Diff}$ can be calculated from the second line in (4.2) with $a_1 = 0, a_2 = a_2$ and $a_3 = -a_2$.

$$S_{22}^{Diff} = S_{22} - S_{23} \tag{4.4}$$

As a comparison, given the same condition, $activeS_{22}$ can be obtained as

$$activeS_{22} = S_{22} - S_{23} \tag{4.5}$$

It can be found that $S_{22}^{Diff}$ is exactly same as $activeS_{22}$.

Similarly, $S_{33}^{Diff}$, the ideal differential reflection response as output balun combiner for port 3, i.e., $activeS_{33}$, can be calculated from the third line in

(4.2) with $a_1 = 0, a_2 = -a_3$ and $a_3 = a_3$.

$$S_{33}^{Diff} = activeS_{33} = S_{33} - S_{32} \tag{4.6}$$

And the input reflection for ideal differential operation $S_{11}^{Diff}$ in line with $activeS_{11}$ would be

$$S_{11}^{Diff} = activeS_{11} = S_{11} \tag{4.7}$$

The phase difference $\Delta\varphi$ as input balun splitter is defined as

$$\Delta\varphi = phase(S_{21}) - phase(S_{31}) \tag{4.8}$$

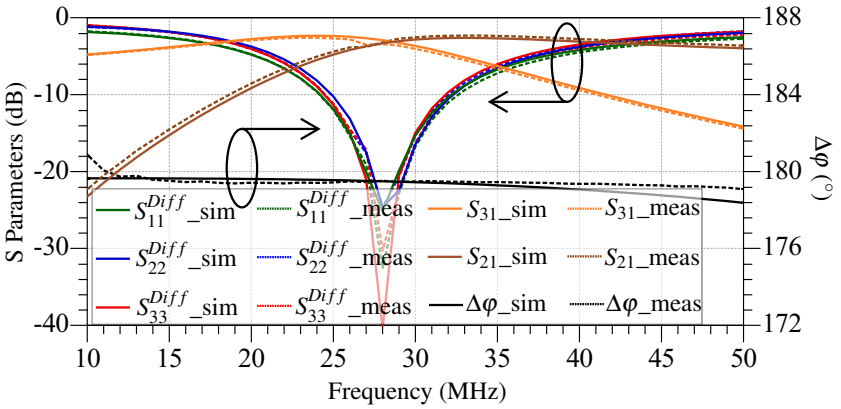



*Figure 4.2. Simulations (solid lines) and measurements (dotted lines) of differential and standard S-parameters for the 3-port lumped LC balun in Figure 4.1(a). The terminal impedance of port 2 and port 3 is* 4.5 Ω*, while the terminal impedance of port 1 is* 50 Ω*.*

The simulation results, using EM simulated board and components models from vendors, and the measurement results are shown in Figure 4.2. The results show a good agreement between simulations and measurements. The differential input and output match are all lower than $-20$ dB at 27 MHz, which implies good matching at each port. $S_{21}$ and $S_{31}$ are also shown in Figure 4.2 to illustrate the amplitude balance between the ports. A 1 dB balance can be expected over a 5 MHz range centered around 27 MHz. The phase difference $\Delta\varphi$ between $S_{21}$ and $S_{31}$ is stable around 180° with only 0.2° variations from 15 MHz to 40 MHz which shows an excellent balance in both branches.

Additionally, to evaluate the transmission loss of this LC balun, two identical lumped LC baluns are symmetrically connected back-to-back as shown in Figure 4.1(b). The measured results show an input matching lower than $-30$ dB at 27 MHz, and the insertion loss $S_{21}$ is $-0.2$ dB, which implies that the transmission loss of this lumped LC balun is only 0.1 dB.

From the measurement results presented above, it can be seen that this lumped LC balun realizes a 180° phase shift and has good matching on both

the balanced and unbalanced ports. All simulations and measurements indicate that this fabricated balun is an excellent candidate for implementing efficient push-pull amplifiers.

### 4.2.2 Second Harmonic Load-Pull

Harmonic components of voltage and current have a significant impact on the shape of waveforms, which affect RF performance accordingly, as described in Chapter 3. And of course, as the harmonic order increases, the harmonic importance diminishes. Moreover, due to the influence of $C_{ds}$ presented in Chapter 1, the higher-order harmonics are inevitably short-circuited. Thus, considering practical factors, it only makes sense to discuss the first three harmonics while the second harmonic is more important. To evaluate the impact of the second harmonic impedance on the transistor's efficiency and output power, load-pull simulations based on a large signal transistor model are depicted in Figure 4.3. From the convergent load-pull contours, it can be observed that the result of the second harmonic load pull shows a large degradation of the performance in terms of output power and drain efficiency, which is illustrated as a blue area in Figure 4.3(a) and (b). While the contours also show the best performance, i.e., the maximum efficiency and output power, illustrated as a red area in Figure 4.3(a) and (b). Second harmonic load-pull simulations from 25 MHz to 29 MHz show that these areas have an anti-clockwise shift with frequency increase. Related results are also included in Figure 4.3. Since the red and blue areas are all located at the edge of the Smith chart, the best and worst performing can swap by tuning the phase of the second harmonic. The efficiency degradation or null location changes from device to device, from technology (such as LDMOS) to technology (such as GaN) [96].

**Harmonic Trap**

In order to improve the RF performance in terms of the drain efficiency and output power, the second harmonic impedance should be located in the red area, and the blue area in Figure 4.3(a) and (b) should be avoided. This is an essential step in this work, which is realized simply by implementing a harmonic trap. The area indicating the optimum second harmonic impedance is almost purely reactive. The resonance of the harmonic trap consisting of a series resonant LC network is initially set close to $2f_0$, and then slightly adjusted by changing the component value to shift the impedance to the reactive red area. Predictably, in the higher frequency bands, the output power and efficiency will suffer from the null point since the phase of the second harmonic inevitably shifts from the red to the blue area.

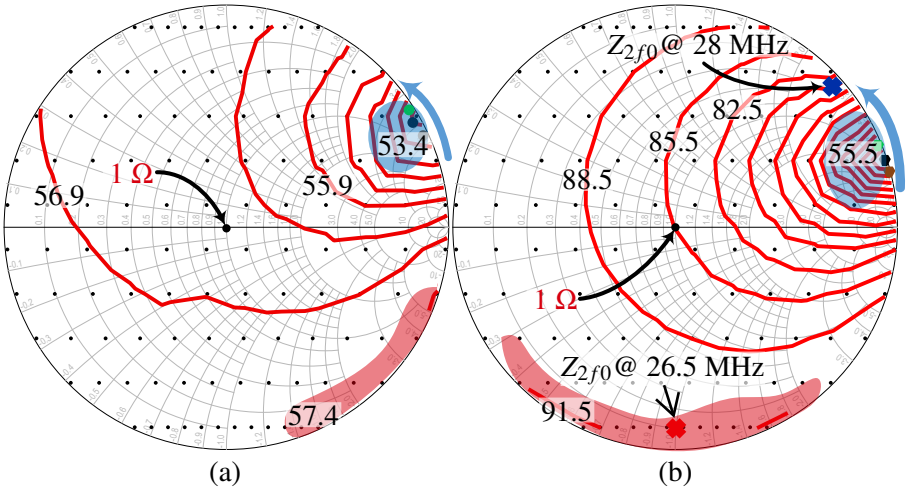



*Figure 4.3. Simulated 2nd harmonic load pull contours at $f_0 = 27$ MHz in 3 dB compression (Bias Status: $V_{DD} = 55$ V, $I_{DQ} = 200$ mA). (a) Output power in dBm, (b) drain efficiency in (%). Note: the Smith chart is normalized to 1 Ohm and the load pull simulations are due to symmetry conducted on one transistor. $Z_{2f_0}$@x MHz is the simulated 2nd harmonic impedance of finalized circuit when $f_0 = x$ MHz.*

### 4.2.3 Matching Circuit Design

Following the design strategies introduced above, the schematic of the proposed push-pull SSPA design is described in Figure 4.4. It comprises two lumped baluns, two harmonic traps, DC supplies, input matching network (IMN) and output matching network (OMN). The lumped balun realizes the 180° phase difference between $S_{21}$ and $S_{31}$ both on the input and the output side. IMN and OMN are pre-matching networks that work with the lumped balun, to transform the matching impedance to a 50 Ω environment system.

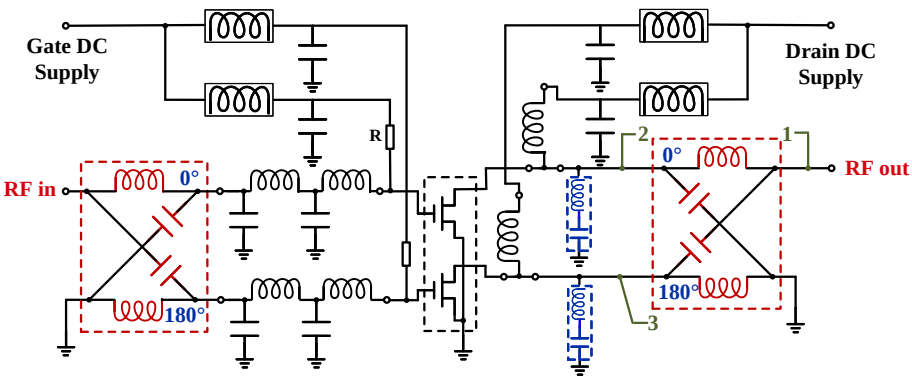



*Figure 4.4. Design schematic including harmonic traps, and lumped baluns.*

The commercial FR4 [97] material is used as substrate in this work. Its final design layout with all components is illustrated in Figure 4.5. The fundamental impedance with the reference plane at the transistor package was chosen to (3 + $j$1.5) Ω at 27 MHz. OMN of the push-pull design is symmetrical for the upper and lower branch. The 42 nH inductor (L6) shunted to the ground through a 22 nF capacitor (C8) generates the required reactive part for the fundamental of the OMN and shifts the real part to the required 4.5 Ω input impedance of the balun. The output balun then provides the impedance transformation from balanced 9 Ω (each branch 4.5 Ω to ground) to the 50 Ω load impedance. L7 and C9 constitute the harmonic trap which is a series LC resonator shunted to the ground and providing the high reactive part at the second harmonic. L5 is the RF isolation for the DC feed and C12 paralleled with C13 are the DC block capacitors on the output.

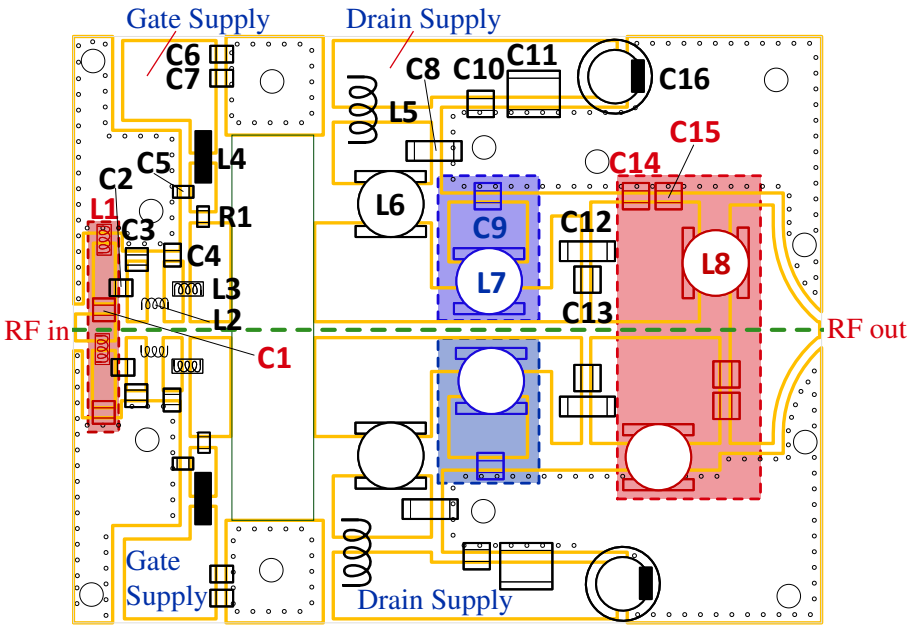



*Figure 4.5. Finalized design layout based on commercial off-the-shelf (COTS) components. The areas marked in red comprise the input and output lumped baluns, while the LC series harmonic traps are marked in blue. All components except balun at the lower side are horizontally mirrored values from the upper side.*

At the input side of the SSPA, (2.5 - $j$5) Ω is selected as the fundamental input impedance. A two-stage LC low-pass network transforms the impedance to approximately 25 Ω. The final transformation to 50 Ω is conducted in the input balun. Resistor R1 and a long ferrite bead (L4) provide LF stability in the DC feed. C5 is the input RF bypass capacitor.

Finally, the photograph of the fabricated circuit is shown in Figure 4.6.

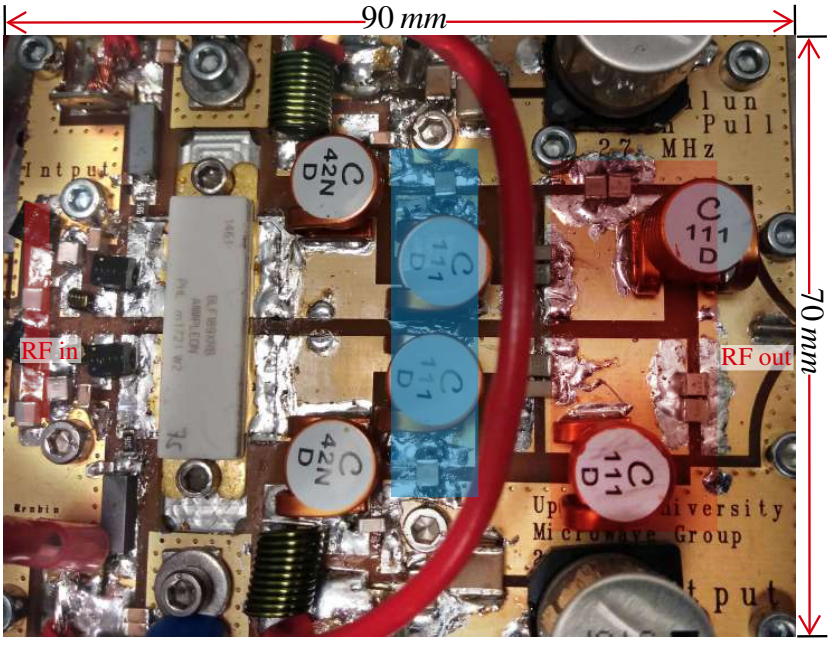



*Figure 4.6. Photograph of the fabricated high-power SSPA with the lumped balun covered in red and harmonic trap covered in blue, the color setting is also corresponding to Figure 4.4.*

Co-simulations with momentum verified PCB layouts and lumped component models from vendors were evaluated and optimized to ensure a close match to the required impedances. The harmonic balance (HB) method is employed to simulate high-power RF performance in the design phase. In addition, a small-signal co-simulation also shows that the stability factor is greater than 1 from 1 MHz to 500 MHz, which means that the SSPA is unconditionally stable in this frequency band including the operating band.

The simulated frequency sweeps in addition to the power sweep can be found in Figure 4.8 and Figure 4.9 respectively in the next Section as a comparison to the measurements. Moreover, to verify the efficiency improvement from the harmonic trap, the simulated response for a solution without a harmonic trap is also shown in Figure 4.9. It shows that efficiency significantly improves with about 15%-points in saturation when the harmonic trap is implemented. From the frequency sweeps in Figure 4.8, it can be seen that the efficiency drastically drops when the frequency increase to 28 MHz. From the large-signal HB simulation, the second harmonic impedance $Z_{2f_0}$ is (0.1 - $j$1) Ω at $f_0 = 26.5$ MHz, while it changes to (0.3 + $j$3) Ω when $f_0 = 28$ MHz. The corresponding impedances are presented in the Smith chart in Figure 4.3(b). Their locations in the Smith chart imply that the efficiency

drop at 28 MHz is caused by the second harmonic impedance position near the blue inefficient region.

## 4.3 RF and Thermal Performance Evaluation

To make this design work at high efficiency without negative impact from the high-temperature operation, an excellent thermal contact to the cooling plate and heat conducting compound between the transistor and the cooling plate is required. During measurements, a water cooling system with a water flow of 8 L/min is operated to cool down the heat sink plate. The assembled SSPA can be seen in Figure 4.6, the aluminum heat sink plate located below the transistor has a void channel with continuous cold water flow. The heat sink is used for cooling purposes, but also to fix the PCB.

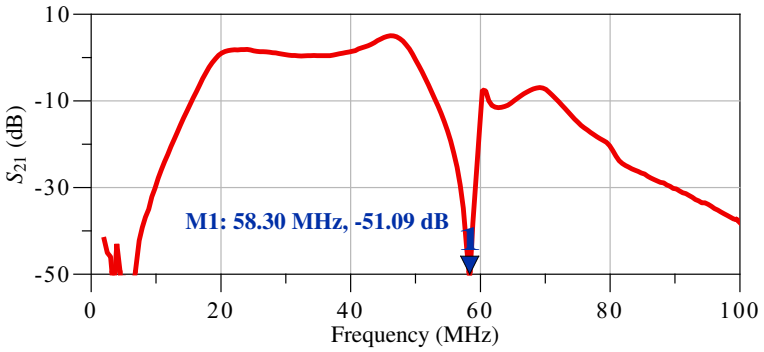



*Figure 4.7. Frequency response of small signal $|S_{21}|$, results are measured by Keysight N9912A. (Bias Status: $V_{DD}$ = 55 V, $I_{DQ}$ = 0 mA).*

**Small-Signal RF Measurements**

The frequency response, measured by a handheld vector network analyzer (VNA), under small signal excitation at $P_{in}$ = -15 dBm is shown in Figure 4.7. To protect the VNA, a class C bias is adopted here to decrease the output power. This means that this SSPA is still pinched-off at this quiescent point and input power level [98], but the small-signal frequency response shows that this design covers the full 27 MHz bands. More importantly, the measurement verifies that the harmonic trap is located at the targeted 58 MHz. This dip is intentionally caused by the harmonic trap circuit to increase the efficiency.

**High Power Pulsed Measurements**

The high-power RF measurement bench setup for large-signal excitation is illustrated in Figure 2.9 in Chapter 2. It is optimized for high-precision measurements of pulsed signals in the kilowatt power range, its related calibration and measurement methodology was also introduced previously in Chapter 2.

The bias status is set as follows: drain bias voltage $V_{DD}$ = 55 V with the quiescent drain current $I_{DQ}$ = 200 mA. The RF input is a pulsed RF signal with 3.5 ms *pulse width* and 70 ms *pulse period*. Hence the duty cycle for the input pulse signal is 5%.

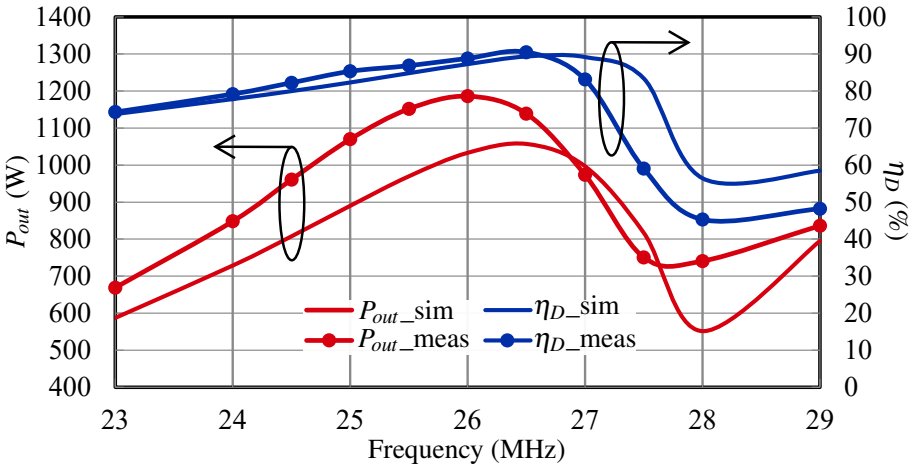



*Figure 4.8. Simulated (solid lines) and measured (solid lines with circles) frequency sweep results for output power and efficiency at saturated power, $P_{in}$ is fixed at 40 dBm.*

To evaluate the frequency response characteristics of the SSPA, a frequency sweep into saturation was conducted, and the related output power and efficiency performance are depicted in Figure 4.8. The measurement results show that this SSPA achieves more than 83% drain efficiency with more than 960 W output power in the 24.5∼27 MHz frequency band, while the input matching is lower than -11 dB for the whole band. Thus, the corresponding relative bandwidth is approximately 10%. The power and efficiency drop sharply at higher frequencies are also observed. The frequency can be shifted by tuning the components values of the harmonic trap, consistent with the analysis in Section 4.2. Further analysis shows that the efficiency drops sharply from 89% to 48% when the frequency increases to 28 MHz since the phase of the second harmonic shifts from the red area in the direction of the blue area in the Smith chart of Figure 4.3(b). These measurement results verify the theoretical analysis of the impact of the second harmonic. Furthermore, measured power sweep results at 26.5 MHz presented in Figure 4.9 show a maximum drain efficiency of 89% at an output power of 1150 W. The power gain $G_p$ is 23 dB and the input matching is lower than -15 dB. Hence, the measurements show a good agreement with the large-signal simulations.

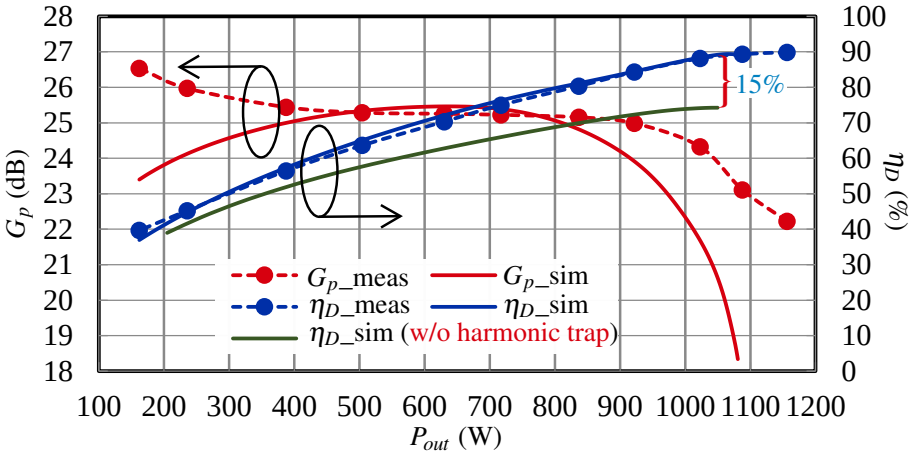



*Figure 4.9. Simulated (solid lines) and measured (solid lines with circles) power sweep results at 26.5 MHz.*

**Pulse and CW Measurements**

In Section 2.2.1, it was analyzed that the 3.5 ms *pulse width* RF pulse can fully reflect the expected CW performance of the particular transistor since it only exhibits a temperature rise of around $10°C$ when operating efficiently in the kilowatt range. Given that this is a high power design and in particular a relatively low impedance node given the lumped balun's transformation ratio, the current handling and thermal limitations of the balun components should be evaluated. Therefore, the power sweep is evaluated in pulse tests with a 5% and 50% duty cycle, and with the same *pulse period* of 70 ms, and a CW test. Their corresponding RF performance is shown in Figure 4.10.

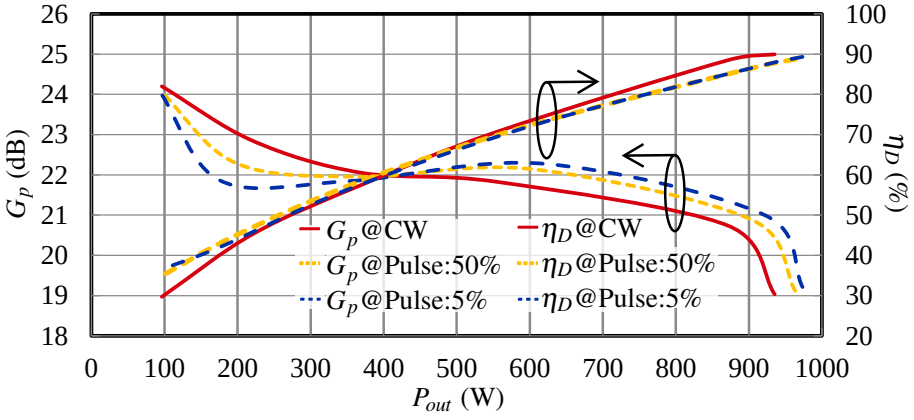



*Figure 4.10. Comparative power sweep results under CW and Pulse mode.*

Meanwhile, as can be seen from the summarized RF performance in Table 4.1, the CW measurement results in a slight degradation compared to the

**Table 4.1.** *Measurement comparison for CW and Pulse test with full power @26.5 MHz. (Bias Status: $V_{DD}$ = 50 V, $I_{DQ}$ = 200 mA).*

| Test Methodology | $P_{out}$ (W) | $\eta_D$ (%) | $G_p$ (dB) |
|---|---|---|---|
| Pulse (Duty Cycle: 5%) | 973 | 89.3 | 19.2 |
| Pulse (Duty Cycle: 50%) | 963 | 88.7 | 19.1 |
| CW | 935 | 89.9 | 19.0 |

pulse measurements, but can still produce about 1 kilowatt with 89% efficiency.

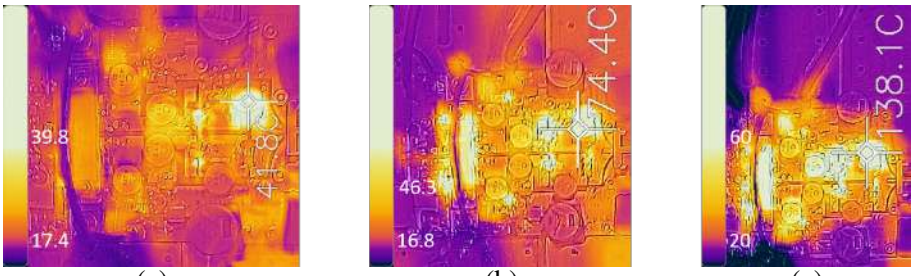
The detailed thermal measurements under pulse and CW will follow in the next Section.

**Thermal Evaluation**

Given the very high power output and continuous operation in the application, it is important to identify the root causes of the remaining losses in order to verify operation under thermally safe operating conditions and provide understanding for further improvements. Therefore, the thermal performance is also evaluated during the RF pulse and CW measurements. The thermal images were taken while the amplifier operated under steady-state conditions. To reach steady-state conditions, the cooled SSPA was operated with an output power of around 1 kW for approximately 20 minutes, then the thermal images shown in Figure 4.11 were captured with a FLIR ONE Pro IR camera. Figure 4.11 verifies that the cooling of the transistor is very efficient and keeps the transistor flange well cooled even when the SSPA delivers 1 kW output power. The highest temperature reading of the board is 42°$C$ at 5% RF pulse as shown in Figure 4.11(a), 75°$C$ in 50% RF pulse as shown in Figure 4.11(b), and 139°$C$ in CW as shown in Figure 4.11(c). The highest temperature spots are all on inductor L8 in the output balun. C12, which acts as part of the DC block, as well as L5, L6 and L7 also show an increase in temperature. This indicates that the passive components and board losses can contribute significantly to the overall system losses.

Based on the component models it is possible to simulate the power dissipation in each passive component and identify the contribution to the overall loss. From the results, it is clear that the inductor **L8** of the output balun makes the main contribution to the total losses with 19 W of dissipated power. Despite the large power loss, it is still within the limits for the component. In addition, the capacitor C12 contributes about 6 W of power dissipation. The board itself shows losses in the 11 W range based on the EM simulations.

What the thermal analysis foremost show is that, in reality, the transistor itself is so efficient that the dissipated power from the matching network has a significant impact on the overall efficiency, and more attention needs to be given to optimizing the passive parts of such high power designs.




(a) (b) (c)

*Figure 4.11. Thermal image during the RF measurements at (a) 5% RF pulsed mode, (b) 50% RF pulsed mode, and (c) CW mode. All modes with 1.0 kW output power and water cooling with a flow rate of approx. 8 L/min. The images are captured with an infrared camera (FLIR model: ONE Pro).*

**Quasi-Static Drain Supply Modulation**

Drain supply modulation can serve as an efficiency enhancement method that can bring very good performance at back-off power levels as described in Chapter 1. From a static evaluation of the SSPA at different supply voltages, the performance with drain supply modulation can be predicted. A so-called shaping function, i.e., a look-up table of the optimum combinations of supply voltages and output powers can be identified [99]. Normally the drain supply has to be modulated according to the envelope of the signal but in this application the output power is constant, and it can be statically adjusted to accommodate different output power levels. The series of power sweep curves at different drain biases and the corresponding drain efficiency curves that are presented in Figure 4.12 show the full potential of power control by using drain supply modulation.

After post-processing of the statistical analysis of the drain bias voltage and output power values at maximum efficiency points, the functional relationship, i.e., the shaping function, between the drain bias voltage $V_{DD}$ and the output power $P_{out}$ can be empirically expressed as follows:

$$Vd_{fit} = \begin{cases} 30, P_{out} \leq 300 \\ p1 \cdot P_{out}^2 + p2 \cdot P_{out} + p3, P_{out} > 300 \end{cases} \tag{4.9}$$

Here $Vd_{fit}$ is the drain bias fitting voltage of $V_{DD}$ that auto-sets on the DC supply when output power changes. $Vd_{fit}$ is set to 30 $V$ when the output power $P_{out}$ $\leq$300 W. When $P_{out}$ $>$300 W, the quadratic polynomial function in (4.9) is used to fit the drain voltage, final practical parameters are listed as follows: $p1 = -8.13e-06$, $p2 = 0.043$, $p3 = 17.89$. The calculated results for power sweeps with drain supply modulation based on large-signal measurements at different supply voltages are also shown in Figure 4.12. More than 90% drain efficiency can be expected over a 5 dB output power back-off range.

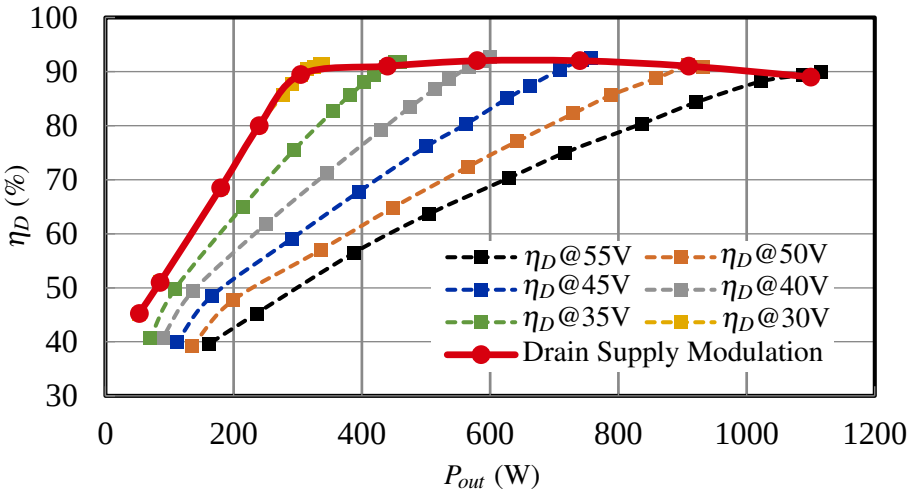



*Figure 4.12. Measured power sweep results after adopting quasi-static drain supply modulation (red solid line with circles), and measured power sweep results at different bias statuses (dashed lines with squares).*

In general power supplies in these power and voltage ranges have an efficiency exceeding 90% [100]. Some allow voltage control within a 20-30% range but the efficiency might be decreased. Given the very high power in this application a dual power supply system where two power supplies, one at 45 V and one at 55 V may be an option. They would be software controlled and provide maximum efficiency at full power and 75% of full power respectively. The reduced energy consumption rapidly compensates additional cost of the second DC supply.

## 4.4 Chapter Summary

This chapter demonstrated a very compact (90 mm $\times$ 70 mm) and highly efficient kilowatt push-pull SSPA in a low VHF band, this module is developed to be used for RF power source systems in radioisotope production. The measured results of the fabricated SSPA show that it achieves about 89% efficiency with 1150 W output power at 26.5 MHz, and more than 83% efficiency with more than 960 W in the entire 24.5$\sim$27 MHz band. In addition, a quasi-static drain supply modulation manages to realize more than 90% drain efficiency over a 5 dB back-off power range.

# 5. Conclusions

The work presented in this thesis concerns efficient SSPA exploration in high-power RF sources as well as its associated measurement technologies. It offers a new understanding of the SSPA architecture from circuits, design methods and analytical approaches. These in-depth analytical approaches have been evaluated using a large number of simulations, including small-signal S-parameter simulation and large-signal HB simulation, and also verified by measurements on demonstrated circuit designs. And the final results show good agreement between simulation and measurement. Overall, the theoretical and experimental studies in this thesis complement each other and construct a comprehensive understanding of the SSPA used in particular for RF source applications. In summary, the main contributions of this thesis are highlighted as follows:

- **Thru-Only De-embedding Approach**: This de-embedding approach benefits from the fully symmetric nature of the constructed tapered transmission line test fixture and requires only one THRU standard. An important point of this approach is the solution for a new coefficient $R_x$, which is defined to reflect the inherent physical properties of the transmission network. Compared to previous thru-only de-embedding methods, the present approach is applicable to a significantly wider frequency range and offers significantly more flexibility in the design of the test device. In addition, this approach simplifies the procedure in the case of multiport configurations compared to traditional complicated calibration methods, like TRL.
- **High Power Measurement Bench**: The high-power measurement bench and its required calibration method are developed as a solid hold for measuring PA modules in the kilowatts and even tens of kilowatts range. Moreover, an automatic measurement program based on the MATLAB platform is also being developed for fast measurements. Meanwhile, data processing is also included in the measurement program.
- **High Efficiency SSPA Modules**: As the core of the RF power source, two efficient SSPA modules are developed and implemented respectively in single-ended and push-pull configurations. Waveform engineering and harmonic load-pull techniques are involved for efficiency improvements. Multimode operation with Class-J / Class-$F^{-1}$ properties are examined from theory to practice. The push-pull PA module using lumped balun reaches the compact purpose. Both SSPA modules are evaluated for RF and thermal performance, the associated measured results improve the state-of-the-art.

- **Power Control and Back-off Efficiency Improvements**: In order to increase the efficiency in the back-off power range, the implemented two SSPA modules were intentionally designed and evaluated at various drain supply voltages. With more than 90% efficiency is achieved over 5 dB output power back-off using quasi-static supply modulation.

The thesis has presented promising SSPA architectures that achieve high efficiency in saturation and back-off power region by using waveform engineering, harmonic load-pull, bias modulation, etc. The proposed topologies and measurement technologies in this thesis can be used further to facilitate the development of the RF power source system.

## 5.1 Future Perspectives

With the increasing demand for high-power RF sources in much broader applications, more efforts are directed to higher power and higher frequency for RF power source developments, therefore, more efforts can be made for interesting research topics as follow:

- **Higher Frequency Trends**: The SSPA of RF power source implementation will toward the higher frequency range with the application expansion. Therefore, with the development of RF power transistor technologies, some lateral technologies like GaN and AlN are promising candidates and could benefit from the developments for industries. Other alternatives include GaO and vertical GaN. These technologies are expected to be mature in a 5 to 10 year perspective, and their costs will continue to decrease with their widespread commercial use.
- **High Efficiency Technologies**: It is possible to develop or dig more potential of SSPA efficiency when using advanced RF power transistor technologies, such as the well-known switching mode, etc. The efficiency enhancement technology can consider combining both load modulation and bias modulation together for back-off efficiency improvements. Additionally, PA architectures such as Doherty, Outphasing, etc., and novel configurations or architectures should be further explored to find the efficiency potential, as the efficiency technologies for individual transistors have been well studied over the past few decades.
- **Power Combining Technology**: Power combination plays a crucial role as SSPA in RF power sources. Wilkinson, Gysel power combiner or divider as well as cavity combiner, etc., should be investigated and then explored compact and efficient $N$-way power combiner to be used in RF power source. In fact, in this RF power source study, some meaningful and promising research is already being carried out, an ultra-compact multi-way power combiner based on the cavity resonator is designed, its related theory is also explored, along with good measurement results are obtained. The associated work will be disclosed after the relevant patent application has been issued.

# Sammanfattning på Svenska

Radiofrekventa (RF) effektgeneratorer används i många olika områden. Ett av de viktigaste områdena är inom medicinsk teknik för generering av kortlivade radioaktiva spårämnen s.k. radioisotoper för positronemissionstomografi (PET). Systemen är konstant i drift och kräver omfattande underhåll vilket leder till höga driftkostnader. Därför att det viktigt att det utvecklas effektivare och mer underhållsfria RF förstärkare eftersom dessa bidrar mest till de höga kostnaderna för energiförbrukning och service av effektgeneratorerna. Historiskt har dessa högeffekt RF/mikrovågs-förstärkare baserats på vakuumrör-teknologi men halvledarteknologi har på senare år klivit fram som ett tekniskt realiserbart alternativ som erbjuder bättre effekt-kontroll, högre tillförlitlighet och enklare handhavande. Halvledarbaserade förstärkare (Solid-State Power Amplifier, SSPA) möjliggör dynamisk effekt och frekvenskontroll för att optimera energiöverföringen. Dessutom har halvledare längre livslängd och moduler kan bytas ut under drift vilket leder till längre drifttid och färre kostsamma driftstopp. Summerat innebär införandet av halvledarteknologi i effektgeneratorer att RF-energi kan genereras mer effektivt och kontrollerbart, i mindre och robustare moduler vilket leder till kompaktare system med mindre underhåll och längre drifttid. Detta avhandlingsarbete är ett led i att visa möjligheterna med sådana system.

Denna avhandling handlar om effektiva halvledarförstärkare (SSPAs) för effektgeneratorer och RF-mätningar av dessa förstärkare. Först avhandlas det MATLAB styrda automatiserade RF-mätsystemet som möjliggör snabba, små- och stor-signal mätningar av de utvecklade RF modulerna. En ny enklare metod “thru-only” for att de-embedda multiport mätningarna för de balanserade förstärkarna som utvecklades beskrivs sedan. Andra delen av avhandlingen berör sedan utvecklingen av de effektiva halvledarbaserade kilowatt-modulerna som krävs för effektgeneratorer. En multimode kilowatt-förstärkare för 100 MHz som utvecklats med hjälp av Fourier-vågformsanalys ger mer än 90% verkningsgrad med bara 5 dB variation i uteffekt genom statisk kontroll av drivspänningen. En annan kompakt push-pull kilowatt förstärkare för 27 MHz med harmonisk avstämning visar även mer än 90% verkningsgrad över 5 dB effektförändring på utgången. Även denna med effektstyrning över matningsspänningen. Båda är baserade på Si-LDMOS technologi och når absoluta topp-värden för forskningsfronten idag. De djupgående analyserna i avhandlingen understöds av omfattande simuleringar, innefattande småsignal, storsignal (Harmonic Balance, HB) och fält-simuleringar (FEM) som sedan bekräftas i demonstratorer. De

teoretiska och experimentella undersökningarna kompletterar varandra och skapar ny förståelse kring utvecklingen av högeffektiva halvledarförstärkare som effektgeneratorer.

Sammanfattningsvis utgör huvudbidragen till forskningsfronten i denna avhandling:

- **Enbart Thru-deembedding**: En de-embeddingmetod som utnyttjar symmetrin i avsmalnande (taperade) transmissionsledningar för att flytta referensplanen i test-fixturer. Viktigt med denna metod är koefficienten $R_x$ som återspeglar de fysikaliska egenskaperna as transmissionsledningen. Jämfört med etablerade metoder som också baseras på en thru-standard kan den föreslagna metoden användas över en större bandbredd och ger mer flexibilitet i hur standarden designas. Metoden är avsevärt enklare för multiport kalibreringar än den etablerade och mer komplexa TRL metoden.
- **Högeffektmätplats**: Mätplatsen för höga RF effekter och dess kalibrering har utvecklats för att genomföra precisionsmätningar för riktigt höga effekter i kilowatt området. Det innefattar även automatisk styrning med MATLAB samt databehandling och presentation av data.
- **Effektiva kilowatt halvledarmoduler**: Två alternativa högeffektiva RF-kilowatt moduler för effektgeneratorer har utvecklats. En single-ended multimode förstärkare och en push-pull förstärkare med harmonisk avstämning. Vågformsanalys och harmonisk avstämning har använts för att skapa riktigt hög verkningsgrad. Den högeffektiva multimode (klass-J / klass-$F^{-1}$) förstärkaren har analyserats från teori till praktik och visar nyttan med vågformsanalys även för smalbandiga tillämpningar. Push-pull förstärkaren med den komponentbaserade balun-designen visar att även kilowatt-moduler kan göras väldigt kompakta. Även de termiska egenskaperna har utvärderats för de tillverkade förstärkarna.
- **Effektreglering och verkningsgrad i back-off**: Vanligtvis används inte effektgeneratorerna vid sin fulla uteffekt utan uteffekten måste kunna varieras (statiskt). Ofta regleras en förstärkares uteffekt genom att ineffekten förändras. Vilket dock är ineffektivt. I detta arbetet har förstärkarna medvetet designats för att uteffekten också skall regleras med hjälp av matningsspänningen. I båda förstärkarna kunde över 90% verkningsgrad uppmätas över 5 dB variation av uteffekten genom reglering av matningsspänningen.

Detta arbete breddar RF- och mikrovågsforskningen genom att skapa ny kunskap kring arkitekturer för halvledarförstärkare för kilowatt-applikationer. Från en analytisk bas har nya koncept tagits fram som implementerats i moderna verktyg och direkt omsatts i industriapplikationer. Detta har skapat nya metoder och verktyg som direkt baserat på moderna designmetoder,

förbättrar energieffektivitetet för effektgeneratorer, samt skapar möjligheten för mer robusta och flexibla halvledarbaserade effektgenerator-system med avsevärt lägre kostnader och längre livslängd. Metoderna och kunskapen kan även komma till användning i andra applikationer som telekommunikation och RADAR-system men även för ISM applikationer som uppvärmning, och för partikelacceleratorer.

# Appendices

## Appendix A: Derivation Process for Equation (2.12)

Equation (2.12) is significantly advantageous in S-parameters converted to S-parameters (stos), it can be easily used in network analysis such as to calculate the optimal reference impedance in a matching network, etc. Therefore, the derivation process is presented here to clarify it clearly as proof.

For an N-port network, its incident wave $a$, scattered wave $b$, voltage $V$ and current $I$ have the following relationships [101], rewritten below:

$$a = \frac{1}{2}\left(g^{-1}V + gI\right) \tag{A.1a}$$

$$b = \frac{1}{2}\left(g^{-1}V - gI\right) \tag{A.1b}$$

where $g = \text{diag}\left\{\sqrt{Z_{01}}, \sqrt{Z_{02}}, \ldots, \sqrt{Z_{0n}}\right\}$, $Z_{0n}$ is the reference impedance at port $n$.

Furthermore, (A.1) can be further revised as

$$g^{-1}V = a + b \tag{A.2a}$$

$$gI = a - b \tag{A.2b}$$

Assuming that the reference impedance changes to $Z'_{0n}$ ($Z'_{0n} = D_{xn}Z_{0n}$) at each terminal port, the characteristic impedance matrix $g$ then changes to $g'$ and $g' = \text{diag}\left\{\sqrt{Z'_{01}}, \sqrt{Z'_{02}}, \ldots, \sqrt{Z'_{0n}}\right\}$.
If defining $D_x = \text{diag}\left\{\sqrt{D_{01}}, \sqrt{D_{02}}, \ldots, \sqrt{D_{0n}}\right\}$, $g'$ then can be expressed as

$$g' = g \cdot D_x = D_x \cdot g \tag{A.3a}$$

$$(g')^{-1} = g^{-1} \cdot D_x^{-1} = D_x^{-1} \cdot g^{-1} \tag{A.3b}$$

When the reference impedance changes, the voltage changes to $V'$, and if $V' = \kappa V$ is set, the current $I' = \kappa I$ will be derived since reference impedance has no effect on the Y- or Z-parameter. Taking them into (A.1), with the modified reference impedance, it changes to

$$a' = \frac{\kappa}{2}\left[(g')^{-1}V + g'I\right] \tag{A.4a}$$

$$b' = \frac{\kappa}{2}\left[(g')^{-1}V - g'I\right] \tag{A.4b}$$

And then taking (A.3) into (A.4), it expands to

$$a' = \frac{\kappa}{2}\left(D_x^{-1} \cdot g^{-1}V + D_x \cdot gI\right) \tag{A.5a}$$

$$b' = \frac{\kappa}{2}\left(D_x^{-1} \cdot g^{-1}V - D_x \cdot gI\right) \tag{A.5b}$$

Subsequent taking (A.2) into (A.5) yields

$$a' = \frac{\kappa}{2}\left[(D_x^{-1} + D_x) \cdot a + (D_x^{-1} - D_x) \cdot b)\right] \tag{A.6a}$$

$$b' = \frac{\kappa}{2}\left[(D_x^{-1} - D_x) \cdot a + (D_x^{-1} + D_x) \cdot b)\right] \tag{A.6b}$$

Finally, from the definition of S-parameter, $S'_n = b'/a'$, $S_n = b/a$, when (A.6a) is divided by (A.6b) then gives (2.12).

# Appendix B: Codes Example for Pulse and CW Control

As an example of the RF pulse test and to show how waveform data is captured by the power meter, particularly in automatic measurement, R&S NRP2 [102] source control codes are demonstrated as follows, especially for 70 ms time periods signals.

```
function [retVal1,retVal2] = getPulseTrace(obj)
    open(obj);
    fprintf(obj.commObj, 'INIT:ALL:CONT OFF');
    fprintf(obj.commObj, 'SENS:FUNC "XTIM:POW"');
    fprintf(obj.commObj, 'SENS2:FUNC "XTIM:POW"');
    fprintf(obj.commObj, 'SENS:TRAC:POIN 100');
    fprintf(obj.commObj, 'SENS2:TRAC:POIN 100');
    fprintf(obj.commObj, 'SENS:TRAC:TIME 5e-3');
    fprintf(obj.commObj, 'SENS2:TRAC:TIME 5e-3');
    fprintf(obj.commObj, 'SENS:TRAC:OFFS:TIME -5e-4');
    fprintf(obj.commObj, 'SENS2:TRAC:OFFS:TIME -5e-4');
    fprintf(obj.commObj, 'TRIG:SLOP POS');
    fprintf(obj.commObj, 'TRIG2:SLOP POS');
    fprintf(obj.commObj, 'TRIG:LEV -25');
    fprintf(obj.commObj, 'TRIG2:LEV -25');
    fprintf(obj.commObj, 'TRIG:SOUR EXT');
    fprintf(obj.commObj, 'TRIG2:SOUR EXT');
    fprintf(obj.commObj, 'TRIG:DTIM 0');
    fprintf(obj.commObj, 'TRIG2:DTIM 0');
    fprintf(obj.commObj, 'SENS:AVER:STAT ON');
    fprintf(obj.commObj, 'SENS2:AVER:STAT ON');
```

```
    fprintf(obj.commObj, 'SENS:AVER:TCON REP');
    fprintf(obj.commObj, 'SENS2:AVER:TCON REP');
    fprintf(obj.commObj, 'FORM ASC');
    retVal1 = str2num( query(obj.commObj, 'READ?'));
    retVal2 = str2num( query(obj.commObj, 'READ2?'));
    close(obj);
end
```

Of course, considering the CW test, the CW data can also be captured by the codes listed above in pulse mode, but the duty cycle is set to 100%. However, the code is not efficient because data can be read directly in CW mode, so the source control codes are shown as follows:

```
function retVal = getPower(obj,SensorNum)
    open(obj);
    fprintf(obj.commObj,sprintf('FETCh%d?',SensorNum));
    retVal = str2double(fscanf(obj.commObj));
    fprintf(obj.commObj, 'INIT:ALL:CONT ON');
    close(obj);
end
```

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