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Metal Gate Technology for Advanced CMOS Devices

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Abstract

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The development and implementation of a metal gate technology (alloy, compound, or silicide) into metal-oxide-semiconductor field effect transistors (MOSFETs) is necessary to extend the life of planar CMOS devices and enable further downscaling. This thesis examines possible metal gate materials for improving the performance of the gate stack and discusses process integration as well as improved electrical and physical measurement methodologies, tested on capacitor structures and transistors.

By using reactive PVD and gradually increasing the N_2/Ar flow ratio, it was found that the work function (on SiO_2) of the TiN_x and ZrN_x metal systems could be modulated ~0.7 eV from low near nMOS work functions to high pMOS work functions. After high-temperature anneals corresponding to junction activation, both metals systems reached mid-gap work function values. The mechanisms behind the work function changes are explained with XPS data and discussed in terms of metal gradients and Fermi level pinning due to extrinsic interface states.

A modified scheme for improved Fowler-Nordheim tunnelling is also shown, using degenerately doped silicon substrates. In that case, the work functions of ALD/PVD TaN were accurately determined on both SiO_2 and HfO_2 and benchmarked against IPE (Internal Photoemission) results. KFM (Kelvin Force Microscopy) was also used to physically measure the work functions of PVD TiN and Mo deposited on SiO_2; the results agreed well with *C-V* and *I-V* data.

Finally, an appealing combination of novel materials is demonstrated with ALD $TiN/Al_2O_3/HfAlO_x/Al_2O_3$/strained-SiGe surface channel pMOS devices. The drive current and transconductance were measured to be 30% higher than the Si reference, clearly demonstrating increased mobility and the absence of polydepletion. Finally, using similarly processed transistors with Al_2O_3 dielectric instead, low-temperature water vapour annealing was shown to improve the device characteristics by reducing the negative charge within the ALD Al_2O_3.

Keywords: metal gate, high-k dielectrics, titanium nitride, zirconium nitride, MOSFET, thin film, work function, XPS

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List of Papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I G. Sjöblom, J. Westlinder, and J. Olsson, "*Investigation of the Thermal Stability of Reactively Sputter Deposited TiN MOS Gate Electrodes*", IEEE Transactions on Electron Devices, Vol. 52, No. 10, pp. 2349-2352 (2005)

II G. Sjöblom, H.-O. Blom, and J. Olsson, "*Flatband Voltage Adjustment Using Reactively Sputtered TiN Metal Gates*", Proc. of the AVS 4th International Conference on Microelectronics and Interfaces, pp. 215-217 (2003)

III J. Westlinder, G. Sjöblom, and J. Olsson, "*Variable work function in MOS capacitors utilizing nitrogen-controlled TiN_x gate electrodes*", Microelectronic Engineering, Vol. 75, No. 4, pp. 389-396 (2004)

IV J. Westlinder, J. Malmström, G. Sjöblom, and J. Olsson, "*Low-resistivity ZrN_x metal gate in MOS devices*", Solid-State Electronics, Vol. 49, No. 8, pp. 1410-1413 (2005)

V S. Abermann, G. Sjöblom, J. Efavi, M. Lemme, J. Olsson, and E. Bertagnolli, "*Comparative Study On The Impact Of TiN And Mo Metal Gates On MOCVD-Grown HfO_2 And ZrO_2 High-κ Dielectrics For CMOS Technology*", accepted for publication in Proc. of the 28th International Conference on the Physics of Semiconductors (2006)

VI G. Sjöblom, L. Pantisano, T. Schram, J. Olsson, V. Afanas'ev, and M. Heyns, "*Metal gate work function extraction using Fowler-Nordheim tunneling techniques*", Microelectronic Engineering, Vol. 80, 14th biennial Conference on Insulating Films on Semiconductors, pp. 280-283 (2005)

VII G. Sjöblom, N. Gaillard, D. Mariolle, F. Bertin, A. Bsiesy, M. Gros-Jean, and J. Olsson, "*Comparison between physical and electrical work function extraction methods: Kelvin force microscopy vs. capacitance and current measurements*", in manuscript (2006)

VIII D. Wu, A.-C. Lindgren, S. Persson, G. Sjöblom, M. von Haartman, J. Seger, P.-E. Hellström, J. Olsson, H.-O. Blom, S.-L. Zhang, M. Östling, E. Vainonen-Ahlgren, W.-M. Li, E. Tois, and M. Tuominen, "*A Novel Strained $Si_{0.7}Ge_{0.3}$ Surface-Channel pMOSFET with ALCVD^{TM} TiN/Al_2O_3/$HfAlO_x$/Al_2O_3 Gate Stack*", IEEE Electron Device Letters, Vol. 24, No. 3, pp. 171-173 (2003)

IX J. Westlinder, G. Sjöblom, J. Olsson, D. Wu, P.-E. Hellström, S.-L. Zhang, M. Östling, "*Effects of low-temperature water vapor annealing of strained SiGe surface-channel pMOSFETs with high-κ dielectric*", Proc. of the 33rd European Solid-State Device Research Conference, pp. 525-528 (2003)

Contents

1. Introduction

For the past four decades, silicon microelectronics has revolutionized and vastly improved the way we live. Major 20th century events such as the lunar space missions demanded swift calculations and hence, hastened the development of integrated circuits. The need for faster calculations, be it predicting climate changes, modelling the stock market, monitoring fiber-optic networks or rendering complex animated monsters in the latest 3D computer games, all require circuits with more densely packed transistors. In every logic circuit, the key element is the metal-oxide-semiconductor (MOS) transistor, which basically constitutes an electrical switch. The ever-present development of the transistor manifests itself in two ways. First, it has become smaller, and second, the number of transistors interconnected on state-of-the-art chips is in excess of 1 billion, as of 2006.

The history of integrated circuits (IC:s) is said to have started with the introduction of the bipolar transistor, pioneered by Bardeen, Brattain and Shockley in 1947. These devices, which were actually built from germanium, were about 100 times smaller than the bulky vacuum tubes which they replaced. During the 1950's, intensive research identified monocrystalline silicon as the material of choice for the modern transistor. The beauty of silicon is its ability to, under certain conditions, grow a fine, insulating oxide which simplified device manufacturing. These findings enabled Jack Kilby to invent the integrated circuit in 1958 and paved the way for Robert Noyce, who developed planar silicon technology the following year. This meant that the technology was ready for mass production, owing to the development of lithographic technology. When Dawon Kahng and John Attala of Bell Labs invented the MOS transistor in 1960 and engineers had figured out how to remove contaminants from silicon dioxide, the era of silicon microelectronics had begun. While the groundwork for the field effect transistor was laid down (and even patented) by J. E. Lilienfeld in the 1920's, it was only until 1963 that it could be realized, owing to the work of Frank Wanlass.

The bulk of this thesis deals primarily with process integration of metal gates on silicon-based devices and to a lesser extent with the introduction of so-called "high-κ" dielectric insulators. This thesis is more or less divided into two parts: development and integration of metal gate process flows for CMOS devices and the development of work function extraction methods, mainly electrical. Chapter 2 begins with a brief overview of the MOSFET,

discussing important parameters whose current relevance is highlighted, which is then followed by an overview of metal gate research and some of the latest device technology options for advanced CMOS. In Chapter 3, device processing is explained, with heavy emphasis on metal and dielectric deposition. Chapter 4 deals with electrical and physical work function measurements and presents the most important results from capacitor and device measurements. Throughout the chapter, some new results (unpublished data) and additional, more extensive discussions are presented with intent to complement the data in the appended articles. Chapter 5 concludes the thesis and provides a future outlook on the development of integrated devices, while the key achievements in the papers are listed in Chapter 6.

The research presented in this thesis has been conducted within the framework of the "High Frequency Silicon Program", which was financed by the Swedish Foundation for Strategic Research, and the SINANO (SIlicon-based NANOdevices) network, funded by the European Commission under the sixth EU framework programme for Research and Technological Development. The experimental work (processing and characterization) has been conducted mainly at the Ångström Laboratory in Uppsala, Sweden, in addition to excursions to the Royal Institute of Technology (KTH), in Kista, Sweden, and the Inter-University Microelectronics Center (IMEC), located in Leuven, Belgium.

2. CMOS gate stack development

The MOSFET

The metal-oxide-silicon field effect transistor (MOSFET) consists of four terminals, namely the source, gate, drain, and substrate (body). It is, in its very simplest form, a mere extension of the MOS capacitor, in which the gate electrode and the semiconductor channel constitute the parallel capacitor plates and the isolating oxide layer is equivalent to the dielectric material. A simple pMOS representation is shown in Figure 1.

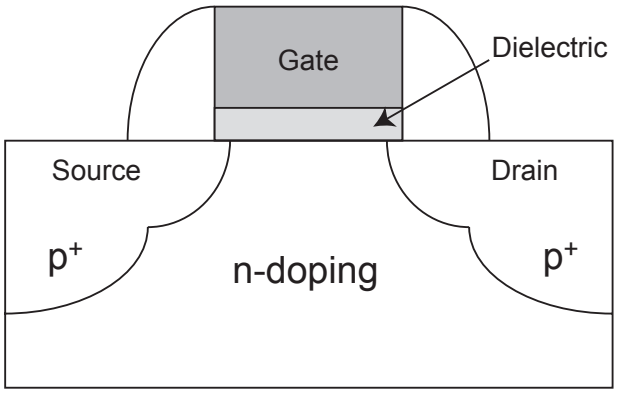

Figure 1. A typical pMOSFET.

The pMOS (nMOS) device is operated by setting a bias on the drain contact and using the gate voltage to control the flow of holes (electrons) from the source to the channel. The gate electrode controls the electric field; more specifically, when a negative voltage is applied, the Si surface region beneath the isolator becomes inverted to p-type and a current conducting path connects the source and the drain. The purpose of the gate oxide, usually thermally grown SiO_2, is to act as an energy barrier between the gate and the substrate in order to confine charge carriers in the channel.

There are several important parameters which govern the function of the transistor, whose relevance will be highlighted throughout this chapter. The drain current (I_d) specifies the current flowing in the channel, either in the

linear or saturated states, as illustrated in the pMOS case in Figure 2. The I_d expressions for the respective long-channel situations are given by Eq. 1 and 2 below [1].

$$I_d = \mu_{eff} C_{ox} \frac{W}{L} \left(V_g - V_t\right) V_d \tag{1}$$

$$I_{dsat} = \mu_{eff} C_{ox} \frac{W}{L} \frac{\left(V_g - V_t\right)^2}{2m} \tag{2}$$

The equations depend on the mobility of the charge carriers (μ_{eff}), the gate capacitance per unit area (C_{ox}), the channel length and width (W & L), the gate, threshold and drain voltages (V_g, V_t, and V_d), and the body effect coefficient (m).

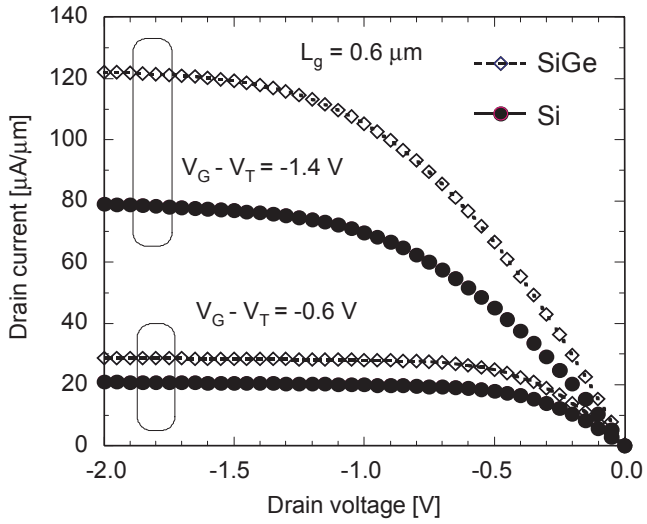

Figure 2. I_d-V_d characteristics of two different pMOS devices for two different gate overdrive voltages. SiGe devices display higher I_d due to improved channel mobility.

The threshold voltage (V_t), which is included in the above expressions and given by Eq. 3, is another parameter which is largely controlled by the characteristics of the gate electrode. V_T determines the minimum voltage over the gate required to achieve an inverted channel and hence the current in the ON and OFF states.

$$V_T = V_{fb} + 2\varphi_B + \frac{\sqrt{4\varepsilon_{Si} q N_A \varphi_B}}{C_{ox}} \tag{3}$$

The V_T expression includes the band bending in the substrate, or the potential difference between the intrinsic and substrate Fermi levels (φ_B), the permittivity of silicon (ε_{Si}), the electronic charge (q), and the channel dopant concentration (N_A). Finally, V_{fb} denotes the applied gate voltage that eliminates any band bending across the stack, given by Eq. 4, which includes

$$V_{fb} = \phi_{ms} - \frac{Q_{ox}}{\varepsilon_0 \kappa_{ox}} T_{ox} \tag{4}$$

the difference in work function between the gate electrode and the Si channel substrate (ϕ_{ms}), the amount of fixed charges in the dielectric (Q_{ox}), the permittivity in vacuum (ε_0), the dielectric constant (κ_{ox} = 3.9 for SiO_2) and the physical thickness of the isolator (T_{ox}). Eq. 4 thus shows that the work function of the gate electrode is primarily responsible for setting V_T.

$$\varphi_B = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{5}$$

The band bending in the channel (Eq. 5) is determined by Boltzmann's constant (k), the temperature (T), the channel doping concentration (N_A) and the intrinsic Si carrier concentration (n_i).

The drain current, or the velocity of charge carriers in the inverted channel, is proportional to the effective mobility μ_{eff}. In bulk silicon, electrons exhibit three times higher mobility than holes, since the electrons in the conduction band are much lighter than holes in the valence band. However, due to different scattering mechanisms such as Coulomb scattering, phonon scattering and surface roughness scattering, the mobility in the inversion channel is much lower compared to bulk silicon.

As the distance between the source and the drain regions is reduced with scaling, short-channel effects (SCE) degrade the performance of the device. SCE causes the drain voltage to affect the channel which means that the electric field over the gate does not control the inversion layer any more, and the threshold voltage is decreased. The problem is that the drain voltage starts to produce charges in the channel which means that a lower gate voltage is required to reach V_T. Other significant parameters such as oxide thickness (T_{ox}) and the channel dimensions (W/L) will be discussed later in the chapter.

CMOS Development and Scaling

The ever-changing scaling requirements for integrated circuits has for some time been dictated by the ITRS (International Technology Roadmap for Semiconductors) establishment [2]. It regularly posts a set of guidelines for the semiconductor industry, stating in great detail how the different sectors of semiconductor manufacturing will develop in the next 10-15 years. With increased scaling, both constant-field and generalized scaling, several key issues have arisen that require addressing in the near future. With decreasing oxide thickness (Intel's 65 nm CMOS process dictates a thickness (T_{ox}) of 1.2 nm [3], equivalent to about 5 monolayers of SiO_2), gate oxide leakage due to direct tunnelling becomes more significant. The obvious remedy is to replace silicon dioxide with an isolator that has significantly higher dielectric constant than 3.9, i.e. a high-κ dielectric. This will allow the device to operate using the same capacitance, but with a higher physical thickness that suppresses direct current leakage, and hence, lower power consumption. A directly related issue concerns the integration of metal gate electrodes, which are probably required for high-κ isolators, mostly for compatibility reasons. For metal gates, metal systems with the correct band-edge work functions are required in order to fully replace heavily doped polysilicon gates.

Metal gate overview

Introduction

Using a pure metal as a gate electrode is nothing new; early CMOS processes used aluminium gates in the 1970's. As scaling continued, n^+ polysilicon was used as a gate electrode instead due to its ability to withstand heat treatments necessary to activate the source and drain dopants. Another benefit is that the patterned poly-Si is employed as a mask when implanting the source and drain regions – the self-aligned approach. However, later process schemes switched to dual work function doped polysilicon gate in order to control the short channel effects and achieving specified threshold voltages.

In the late 1990's, metal gates once again became fashionable for a couple of reasons. First, metals do not exhibit the poly depletion effect, meaning that the lower portion of the gate is depleted when the channel is inverted, effectively increasing the EOT by 7-8 Å and adding a capacitance in series with the gate dielectric capacitance. Second, the vast majority of results indicate that regular poly-Si gates are not chemically stable in contact with high-κ dielectrics. Finally, the need to aggressively dope the poly-Si in order to decrease the resistance in short gate electrodes has resulted in boron

diffusing from the gate and penetrating the dielectric, ultimately degrading transistor performance. Early papers such as [4] discussed the need for metal gates at the 130 nm CMOS node, where TiN gated devices were shown with no polydepletion effects and very low resisitivity. The benefits of metals are obviously several. Metals do not require doping since they have excess electrons owing to their metallic nature. Although the resistivity of a metal may under optimized deposition conditions be significantly lower than in a highly doped poly-Si stack, it is not a requirement since modern gate stacks are already silicided at the top, which reduces the sheet resistance.

In order to alleviate the problem of poly depletion, polysilicon gates can be alloyed with germanium [5]. A solution to decrease the power dissipation due to direct tunneling, is to replace SiO_2 with a nitrided oxide (SiON), which suppresses dopant penetration and increases the dielectric constant [6]. While these technology extensions, combined with several generations of channel strain engineering, have certainly postponed the introduction of a metal gate/high-κ gate stack for several CMOS nodes, new materials will inevitably require introduction.

Metal Requirements & Selection

The primary requirement for a prospective metal gate technology is attaining correct work functions for setting symmetrical threshold voltages for nMOS and pMOS. The work function of the gate material is responsible for setting the threshold voltage of a CMOS transistor and equals 5.2 eV (4.1 eV) in a p-type (n-type) pMOS (nMOS) bulk Si transistor using heavily doped poly-Si gates. This means that the work functions of the metals must be equal to or close to those of the poly-Si gates being replaced. These specifications are somewhat relaxed for FD-SOI and FinFETs, 4.4 and 4.9 eV for nMOS and pMOS, respectively [7].

A key requirement (for a gate-first process) is also the ability to withstand source/drain dopant activation anneals, which is usually done at 1000 °C for 5 seconds. This means that the metal must be chemically stable with the chosen dielectric. Unfortunately, low work function metals are inherently very reactive and may react with both the top and bottom interfaces. High work function metals, on the other hand are usually chemically stable, but this trait causes integration concerns, such as etching and achieving high selectivity with regard to the underlying dielectric. In terms of overall device performance, a metal gate technology must maintain V_t stability, exhibit reliability comparable to poly-Si/SiO_2, and show a high frequency C-V hysteresis of less than 10 mV [7].

In addition to the basic electric requirements, there are integration issues which pose more restrictions. For examples, with present gate widths in the 20-30 nm range, line edge roughness (LER) needs to be addressed since many metals tend to corrode in the sidewalls during chlorine dry etching.

The minimum thickness required to set the work function also requires scrutiny. While some work [8] has already been done concerning ultra thin gate films, it is still unclear how tensile or compressive strain in the film may affect the gate stack properties. Other issues include the cost of the actual materials, the abundance of it in the earth's crust and possible purity issues. It is also essential that the metal and its associated by-products and waste may pass toxic regulations when being used.

Initially, the metal systems investigated consisted of those already being used in CMOS processing, such as diffusion barriers (TiN, TaN), BEOL metals (W), and lately source/drain metal silicides such as NiSi and CoSi. Owing to the limitations of these metals, more exotic material combinations have been studied, such as conducting metal oxides (MoO_2) [9], ternary nitrides and also doping fully silicided gates (FUSI) with lanthanide elements such as Yb [10].

One option that has attracted a lot of attention lately [11] is FUSI gate technology, which is basically a metal silicide that is created by first depositing a poly-Si layer, followed by capping with a metal layer and annealing it, which yields a certain silicide phase. The work function can be modulated by obtaining different silicide phases [12] and/or doping the polysilicon.

Integration

Several integration approaches have been suggested for implementing metals in a CMOS process flow, all with their own distinctive merits and disadvantages. The first involves (dual metal gate approach) depositing two metals, each with distinct work functions for nMOS and pMOS. The first metal is deposited after active area definition, then etched and finally the second metal is deposited and lithographically defined. While this method is simple to do, it means that the fragile dielectric is exposed to a potentially harmful etchant once. A variation is to completely strip the first dielectric layer after the first etch and deposit a new, perhaps different isolator for the second metal. Another technique uses a uniform layer of Metal 1, with a subsequent deposition of Metal 2, which is then selectively etched with regard to Metal 1. Finally, a high-temperature anneal forces Metal 1 & 2 to intermix, resulting in a different work function. This was successfully demonstrated for the Ru-Ta system [13]. It has also been shown that Mo can be modified [14] using N^+ implantation, similar to poly-Si modification. However, the resulting work function shift is not sufficient for band-edge work functions.

All of these methods follow the "gate-first" approach, meaning that the gate stack is deposited early in the process. An attractive alternative would be the "gate-last" scheme, in which a dummy gate stack is deposited, annealed, then removed and substituted with the proper dielectric and gate

electrode. While this method increases process complexity, it means that the thermal requirements are somewhat loosened. The benefits and disadvantages of all these approaches are discussed in [15].

High-κ dielectrics

As the MOSFET is continually being downscaled, above all the gate dielectric must be decreased according to the previously mentioned scaling laws. The present 65 nm CMOS technologies feature an oxide thickness of only 1.2 nm, which is equivalent to about 5 atomic layers of nitrided SiO_2. The leakage current due to direct tunnelling at this thickness is ~100 A/cm^2. However, for future technology nodes, it is anticipated that a high-κ dielectric will be used, i.e. a dielectric that keeps the same capacitance, but with a physically thicker layer that prevents excessive leakage due to direct tunnelling. This is especially important for low stand-by power (LSTP) applications, such as portable user electronics, where conserving power is of utmost importance whereas higher leakage may be tolerated for high performance (HP) devices, for example desktop CPUs.

Much research has been done lately on finding a suitable SiO_2 replacement. From a thermodynamic point of view it is well-known that most of the binary oxides and nitrides are unstable [16] in contact with silicon. Of the remaining compatible compounds, the oxides seem to possess higher dielectric constants than the corresponding nitrides. Currently, hafnium-based compounds are being investigated, but also the oxides of the lanthanoid elements such as La_2O_3 [17] and Dy_2O_3 [18]. A key problem lies in the fact that a high-κ dielectric must be *deposited* using either chemical or physical processes, which creates structural imperfections in the form of oxygen vacancies and contaminants. SiO_2, on the other hand, is *grown* on Si, forming a clean isolator that forms an atomically perfect interface with the Si channel. Another issue is the existence of an extremely thin interfacial layer of SiO_x between the channel and the high-κ dielectric. This interfacial SiO_x is present since Si oxidizes in air. However, this interfacial layer has been shown [19] to be a prerequisite for proper high-κ dielectric nucleation.

All these problems have a negative impact on the performance of high-κ devices. The imperfections in the isolator cause charges which affect the density of inversion charge carriers in the channel, thus degrading the mobility [20]. An advantage of the aforementioned interfacial SiO_x is that it minimizes the mobility degradation. Unfortunately, it also increases the overall EOT.

Present and future CMOS technology options

Regarding the integration of metal gates and/or high-κ dielectric insulators there is no clear consensus as of this writing (August 2006). A detailed overview of the issues surrounding the integration of high-κ/metal gate stacks is given in [21]. While fully silicided gates (FUSI) have been demonstrated to work [22] it may only be viable for one CMOS logic node since the technology suffers from Ni diffusion, limited work function tuning range and the existence of dual silicide phases. Also, a metal gate/oxynitride stack has been suggested [23], but it is more probable that further enhancements of drive current will be mainly due to refined strain engineering in the channel. While advanced nitrogen profiling may push the EOT towards 1.0 nm for HP logic devices, it is still only a short-term solution and it will do little to decrease heat dissipation. Metal gates and/or high-κ will probably not be introduced until the 32 nm node or beyond, when V_{th} instability issues expect to be rectified. However, the Nippon Electric Co. (NEC) has on several occasions stated that they intend to introduce HfSiON isolators for the intermediate 55 nm node, with dual work function NiSi gate electrodes. According to the latest version of the ITRS projection, the simultaneous integration of metal gates/high-κ dielectrics has been delayed until the 2008 time frame [2].

During the last couple of years, there have been several technology improvements that have maintained or even improved device characteristics without introducing entirely new material systems within the gate stack. Mechanical strain (compressive or tensile stress) has been implemented in the channel, which drastically improves channel mobility. Another technology that has gained widespread acceptance is silicon-on-insulator (SOI). SOI wafers consist of a thin layer of silicon (50 nm – 100 μm) which is deposited on an insulating substrate, for example SiO_2 on bulk silicon. Creating devices on SOI wafers is beneficial since SOI offers reduced parasitic junction capacitances, lower leakage currents and radiation resistance. However, the main advantage is that SOI offers the possibility to control short-channel effects. Apart from Ultra-Thin-Body SOI (UTB), SOI is also used for FinFET and other multi-gate MOSFET devices. All these device improvements have postponed the introduction of high-κ/metal gate stacks. There have also been many improvements on the circuit design level. For example, the latest device generation utilize new ways of circuit design such as sleep transistors [24] and prediction logic.

Transistor scaling limits

The penultimate limit of MOS gate length scaling is governed by fundamental quantum mechanics. The distance between the source and the drain regions in a field effect transistor must be larger [25] than the de Broglie wavelength of the electrons:

$$\lambda = \frac{\hbar}{\sqrt{2mE}} \tag{6}$$

In Eq. 6, ħ is defined as Planck's constant, m is the electron mass and E is the energy of the electron. If this requirement is not satisfied, the electrons will behave more like waves than particles and the device ceases to operate as an electrical switch. Thus, the minimum gate length is limited to the distance between individual atoms in the silicon lattice (0.27 nm) as well as the uncertainty principle limiting device parameters such as current and voltage.

Beyond the ever-present physical limit, there are other factors that may prevent further scaling. Since building a new facility (or perhaps upgrading an existing one) for each new device generation is a huge investment, it may not be economically viable to continue device miniaturization. Historically, the semiconductor manufacturers have been pessimistic concerning solving potential show-stoppers such as lithographic hurdles, but they have always been resolved. However, problems such as line edge roughness will become serious and also have a significant impact on transistor noise margins.

3. CMOS Processing

The development of processing techniques for manufacturing ever-shrinking integrated circuits is the key to producing faster devices. The purpose of this chapter is to briefly review those deposition methods considered for depositing a high-κ/metal gate stack and which have all been employed in the appended papers. The techniques either use the concept of physical vapor deposition (PVD) or based on chemical reactions (ALD and MOCVD). All are capable of creating metallic or isolating films. Finally, a short description of material etching mechanisms will be provided.

Introduction

The integrated circuits being manufactured today are processed on 300 mm Si wafers. Figure 3 illustrates how the number of on-wafer dies increased simply by making the transition from older 200 mm-wafers.

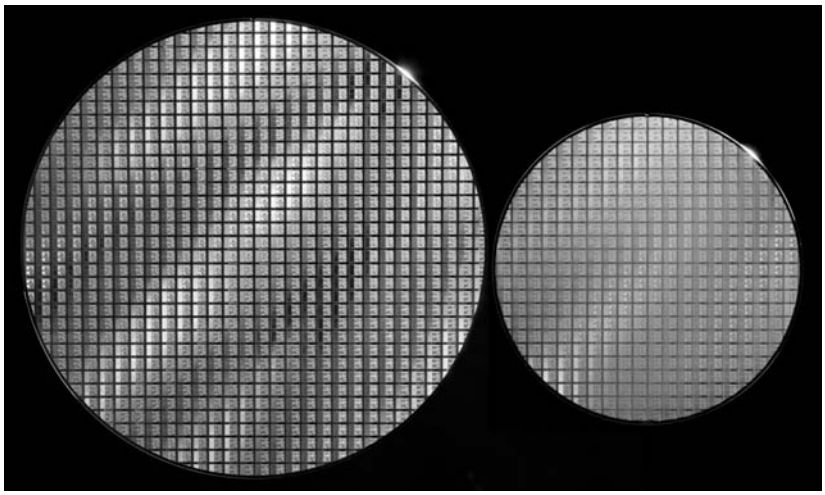

Figure 3. Identical dies created on both 300-mm wafers (left) and 200-mm wafers (right). (Copyright AMD 2006).

Integrated circuits are basically made by sequentially depositing materials (isolators, metals, photoresist) and selectively (lithography) removing

(etching, polishing) certain areas of the deposited thin films. Atomic species can also be introduced in the subsurface region of the wafer using accelerated ions or diffusion (implantation).

PVD

Physical Vapor Deposition (PVD) is a physical deposition process. It is a derivative of basic evaporation processes, while sputtering (and specifically magnetron sputtering) is by far the most widely used PVD process today. While magnetrons can assume many different configurations, the most widespread one is a flat, circular plate onto which the source material (target) is bolted. An inert gas (usually argon) is purged into the chamber and the plasma is then ignited by applying bias to the target. Ionised Ar^+ particles are attracted to the target, which hit it and eject metal species in the other direction. In the reactive mode, a reactive gas (typically nitrogen or oxygen) is let into the chamber. With increasing N_2 flow, a nitride of the desired material is built up on the target surface, so-called racetrack poisoning. At a certain flow, a stoichiometric phase of the desired compound is formed, which is continually being deposited on the substrate surface. The option of varying the nitrogen flow to control the metal work function was the basis for Paper I-IV. PVD is mainly used to deposit metal gates, and to a lesser extent isolators, owing to uniformity issues. The benefits of PVD include high film purity, high deposition rate and the ability to tailor film characteristics such as texture, stoichiometry and resistivity simply by altering deposition parameters like pressure, current and gas flows. A disadvantage of PVD is that the physical bombardment can erode the dielectric surface, thus increasing the roughness of the dielectric/metal interface as well as cause charge trapping, both of which can lower device performance. It is also a very directional deposition process which translates into poor step coverage. PVD deposited metals, in their work function defining role, were used in Papers I-VII.

ALD

Atomic Layer Deposition (ALD, previously designated Atomic Layer Epitaxy) is a chemical deposition method in which the resulting film is formed by pulsing two gases (the primary one is called the precursor) into the sample chamber, which react and form a thin layer of the desired film on a substrate. A combination of pulses is referred to as a *cycle*. A common misconception is that atomically uniform layers are deposited during each cycle. In reality, however, it takes a number of cycles to form a single monolayer (ML) and even higher number of cycles to form a fully closed

film during the initial growth on a surface. This is in part due to the fact that initial nucleation exhibits a non-linear behaviour as was shown in [26]. In gate stack research, ALD is extensively used to manufacture high-κ oxides in addition to metal gate films. ALD offers excellent uniformity over large areas and control of film thickness on an atomic level. ALD deposited films were used in papers VI, VIII and IX.

MOCVD

Metal-organic chemical vapor deposition (MOCVD) is a CVD process which uses metal-organic precursors to generate the desired materials. For example, tetra-dimethyl-amino-titanium (TDMAT) is used to form TiN. MOCVD deposited isolators are demonstrated in Paper V.

Etching

Etching is a process in which material on a wafer is selectively removed by means of a hard mask. It can be done either using wet chemical etching or dry plasma etching. In the case of dry metal etching, the process can be divided into chemical and physical etching. Chemical processes indicate that the gases react with the metal species, forming volatile waste gases that are pumped out of the system. Physical etching, on the other hand, means that molecules from the constituent gases are physically accelerated towards the metal, hence sputtering away material. This is especially useful when the exposed metal is very inert and cannot be etched chemically, for example heavily oxidised metal surfaces. Dry etching is a complex process and is usually a combination of both physical and chemical etching, where the combined etch rate can be substantially higher than each etch rate separately. While it is possible to wet etch TiN using a heated SC-1 (RCA1) solution (H_2O, NH_3 & H_2O_2), the majority of the devices presented in this thesis have been dry etched for simplicity and process integration relevance.

4. Characterization methods and results

Electrical and physical characterization of processed capacitor structures and transistors are a significant part of the gate stack research. In this chapter, several different work function extraction methods will be presented along with the results obtained using different gate stack configurations. Electrical and physical means of determining the metal work function will be presented and compared with each other. Finally, results obtained from pMOSFETs will be presented along with processing details and the effects of water vapor annealing.

Electrical work function extraction methods

The work function of a metal or metal compound is defined as the minimum energy required to extract an electron from the crystal lattice of the metal to vacuum. In order to screen the suitability of a metal gate candidate, processed devices are usually not necessary since capacitors yield a sufficient amount of information in terms of equivalent oxide thickness (EOT), flatband voltage, barrier heights and doping.

Capacitance-voltage (*C-V*)

Capacitance measurements is by far the most popular method to screen potential metal gate candidate materials, since it is a rather straightforward method which provides a lot of information requiring only a simple measurement, but is also prone to measurement-induced errors. Capacitance-voltage measurements require a capacitor, which is equivalent to a MOSFET (Figure 1), but lacking the implanted source/drain regions. When the gate voltage is varied, the capacitance varies due to accumulation, depletion and inversion of charge carriers in the silicon substrate near the SiO_2 interface. A typical set of high-frequency (10 kHz) *C-V* curves is shown in Figure 4. The capacitance extremes of accumulation and inversion are used to calculate the equivalent oxide thickness (EOT) and doping density, respectively. The flatband voltage is defined as the gate voltage which causes no band bending in the silicon and was given previously by Eq. 4:

$$V_{fb} = \phi_{ms} - \frac{Q_{ox}}{\varepsilon_0 \kappa_{ox}} T_{ox} \tag{7}$$

Ideally, the flatband state should occur at zero applied gate voltage, but due to charges in the oxide and more importantly, a work function difference between the gate and the silicon, the flatband voltage can be shifted according to Eq. 7. The charges can be classified [27] into four distinct types. The interface trapped charge (Q_{it}), located in the Si/SiO_2 interface, can be either positively or negatively charged and are electrically active due to interaction with the silicon substrate. The positively charged fixed oxide charge (Q_f) exists in the oxide or close to the silicon and is not electrically active. Positive or negative oxide trapped charges (Q_{ot}) are distributed in the oxide and are electrons/holes trapped due to x-ray radiation or hot-electron injection. Mobile ionic charges (Q_m) are caused by ionic contaminations, such as sodium and are mobile in response to bias-temperature conditions. This last type is not significant today, with the advent of modern ultra-clean furnaces.

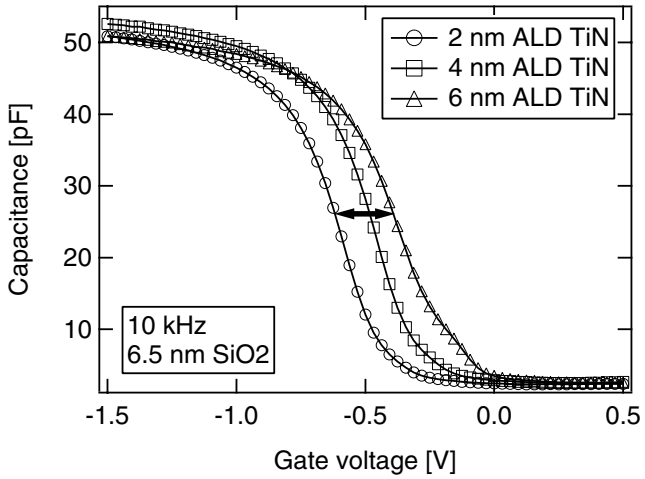

Figure 4. A typical high-frequency *C-V* measurement. The curves represent different interfacial chemistries.

A very simple approach is to measure the capacitance as a function of the applied gate voltage which is then compared to another *C-V* measurement, but with a reference metal instead whose work function is known. The work function is determined by measuring the voltage offset which is equivalent to the work function difference and then added or subtracted to the reference metal work function. However, even if similar wafers are used, the two different metals may yield different density of oxide charges after

deposition, exhibit different reactivities with regard to the dielectric and could be susceptible to varying degrees of contaminant diffusion through the metal plate. Another approach is to just extract the flatband voltage from a single measurement which is then said to equal the work function difference between the metal and the silicon. However, this approach assumes that the oxide charge is nil, which is far from apparent, even on very thin SiO_2 and after post-metallization anneals.

The V_{fb}-EOT (flatband voltage – equivalent oxide thickness) method is probably the most widespread method for extracting the electrical work function of a metal. When used, a capacitance sweep is measured as a function of voltage over the capacitor. Using the measured capacitance values in accumulation and inversion, the EOT, flatband voltage, and surface doping values are calculated. In order to extract the difference in work function between the metal and the silicon surface, a set of several different oxide thicknesses are required to extrapolate its magnitude, which is defined as the y-axis intercept. A typical V_{fb}-EOT plot of different samples is shown in Figure 5. The slope thus corresponds to the density of fixed oxide charge, which is given by Eq. 7.

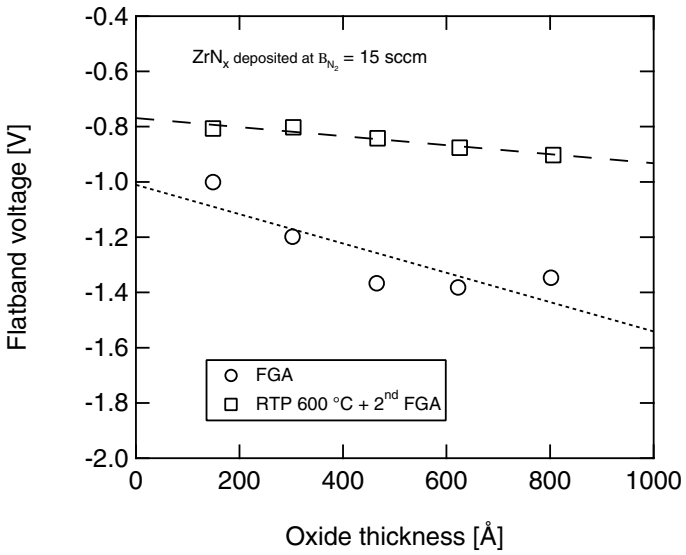

Figure 5. V_{fb} vs. EOT plot for ZrN_x/SiO_2. The accuracy is very dependent on the quality of the linear least-squares fit.

While the method is very straightforward to use and yields results quickly, it has several drawbacks, the most notable being the assumption that the oxide charge is constant. It is very much possible that the charge density varies when comparing wafers with different oxide thicknesses. Also, the precise measurement of the oxide thickness is prone to errors, which necessitates

quantum-mechanical corrections after measurement. For very thin oxides, parasitic capacitance due to contact pads as well as contributions from the measurement equipment (cables, switching matrices, equipment calibration) requires constant monitoring. When measuring the capacitance of high-κ oxides, in reality two dielectric films are being measured: the interfacial SiO_x and the deposited high-κ film. It has been shown [28] that both charge distributions may be estimated by measuring a high-κ series on constant thickness interfacial SiO_2 *and* a SiO_2 series capped with a layer of constant thickness high-κ. This approach does mean that numerous test wafers need to be processed, in addition to the increased number of required measurements.

The main benefit of using a single wafer is that a constant Si/SiO_2 charge can be maintained across all thicknesses, in addition to minimizing the necessary number of processed wafers. However, in spite of these nuisances, it is still the only valid method when screening metals on bulk high-κ layers. The benefits also include the ability to measure the density of interface states, a parameter which very much defines the suitability of a high-κ dielectric. However, in order to correctly assess the metal work function when deposited on a high-κ dielectric film, one needs to consider the presence of the interlayer SiO_2, which adds to the several different charge distributions.

Current-voltage (*I-V*)

The purpose of the gate dielectric is to prevent any gate current from flowing; however, for very thin isolators subjected to high electric oxide fields, different currents arise. The metal work function can then be determined by measuring the current through the gate stack in response to the applied voltage polarity. Depending on the gate stack configuration, different current transport mechanisms can be used to extract the metal work function. In general, these methods only apply to SiO_2 capacitor stacks, where Fowler-Nordheim (F-N) measurements are the most established.

Fowler-Nordheim tunnelling is a quantum-mechanical current transport mechanism which describes the transport of electrons from the gate electrode into the conduction band of the oxide. It occurs when the thickness of the isolator ranges from 5 to ~30 nm. The tunnelling current density [29] is given by

$$J_{FN} = AE_{ox}^2 \exp\left(\frac{-B}{E_{ox}}\right) \tag{8}$$

The parameters A and B are defined as

$$A = \frac{q^3 \left(m_0 / m_{ox} \right)}{8\pi h \phi_B} \tag{9}$$

$$B = \frac{8\pi \sqrt{2 m_{ox} \phi_B^3}}{3qh} \tag{10}$$

where ϕ_B either represents the metal/SiO_2 barrier or the SiO_2/Si barrier. The method relies on measuring the gate and substrate injection current through a MOS capacitor. The electric field over the oxide needs to be sufficiently high in both directions in order to reach the tunnelling regime, which is roughly 10 MV/cm. This means that the oxide needs to be of high quality; otherwise it will fail prior to the onset of tunnelling. When extracting the metal work function, the electron affinity for SiO_2 (0.9 eV) needs to be added to the extracted metal/SiO_2 barrier height. Figure 6 illustrates how the gate/substrate currents behave in the tunneling regime, while Figure 7 shows the same data as a Fowler-Nordheim plot.

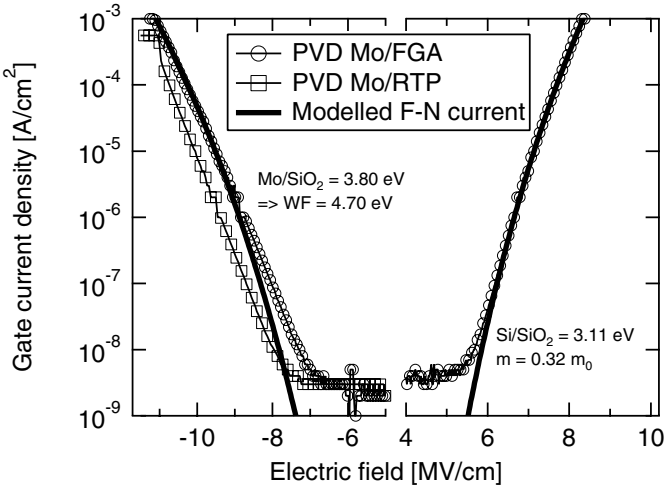

Figure 6. I-V measurements of a 100 nm Mo/20 nm SiO_2 stack in the tunneling regime, showing both gate and substrate injection.

Such a plot will show a straight line (equivalent to the parameter B) if the main conduction mechanism through the oxide is Fowler-Nordheim tunnelling.

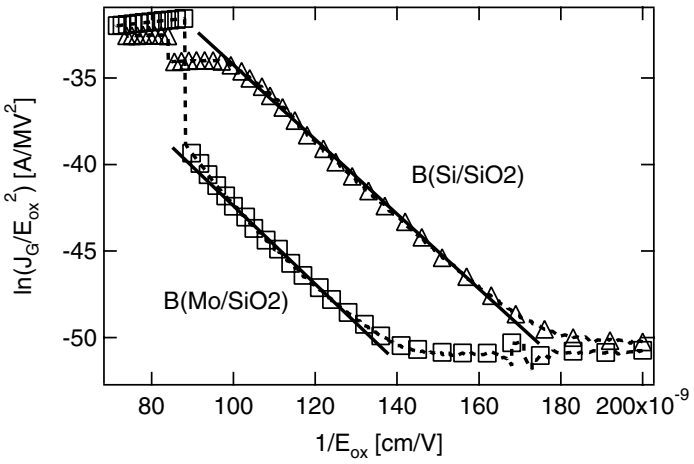

Figure 7. F-N representation of Figure 6. Both currents obey the theoretical linearity.

When fitting the measured *I-V* curves to the theoretical data, several parameters have to be estimated. The Si/SiO_2 barrier is usually considered to always be 3.12 eV and should be constant, irrespective of thermal budget and gate stack constituents. The electron effective mass, on the other hand, may vary considerably depending on the chosen theoretical model [30]. The electric field can deduced from a *C-V* measurement, taking into account the flatband voltage and the oxide thickness.

MOSFETs can also be used to perform precise Fowler-Nordheim tunnelling. However, those devices are obviously more complex than capacitors and are usually not considered as a test vehicle. In addition to the F-N conduction mechanism there is direct tunnelling, where electrons tunnel right through the isolator, which occurs if the oxide is thinner than 4-5 nm. While seldom used, this phenomenon can also be used to determine the barrier heights [31].

Results from capacitors

In essence, Paper I-IV demonstrate that reactive sputtering can be used to deposit metals whose work functions roughly equal those of n+/p+ polysilicon. More specifically, it is the flow of reactive gas (nitrogen) that alters the work function of the gate electrode. TiN was chosen since it had been reported previously [32] that the TiN work function could be modulated by implanting nitrogen ions. In Paper II, it was shown that increasing the flux of reactive nitrogen gas causes a corresponding increase in the flatband voltage of TiN, obtained from capacitor measurements. The

transition from metal to compound mode (10-11 sccm N_2) agrees well with a sharp increase in the flatband voltage, as is shown in Figures 8 and 9.

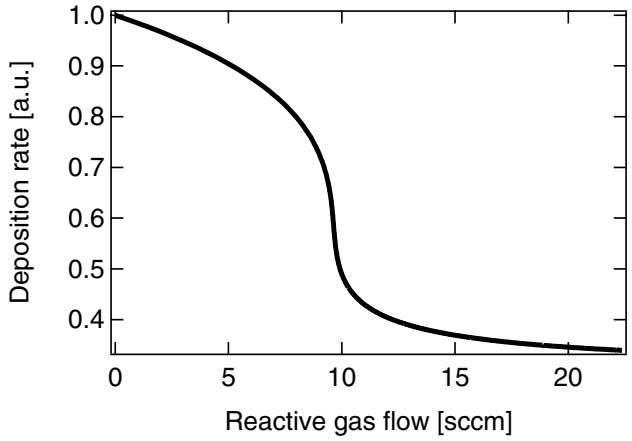

Figure 8. A simulation of the TiN deposition process, depicting the deposition rate as a function of applied reactive gas.

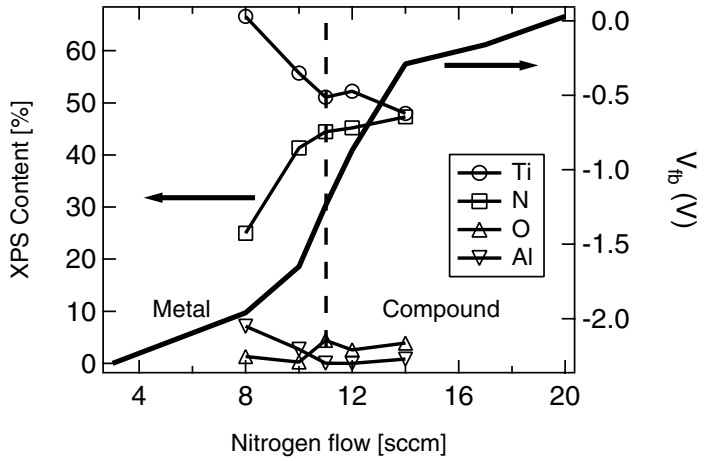

Figure 9. V_{fb} increase due to increased N_2 flow. Compound mode sets in at 11 sccm N_2 which coincides well with the acquired XPS depth profile.

The curve in Figure 8 was obtained by using the steady-state balance equations of reactive sputtering, as presented in [33], for given parameters such as current, target/substrate area and sticking coefficients. As the target surface is gradually being poisoned with increasing reactive gas flow, the deposition rate drops sharply, which the simulation confirms. These data also agree well with XPS (X-ray Photoelectron Spectroscopy, also labelled Electron Spectroscopy for Chemical Analysis (ESCA)) measurements on

aluminium-capped sheet metal samples deposited simultaneously with the capacitor wafers, as Figure 9 shows. A stoichiometric TiN film is obtained at 11 sccm N_2; the slightly higher Ti concentration is due to preferential sputtering during the XPS depth profiling.

In a similar manner, it was demonstrated that the work functions (on thermally grown SiO_2) of PVD TiN_x and ZrN_x could be tuned 0.7 eV by altering the nitrogen flow alone. Figures 10 and 11 illustrate how the work function is modulated for both binary nitrides, after FGA and annealing. While the results obviously mean that dual deposition steps are required, it could be possible to selectively perform N^+ implantation into a nitrogen-deficient film, thus acquiring dual metal work functions, reminiscent of the complementary poly-Si process.

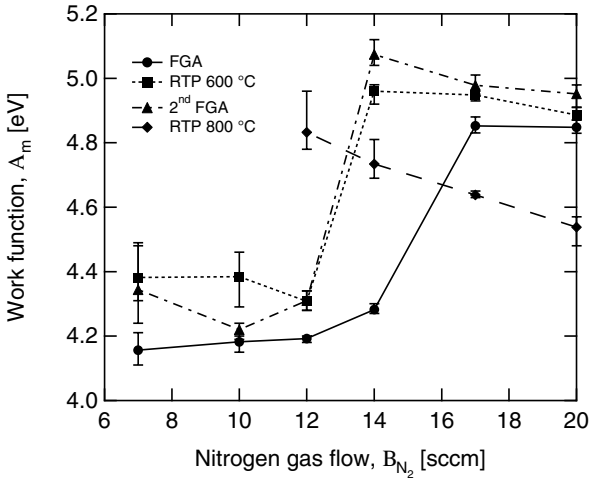

Figure 10. The work function (*C-V*) of TiN_x.

For both metal nitrides, the extracted work function is affected following high-temperature annealing, which is done to examine the effects of junction activation. As the figures show, the two binary nitrides respond somewhat differently. In the case of PVD TiN_x, the work function increases for Ti-rich films, while it decreases for TiN gates deposited at high nitrogen flows. This last behaviour is similar to the response of ALD TiN [34], where the work function also decreases with increasing thermal budget. Also, it seems that very nitrogen-deficient TiN_x gates are unstable when annealed at temperatures in excess of 600 °C, due to reaction with SiO_2. For ZrN_x/SiO_2 capacitors, the work function increases ~0.2 eV irrespective of N_2 flow (compound mode occurs at 14 sccm N_2).

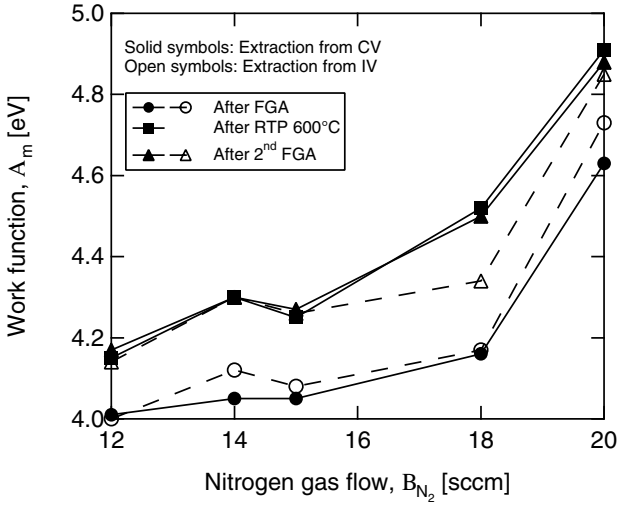

Figure 11. The work function (*C-V* and *I-V*) of ZrN_x.

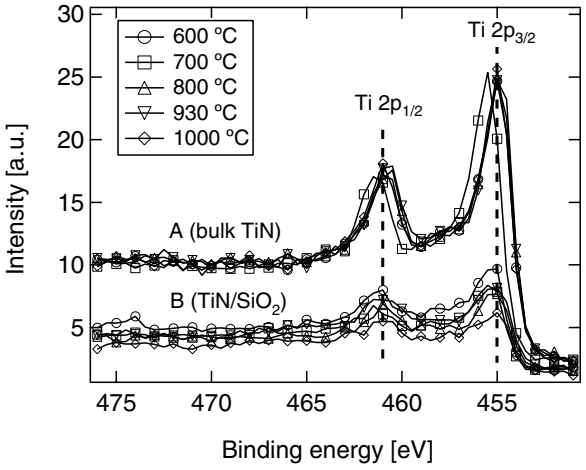

Figure 12. XPS data from sputter depth profiling, showing the energies of the Ti 2p binding states at different depths.

In order to examine the mechanisms responsible for the work function changes after thermal treatment of stoichiometric TiN, XPS depth profiles were taken from several samples annealed at different temperatures. Figure 12 depicts the positions of the Ti 2p peaks in the bulk of the film and very close to the TiN/SiO_2 interface, respectively. While the work function decreased with increasing RTA temperature, there is evidently no change in the position of the Ti 2p peak, either in the film or in the interface. Although

the nitrogen content did seem to vary depending on RTP temperature, the data was not consistent enough to justify a conclusion, very much due to preferential Ar sputtering of lighter elements such as nitrogen. Further HRTEM (high-resolution transmission electron microscopy) and XRD (x-ray diffraction) analysis did not yield any clarifying answers with regard to work function variations (see Paper III).

A modification to regular Fowler-Nordheim tunnelling was also presented, utilizing highly doped p-type substrates. The degenerate doping facilitates substrate injection, which usually requires light (photons) to generate carriers, and causes band-to-band tunnelling of electrons from the substrate. The method was applied to several capacitor combinations of ALD & PVD TaN/increasing ALD HfO_2 thickness/SiO_2; the PVD results are illustrated in Figure 13.

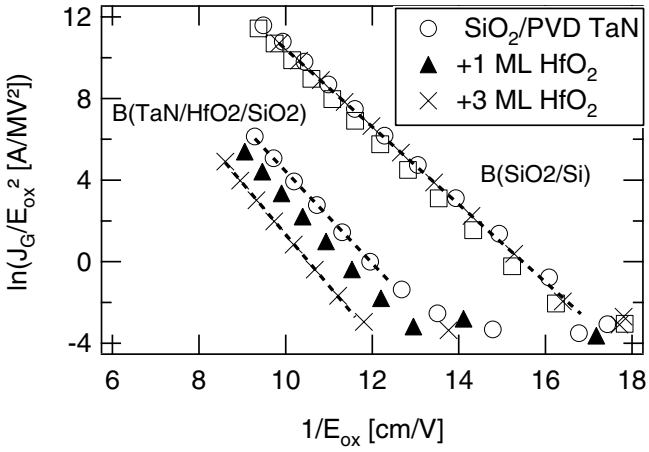

Figure 13. Fowler-Nordheim plots showing a stable Si/SiO_2 barrier while the TaN/SiO_2 barrier increases with inserted ALD HfO_2 monolayers

The consistent slopes (Eq. 10, "B" parameter in the F-N expression) mean that the effective electron mass can be cancelled out when estimating the metal work function. Since B_{TaN}/B_{Si} is proportional to $\phi_{TaN/SiO2}/\phi_{Si/SiO2}$, only the slopes and the Si/SiO_2 barrier height (~3.1 eV) are needed to determine the TaN work function by adding the electron affinity for SiO_2 (0.9 eV). The extracted values are summarized in Table 1. In the case of thicker high-κ films, Fowler-Nordheim is usually not applicable mainly because the conduction mechanism is not well known and it is not obvious how to relate the barrier with the correct metal work function.

Paper VI also describes experiments done on ultrathin ALD TiN gate electrodes capped with PVD TaN. The purpose was to study how very thin (2-6 nm) metal films set the work function. Figure 14 shows the results from

V_{fb}-EOT measurements, where the work function increases ~200 meV with thickness. Aside from the 20 nm SiO_2, the oxide charge density was very low, which accounts for the horizontal slopes. The 2 nm ALD TiN film is expected to be non-continuous due to island-like nucleation [26] and is probably a mixture of TiN and TaN which sets the work function. The work function increase was also confirmed with F-N measurements (Figure 15).

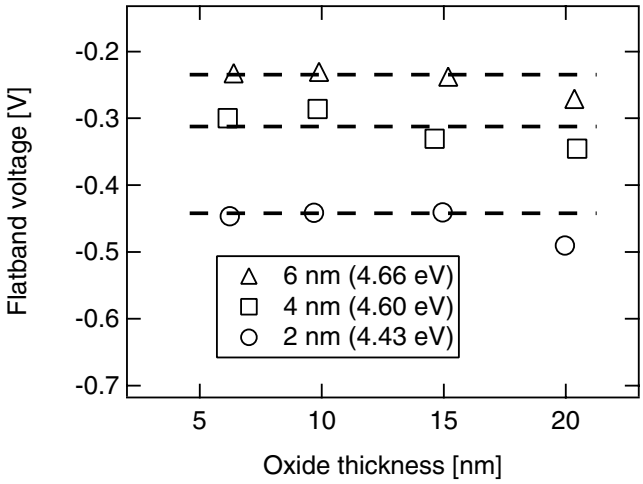

Figure 14. Results obtained from SiO_2/ALD TiN/PVD TaN capacitors. The 20 nm SiO_2 has been omitted from the ϕ_{ms} estimation owing to passivation issues.

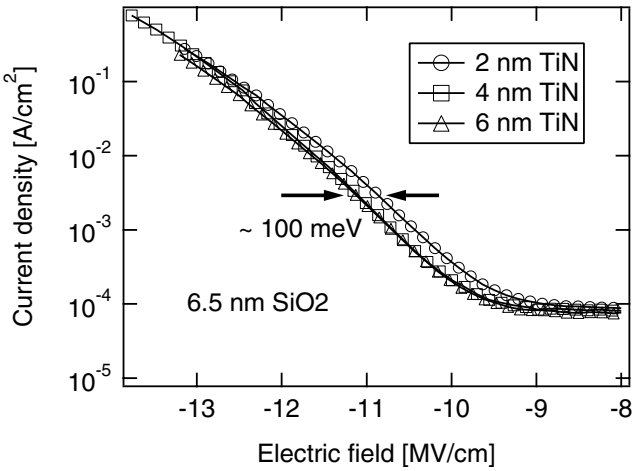

Figure 15. F-N measurements (gate injection) on the same data set as in Figure 14. The barrier shift is primarily due to the island-like deposition of the 2 nm ALD TiN.

In Paper VI, PVD Mo & TiN/MOCVD ZrO_2 & HfO_2 capacitors were fabricated with a 900 °C thermal budget. However, *C-V* and *I-V* measurements revealed an EOT increase and rather high leakage current after activation annealing. This deterioration is mainly attributed to crystallization of the high-κ dielectric after RTP, as was revealed by HRTEM analysis (Figure 16).

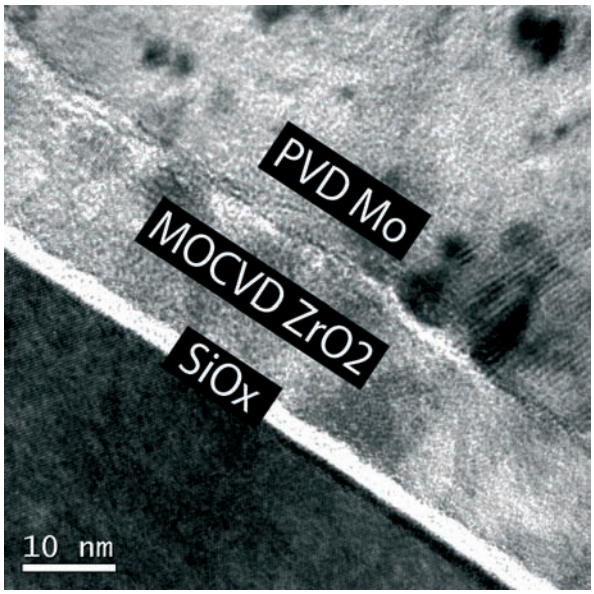

Figure 16. HRTEM micrograph of PVD Mo/MOCVD ZrO_2 gate stack. Note the presence of an interfacial SiO_x layer.

The presence of the interface layer is probably due to the 650 °C PDA after MOCVD deposition. It was also seen in another sample not subjected to RTP. It should be mentioned that higher forming gas temperature (520 °C) can improve the passivation of the metal gate/oxide interface, which was seen in [35].

Physical work function extraction

Internal Photoemission

Internal Photoemission (IPE) is a method to determine the work function of a metal in contact with a dielectric material. A capacitor structure is required where the metal electrode is thin enough to be semitransparent, which is then exposed to ultraviolet light whereas the photocurrent is measured. If a

negative gate voltage is applied, electrons are excited from the metal into the oxide and the metal/dielectric barrier height is extracted. In the case of reverse polarity, the semiconductor/oxide barrier is determined instead. The IPE capacitors are processed somewhat differently for a number of reasons. First, the metal has to be very thin (~10 nm) in order to be transparent to light. The dielectric must be rather thick (low leakage) since the small photocurrent should be dominant. Finally, the patterned metal plates need to be rather large since a large photocurrent is required.

Kelvin probe Force Microscopy

Kelvin probe Force Microscopy (KFM) is a non-contact variant of atomic force microscopy (AFM) which can be used to measure the local work function on a metal surface. Measurements are performed by pointing a probe, or reference electrode, close to the metal surface which then forms a capacitor with the surface. The work function is then estimated by measuring the potential offset between the probe tip and the surface. This assumes that the exact work function of the probe has been characterized with a classical Kelvin Probe.

Results from capacitors and sheet metal samples

In order to compare Fowler-Nordheim tunnelling with internal photoemission, a combination of gate stacks (highly doped capacitors and IPE samples) were prepared. In the table below, the results are listed for different combinations of ALD and PVD TaN, deposited on thermal SiO_2 and non-continuous ALD HfO_2.

Table 1. *Summary of work function measurements obtained using F-N tunneling on degenerate substrates and internal photoemission measurements.*

PVD TaN	*SiO_2*	*+1 ML HfO_2*	***ALD TaN***	*SiO_2*	*+1 ML HfO_2*
F-N	4.4 eV	4.5 eV	**F-N**	4.8 eV	4.9 eV
IPE	4.4 eV	4.5 eV	**IPE**	4.65 eV	4.85 eV

As is apparent, both F-N and IPE measurements agree very well. The two deposition methods differ since the PVD process generated a Ta-rich film while the ALD chemistry yielded a nitrogen-enriched metal.

As another example of benchmarking the validity of different work function measurement methods, Figure 17 summarizes the results from KFM and *C-V* measurements made on several PVD metals deposited on thermally grown SiO_2.

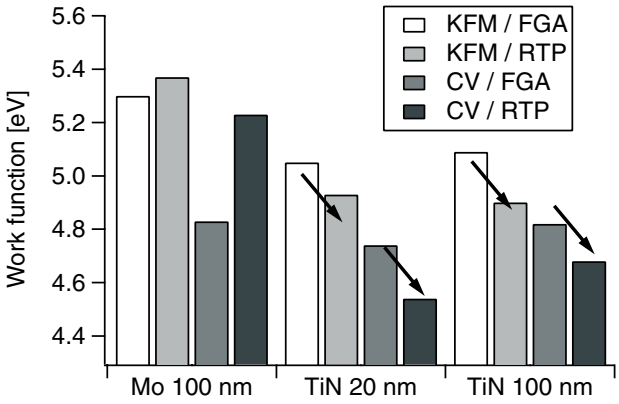

Figure 17. The work function of PVD deposited metals before and after high-temperature annealing. Note that the TiN work function seems to increase with thickness.

It is important to realize that the results show the two ends of the metal: KFM measures the local work function on the *surface*, while *C-V* senses the average work function at the metal/dielectric *interface*. Still, both methods sense a lowering of the TiN work function after RTA 900 °C (N_2, 10 sec.), similar to the results obtained in Paper I, which may be due to extrinsic states. The KFM response to molybdenum is probably due to the existence of conducting MoO_x on the surface.

Discussion on the metal work function

It has been demonstrated that the metal work function is widely dependent on the deposition conditions. A few of the possible mechanisms behind intentional or unintentional work function modulation will be discussed here.

One explanation is based on Fermi level pinning due to the presence of a high density of extrinsic interface states. These states can manifest themselves as lattice vacancies, changes in chemical bonding or texture variations. This model was used in [36] to show that the majority of metal gates, both on SiO_2 or high-κ, reach midgap values after high-temperature activation anneals.

When dealing with the reactively sputter deposited TiN_x and ZrN_x films deposited at intermediate gas flows, the work function increases after annealing. During ZrN_x processing it was observed that thinner films exhibited a more metallic color while thicker samples had an obvious golden hue. This indicates that there may be a N_2 gradient within the film. Since the only difference between the samples was the deposition time, it is possible that the removal of the shutter causes a change within the plasma and a short

time interval is required to pass before a steady state is attained yet again. This transient phenomenon could also apply to the PVD TiN experiments, since a similar scheme was involved: pre-sputter in Ar, pre-sputter in N_2+Ar, and finally open the shutter with the substrate directly below the plasma. Subsequent annealing may cause nitrogen diffusion to the metal/SiO_2 interface, thus increasing the work function.

Characteristics of SiGe devices

Processing of ALD metal gate/high-κ/strained SiGe pMOSFETs

A few processing details of the devices characterized in Paper VIII and IX were omitted and are presented here. The integration of metal gate, high-κ dielectrics and channel strain was demonstrated by manufacturing suitable pMOSFETs. After ALD deposition of the different high-κ layers, 10 nm of work function-setting ALD TiN was deposited. As a gate contact, 180 nm of PVD TiN was employed (Ti:N ~1:1). After hard mask patterning, the gate fingers were dry etched in an ICP chamber using a Cl_2/BCl_3 plasma. Figure 18 show a typical device after metal etch, whereas Figure 19 shows a fully processed device after final metallization. While the dielectric seems to be unharmed, there is still some residue from the dry etching left on the dielectric, or possibly remaining TiN grains.

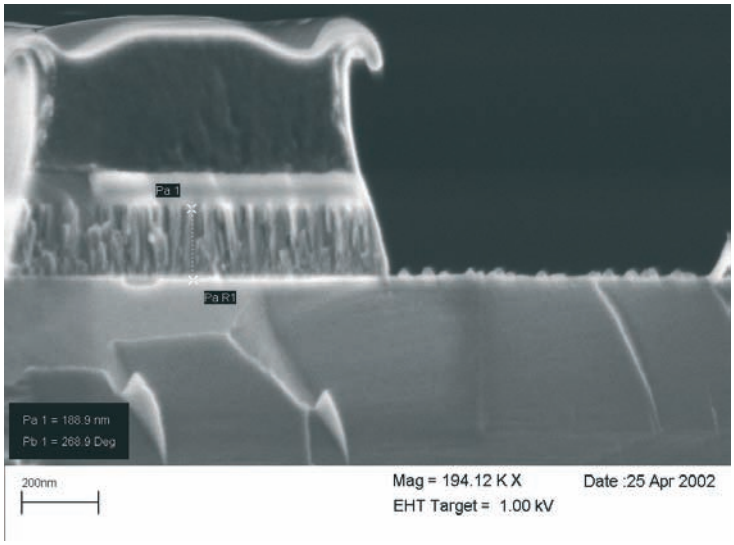

Figure 18. Slightly slanted TiN gate finger sidewall after dry etch. Note etch residue to the right.

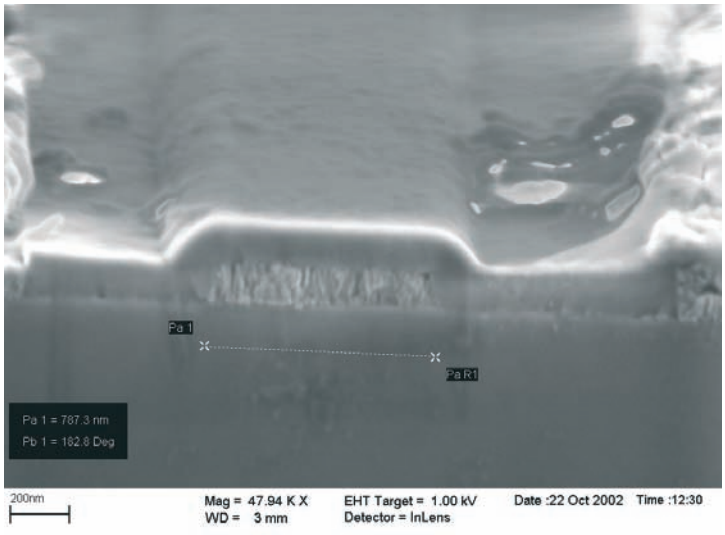

Figure 19. Cross-section of metal gate/high-κ pMOSFET.

Device characteristics and H_2O anneal response

The ALD $TiN/Al_2O_3/HfAlO_x/Al_2O_3$/strained-$Si_{0.7}Ge_{0.3}$ pMOSFETs demonstrate vastly improved device characteristics compared to the Si channel reference. As can be seen in Figure 20, the current drive and peak transconductance is more than 30% higher than the Si device.

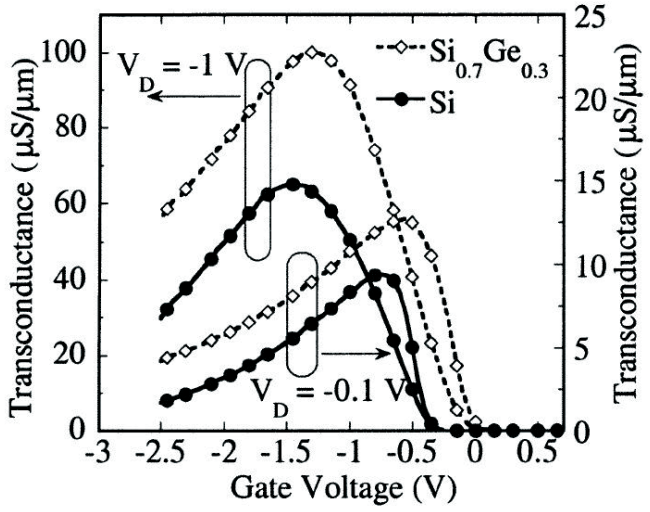

Figure 20. g_m vs. V_G for the $Si_{0.7}Ge_{0.3}$ and reference device.

Capacitance measurements revealed an EOT of 2.8 nm for the entire gate dielectric and showed no evidence of poly-depletion as a consequence of the TiN (ϕ_m=5.0 eV) gate electrode. However, in spite of these improvements, a large subthreshold slope and threshold voltage shift was detected, indicating a high density of interface states as the main culprit. Since it was reported in [37] that the SiO_2/SiGe interface could be improved, sequential (30 min.) water vapor anneals were conducted at 300 °C for the ALD TiN/Al_2O_3/s-$Si_{0.8}Ge_{0.2}$ devices. It turned out that after a few hours of H_2O treatment, the threshold voltage decreased by several 100 mV, finally saturating after 2-3 hours of vapour treatment, see Figure 21.

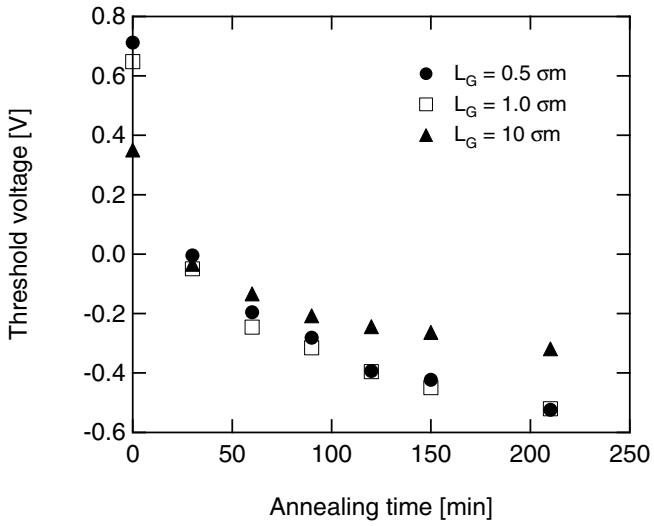

Figure 21. V_t decrease with time for $Al_2O_3/Si_{0.8}Ge_{0.2}$ devices.

Another benefit of H_2O annealing is that it has a positive impact on the 1/f noise characteristics [38] (same device set as previously described). Finally, there are several reports of metal gates being advantageous in terms of reducing the 1/f noise, compared to poly-Si gate electrodes [39].

5. Conclusions

The goal of this thesis has been to primarily address the scaling limitations imposed by the present use of poly-silicon gate electrodes. Possible paths to achieving a metal gate/SiO_x or metal gate/high-κ gate stack are shown, accompanied by several different methods to quantify the metal work function. Since the introduction of metal gates is highly related to the imminent transition to high-κ isolators, devices are shown showcasing the benefits of both technologies in addition to present-day CMOS processing concepts such as channel strain.

Current trends indicate that hafnium-based compounds have been chosen as the next-generation gate dielectric, probably alloyed with either Si or N or a combination of both. There is no clear consensus concerning metal gate integration. However, the prospect of incorporating a metal or perhaps FUSI electrode on regular SiON in order to eliminate gate depletion is an option for several manufacturers.

As for engineering the work function of the gate electrode, a tunable technology has been demonstrated for PVD TiN_x and ZrN_x which is based on varying the nitrogen flow during deposition. In both cases, the work function can be tuned to obtain a span of roughly 0.7 eV, almost satisfying the requirements for band-edge work functions. However, this changes drastically after activation anneals – in most cases the work function reaches midgap values and also requires stoichiometric films in order to ensure chemical stability. While the variation in work function for as-deposited TiN_x has been proven with XPS, no physical analysis method can explain the work function changes after high-temperature annealing, although Fermi level pinning at the metal/dielectric interface is believed to be responsible for some of the alterations. The results thus show that TiN is possible midgap candidate, which exhibit little or no interaction with SiO_2, and that could be N^+ implanted in order to achieve complementary work functions in the case of Ti-rich TiN_x.

The minimum gate metal thickness required for setting the work function has been studied on SiO_2 using ALD TiN in the 2-6 nm range. It was determined that the final work function depends on full closure of the film, which occurs at ~2.5 nm for ALD TiN.

A lot of work has also been done in the field of precisely determining the work function of a metal. A process scheme employing highly doped p-type substrates in order to facilitate barrier height extraction by means of Fowler-Nordheim tunnelling is demonstrated. The results agree well with work functions measured with internal photoemission in the case of PVD/ALD TaN. Another physical method, Kelvin probe Force Microscopy, is used to determine the work function of PVD TiN and Mo on SiO_2. The results point to a high correlation with *C-V* and *I-V* measurements.

Finally, metal gate/high-κ gate stacks are presented. The effect of high-temperature anneals is shown for a PVD Mo/MOCVD ZrO_2 capacitor while ALD TiN devices incorporating compressively strained Si_xGe_y channels and ALD $HfAlO_x$ and/or Al_2O_3 dielectrics are characterized. The devices show vastly improved performance compared to reference devices, while subsequent water vapor anneals reduce the amount of negative charge within the dielectric.

6. Summary of the appended papers

In this section, the most significant results from each paper are presented, with mention of how the subprojects evolved along with the author's individual contributions.

Paper I

"*Investigation of the Thermal Stability of Reactively Sputter Deposited TiN MOS Gate Electrodes*"

PVD TiN/SiO_2 capacitors were examined extensively using XPS depth profiling and capacitance-voltage work function measurements. When RTP temperatures are below 700 °C, the work function is close to the desired pMOS value of ~5 eV. On the other hand, the work function decreases when activation temperatures are in excess of 800 °C, a change which cannot be accounted for by either XRD or XPS analysis. Thorough XPS depth profiling showed that there was no apparent change in the position of the Ti 2p or N 1s binding energies for films annealed at different temperatures. Furthermore, these peaks were at the same position, both in the bulk of the film as well as very close to the TiN/SiO_2 interface, thus indicating the absence of interfacial reactions.

This study was conceived since the thermal response of high-temperature anneals for metal gates is of major research interest. This project was an extension of the results obtained in Paper III. The author supervised the XPS depth profiling and subsequent data analysis, and shared the writing effort.

Paper II

"*Flatband Voltage Adjustment Using Reactively Sputtered TiN Metal Gates*"

The flatband voltage of PVD TiN as a function of nitrogen content was determined using SiO_2 capacitors. It was found that the flatband voltage varied by ~2 V when the nitrogen flow was increased from 0 to 30 sccm, indicating the transition from an n-type to a p-type band-edge metal. The rather large extent of the voltage span is due to the fact that forming gas was

not applied after deposition, hence an elevated amount of oxide charge is present within the SiO_2. XPS results showed that the N_2 content increased with the applied reactive gas flow, which saturated when stoichiometric TiN was obtained at 11 sccm N_2.

The intention of this study was to investigate how the nitrogen flow could be employed to modulate the metal work function. The results then paved the way for a more thorough and improved analysis, see Paper III. The paper was presented by the author at the 4th International Conference on Microelectronics and Interfaces, 2003. The author was responsible for all processing, electrical measurements, and also supervised the XPS analysis. Writing was done with input from the co-authors.

Paper III

"*Variable work function in MOS capacitors utilizing nitrogen-controlled TiN_x gate electrodes*"

Metal gate capacitors (TiN_x/SiO_2/p-Si) were processed and the work functions were extracted, where the effects of annealing as well as due to varying the nitrogen flow were evaluated. The work function of TiN_x varies from 4.2 to 4.9 eV, measured using capacitance-voltage measurements, when the metal was deposited at different reactive nitrogen gas flows. This work function span is almost unchanged if the thermal budget is 600 °C or lower. XRD results indicated a sole [111] texture which was constant irrespective of applied nitrogen flow or activation temperature, and hence, could not explain the measured work function changes. In general, sub-stoichiometric TiN_x films were not chemically stable due to their reactive nature. Finally, annealing at temperatures in excess of 800 °C shifts the work functions towards midgap values for most compositions which may be due to Fermi level pinning due to extrinsic interface states.

The results in this paper were basically refinements of the methods used in Paper II. The effects of subjecting true stoichiometric TiN to high temperature anneals were studied more carefully in Paper I. Processing of wafers, analysis and writing was shared equally by the two primary authors.

Paper IV

"*Low-resistivity ZrN_x metal gate in MOS devices*"

PVD deposited ZrN_x films were characterized electrically on SiO_2 using both capacitance-voltage and current-voltage measurements. In particular, the resistivities and work functions were determined for several nitrogen flows

and annealing temperatures. Highlights include a ZrN resisitivity of 70 μΩcm and an nMOS-suitable work function value of 4.1 eV obtained at low N_2 flows. *I-V* F-N tunnelling agreed well with work functions extracted using capacitance measurements from oxide series. Finally, pMOS metals (4.9 eV) were attained for high nitrogen flows with a thermal budget of 600 °C.

The ZrN metal system was chosen in response to the obvious scarcity of previous electrical measurements. The experience obtained in Paper III proved beneficial when planning the experiments. The author's contributions consisted mainly of writing and discussing the results.

Paper V

"*Comparative Study On The Impact Of TiN And Mo Metal Gates On MOCVD-Grown HfO_2 And ZrO_2 High-κ Dielectrics For CMOS Technology*"

Combinations of metal gate and high-κ capacitors were processed and characterized with *I-V*, *C-V* and HRTEM. 100 nm PVD TiN and Mo was used as metal gate while MOCVD HfO_2 and ZrO_2 constituted the isolators. While the density of oxide charges is rather low after RTP for the Mo/ZrO_2 stack, the leakage current increases which is attributed to crystallization of the ZrO_2. HRTEM also revealed the presence of an interfacial SiO_x layer which is probably formed during post-deposition anneal of the MOCVD dielectric.

This study represents some results obtained within a huge matrix of prospective metal gate/high-κ gate stacks, showcasing a wide variety of materials and deposition methods. The author was responsible for the PVD Mo deposition and dry etching and also electrical measurements after forming gas anneal. Some input was given to the primary author during writing.

Paper VI

"*Metal gate work function extraction using Fowler-Nordheim tunneling techniques*"

Metal gate capacitors were processed with thermally grown SiO_2, capped with increasingly thick ALD HfO_2 dielectric films and combinations of ALD and PVD deposited TaN. The advantage of using highly doped substrates is manifested when measuring the substrate injection current, since on regular wafers the number of carriers is limited, thus limiting the extent of Fowler-Nordheim tunnelling. The work functions of ALD and PVD TaN on SiO_2

(monolayer HfO_2 presence) after FGA was determined to be 4.8 eV (4.9 eV) and 4.4 eV (4.5 eV), respectively. These results agreed very well with values obtained using internal photoemission, within +/- 100 meV.

The idea leading to this paper was mainly to improve the accuracy of work function determination when performing Fowler-Nordheim measurements. Some of the results in this work were produced by the author, during an internship at IMEC in Belgium 2003-2004, while others were produced and discussed with the co-authors. This paper was presented by the author at the 14th Biennial Conference on Insulating Films on Semiconductors, 2005.

Paper VII

"*Comparison between physical and electrical work function extraction methods: Kelvin force microscopy vs. capacitance and current measurements*"

This work aims to compare both physical and electrical methods of assessing the metal work function. Kelvin probe Force Microscopy (KFM) is used to measure the work function of the top metal plate, whereas capacitance-voltage and current-voltage measurements are used to measure the work function at the metal/dielectric interface. PVD TiN and Mo capacitors (SiO_2) were processed simultaneously with sheet metal samples. While the KFM probe reported consistently higher values (0.2-0.3 eV) all methods sensed a decrease in work function due high-temperature anneals in the case of PVD TiN.

The idea behind this comparative study was to complement some of the results in Papers I-III and to benchmark results obtained using KFM with the more commonly used electrical work function extraction procedures. The author was responsible for all processing, electrical measurements, and the majority of the writing effort.

Paper VIII

"*A Novel Strained $Si_{0.7}Ge_{0.3}$ Surface-Channel pMOSFET with ALCVD™ TiN/Al_2O_3/$HfAlO_x$/Al_2O_3 Gate Stack*"

A potential pMOSFET candidate for the 32 nm LSTP CMOS node is presented: a compressively strained $Si_{0.7}Ge_{0.3}$ surface-channel with an ALD TiN/Al_2O_3/$HfAlO_x$/Al_2O_3 gate stack. The channel was selectively grown using reduced-pressure CVD. The current drive and transconductance for SiGe devices was more than 30% higher compared to Si reference devices

using the same gate stack chemistry. In addition, the density of interface states and subthreshold slope was determined as 1.6×10^{12} cm^{-2} eV^{-1} and 110 mV/dec., respectively. Even lower values were similarly attained for the reference Si channel devices.

Some of the processing knowledge (primarily dry etching of TiN) acquired in paper II was used in this work. An extension led to the water vapour experiments presented in Paper IX. The author's contributions consisted of fine-tuning the dry etching of the metal gate using SEM cross-sections, performing activation anneals, participating in the electrical measurements and sharing the writing effort.

Paper IX

"*Effects of low-temperature water vapor annealing of strained SiGe surface-channel pMOSFETs with high-κ dielectric*"

pMOSFETS with compressively strained $Si_{0.8}Ge_{0.2}$ surface-channel and an ALD deposited TiN/Al_2O_3 gate stack were processed. Low temperature (300 °C) water vapour annealing was applied to the samples in 30 min. increments for several hours. The results showed that the subthreshold slope was improved for the reference $SiGe/SiO_2$ devices, but not for the high-κ devices. However, a key observation is that the density of negative oxide charges is significantly reduced after the water vapour annealing, which also follows the decrease of the threshold voltage. One possible explanation states that non-bridging oxygen bonds (Al-O-) in the Al_2O_3 dielectric may be the source of the negative charges.

The background to these experiments were previous reports which stated that a reduction of oxide charges could be observed following water vapour annealing of devices, similar to those presented in Paper VIII. This paper was written with input from all the co-authors and was presented in the form of a poster at the 33rd European Solid-State Device Research Conference, 2003, by the two principal authors.

Sammanfattning på svenska

I dagens integrerade kretsar är fälteffekttransistorn en mycket viktig beståndsdel, både för analoga såväl som för digitala funktioner. Sedan de första fungerande transistorerna började tillverkas på 60-talet har koncentrationen av komponenter på en kretsyta ökat med varje ny generation av processorer. Drivkrafterna bakom denna utveckling är ökad beräkningshastighet och billigare integrerade kretsar. Förutom den kontinuerliga storleksminskningen är kiselskivornas ökande storlek en bidragande orsak till att integrerade kretsar blir än billigare och tillgängliga för en allt större del av jordens befolkning.

Med tiden har forskare lyckats utveckla CMOS-tekniken genom att bl.a. införa mekaniska spänningar i själva transistorn, men nu har det gått så långt att själva materialen måste bytas ut. Den här avhandlingen visar huvudsakligen exempel på möjliga materialkombinationer och processer för styrelektroden, men även för det isolerande skiktet mellan styrelektroden och halvledarsubstratet. I denna avhandling har teststrukturer och även fullständiga fälteffekttransistorer tillverkats för att påvisa fördelarna med metallelektroder. Kondensatorerna används som teststrukturer eftersom de är mycket enklare att tillverka än fullständiga transistorer, samtidigt som mycket information kan fås med avseende på läckströmmar, termisk stabilitet och kapacitans.

Resultaten i denna avhandlingen kan delas upp i tre typer: processning och mätningar på kondensatorer tillverkade med fysisk ytavspjälkning (PVD), mätningar på p-typ kisel-germanium transistorer med en ALD-deponerad metallelektrod respektive dielektrikum samt utveckling av metoder (elektriska och fysikaliska) för att bestämma utträdesarbetet hos en metall.

Utträdesarbeten lämpliga för att ersätta *n*+ och *p*+ polykisel uppmättes för TiN och ZrN, båda deponerade genom PVD på SiO_2. Genom att gradvis öka kväveflödet i kammaren, påvisades en ökning i utträdesarbete från ~4 till ~5 eV för båda metallsystemen, efter sedvanlig formgasbehandling. Värmebehandling vid högre temperaturer gör att utträdesarbetet minskar till så kallade mellanvärden i intervallet 4.7-4.8 eV. Eftersom variationer i metallens sammansättning närmast SiO_2 antogs ligga bakom ändringar gjordes mätningar med ESCA och XRD som dock ej gav något entydigt svar.

Mätningar gjordes också på extremt tunna metallfilmer i syfte att undersöka vilken minsta tjocklek som krävs för att bestämma metallens utträdesarbete. ALD TiN i intervallet 2-6 nm undersöktes, där filmerna sedan täcktes med PVD TaN. Det visade sig att en begänsande faktor var ALD-processen, där en helt sluten film uppnås först vid c:a 2.5 nm.

Primärt används kapacitansmätningar som funktion av pålagd elektrisk spänning för att bestämma metallens utträdesarbete i kontakt med en isolator. Ett alternativt sätt att mäta denna storhet utgörs av tillverkning av testkondensatorer på högdopade substrat, vilket förenklar kvantmekanisk tunnling vid substratinjektion, eftersom laddningsbärare ej behöver genereras via extern ljuskälla. Mätningar gjordes både med Fowler-Nordheim tunnling och fotoemission, på ALD och PVD TaN deponerade på olika kombinationer av ALD HfO_2 och termiskt grodd SiO_2. Skillnaden mellan de olika mätningarna var mindre än +/- 100 meV. En jämförelse mellan KFM (Kelvin probe Force Microscopy) och etablerade elektriska metoder (kapacitans- och ström-spänningsmätningar) visade viss överenstämmelse i uppmätt utträdesarbete för Mo och TiN. Variation i metallens uträdesarbete på grund av värmebehandlingar och metallens tjocklek detekterades av alla metoderna.

En studie som påvisade fördelarna med metallelektrod, isolator med hög dielektricitetskonstant samt mekaniskt spänt halvledarsubstrat gjordes inledningsvis. Kanalen utgjordes av ett kompressivt spänningssatt SiGe substrat i syfte att öka hålmobiliteten i kanalen, medan ALD deponerat TiN och $Al_2O_3/HfAlO_x$ utgjorde styrelektrod samt isolator. Prestandamässigt uppvisades en förbättring jämfört med referenskomponenter på Si: ingen utarmning i metallelektroden och högre ”drain”-ström. Eftersom subtröskellutningen var relativt hög tillämpades värmebehandling i vattenånga vid 300 °C som genomfördes i steg om 30 minuter. Det visade sig (efter ett par timmars behandling) att tillstånden i gränsskiktet ej kunde avlägsnas, men däremot minskade tröskelspänningen i negativ riktning, eftersom antalet negativa fasta laddningar i Al_2O_3-isolatorn reducerades.

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