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# $Ag_2S$-Based Flexible Memristors for Neuromorphic Computing

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ACTA UNIVERSITATIS
UPSALIENSIS
2023

ISSN 1651-6214
ISBN 978-91-513-1975-9
urn:nbn:se:uu:diva-516410

UPPSALA
UNIVERSITET

Dissertation presented at Uppsala University to be publicly examined in Polhemsalen, Ångström, Lagerhyddsvagen 1, Uppsala, Monday, 15 January 2024 at 09:00 for the degree of Doctor of Philosophy. The examination will be conducted in English. Faculty examiner: Professor Qing Cao (University of Illinois at Urbana-Champaign (UIUC)).

**Abstract**

Zhu, Y. 2023. $Ag_2S$-Based Flexible Memristors for Neuromorphic Computing. *Digital Comprehensive Summaries of Uppsala Dissertations from the Faculty of Science and Technology* 2343. 79 pp. Uppsala: Acta Universitatis Upsaliensis. ISBN 978-91-513-1975-9.

Memristive crossbar arrays hold the great promise for fast and energy efficient neuromorphic computing due to their parallel data storage and processing capabilities. As the key component, memristor should achieve stable resistance switching (RS) characteristics with low energy inputs and be compatible with complementary metal–oxide–semiconductor (CMOS) technology. It should also exhibit sufficient device flexibility for applications in wearable electronics. In this thesis, we fabricate flexible memristors (FMs) based on $Ag_2S$ films, investigate their RS behavior and mechanism, demonstrate CMOS-compatible array integration and validate their computing applications.

The thesis starts with a full-inorganic FM, utilizing ductile $Ag_2S$ thick films as both a flexible substrate and a functional electrolyte. The device exhibits dense multiple-level non-volatile states with a remarkable ON/OFF ratio of $10^6$. The exceptional RS behavior is induced by sequential processes of Schottky barrier height (SBH) modification at the contact interface and silver filament formation inside the electrolyte. As a follow-up, we show that interface RS by SBH modification can be facilitated with smaller setting voltages. In contrast to traditional filamentary memristors, the sole interface RS achieves an ultralow switching energy of about 0.2 fJ. An image processing with interface RS indeed exhibits 2 orders of magnitude lower power than that with filamentary RS on the same hardware.

Moreover, interface RS avoids the stochastic nature of filament formation and ablation inside electrolytes. The $Ag_2S$-based FM operating with interface RS exhibits an impressive cycle-to-cycle variation of 1.4%, which is in direct contrast to the variation (28.9%) of filament RS extracted from the same device. Its significantly improved image learning ability over filament RS is also demonstrated during the frequent weight update process in simulations.

Large-scale memristor array, with energy-efficient memristive units at each cross-point, is imperative for neuromorphic computing. We further demonstrate a wafer-scale integration of $Ag_2S$-based memristive crossbar array by fully CMOS-compatible processes. With modulated $Ag_2S$ microstructure, the integrated memristors exhibit a record low threshold voltage of approximately -0.1V for filament formation, and an ultra-small switching energy approaching biological synapses at femtojoules. In addition, the same crossbar arrays are integrated on flexible polyimide substrates, on which analogue multiply accumulate calculations and image recognition simulations are successfully demonstrated. An impressive accuracy of 92.6% is finally achieved in handwritten digit recognition, with the intrinsic nonidealities of the integrated memristors compensated by an advanced training algorithm.

*Keywords:* Ag2S film, flexible memristor, resistance switching, CMOS-compatible integration, neuromorphic computing

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ISSN 1651-6214
ISBN 978-91-513-1975-9
URN urn:nbn:se:uu:diva-516410 (http://urn.kb.se/resolve?urn=urn:nbn:se:uu:diva-516410)

*To my beloved family*

# List of Papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I. **Zhu, Y.**, Liang, J., Mathayan, V., Nyberg, T., Primetzhofer, D., Shi, X. & Zhang, Z. (2022) High Performance Full-Inorganic Flexible Memristor with Combined Resistance-Switching. *ACS Applied Materials & Interfaces*, 14, 21173-21180

II. **Zhu, Y.**, Liang, J., Shi, X. & Zhang, Z. (2022) Full-Inorganic Flexible $Ag_2S$ Memristor with Interface Resistance−Switching for Energy-Efficient Computing. *ACS Applied Materials & Interfaces*, 14, 43482-43489

III. **Zhu, Y.**, Liang, J., Shi, X. & Zhang, Z. (2023) Interface Resistance-Switching with Reduced Cyclic Variations for Reliable Neuromorphic Computing. *Journal of Physics D: Applied Physics*, 57, 075105.

IV. **Zhu, Y.**, Nyberg, T., Primetzhofer, D., Shi, X. & Zhang, Z. (2023) Wafer-Scale Integration of $Ag_2S$-Based Memristive Crossbar Array with an Ultra-Low Switching-Energy Approaching those of Biological Synapses. *In manuscript*.

# Author's Contributions

I. Fabricated and characterized the flexible memristor based on thick $Ag_2S$ films, designed and performed the electrical measurements, modelled the resistance switching mechanism, wrote and revised the manuscript.

II. Fabricated the device, performed the electrical measurements, analyzed the data, wrote and revised the manuscript.

III. Fabricated the device, performed the electrical measurements, designed and performed the simulations, wrote and revised the manuscript.

IV. Synthesized the $Ag_2S$ thin film, fabricated and characterized the $Ag_2S$-based memristive crossbar array, performed the electrical measurements, simulated the image classification, wrote and revised the manuscript.

# List of Papers Not Included in the Thesis

I. Liang, J., Qiu, P., **Zhu, Y.**, Huang, H., Gao, Z., Zhang, Z., Shi, X. & Chen, L. (2020) Crystalline structure dependent mechanical and thermoelectric performance in $Ag_2Se_{1-x}S_x$ system. *Research*, 1-10.

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# Abbreviations

| | |
|---|---|
| AFM | Atomic force microscopy |
| AI | Artificial intelligence |
| ALD | Atomic layer deposition |
| ANNs | Artificial neural networks |
| CBM | Conductive bridging memory |
| CMOS | Complementary metal-oxide-semiconductor |
| CPU | Central processing unit |
| DNN | Deep learning neural network |
| DRAM | Dynamic random-access memory |
| EBL | Electron-beam lithography |
| ECRAM | Electrochemical random-access memory |
| EDS | Energy-dispersive spectroscopy |
| FM | Flexible memristor |
| FTM | Filament-type memristor |
| GPU | Graphics Processing Unit |
| HP | Hewlett-Packard |
| HRS | High-resistance state |
| IoT | Internet of Things |
| ITM | Interface-type memristor |
| LRS | Low-resistance state |
| LTP | Long-term potentiation |
| MAC | Multiply-accumulate |
| MANN | Memristor-based artificial neural network |
| MNIST | Modified National Institute of Standards and Technology |
| PCM | Phase change memory |
| RBS | Rutherford backscattering spectrometry |
| RIE | Reactive ion etching |
| RRAM | Resistive random-access memory |
| RS | Resistance switching |
| SBH | Schottky barrier height |
| SEM | Scanning electron microscopy |
| SGD | Stochastic gradient descent |
| STP | Short-term potentiation |
| TPU | Tensor Processing Unit |
| TT | Tiki-Taka |

| | |
|---|---|
| TTV2 | Tiki-Taka version 2 |
| XRD | X-ray diffraction |
| $A$ | Contact area |
| $C_v$ | Coefficient of variation |
| $g_{ij}$ | Conductance stored in $i^{th}$ column and $j^{th}$ row |
| $g_{ij,ref}$ | Conductance stored as a reference |
| $I$ | Current |
| $I_{cc}$ | Current compliance |
| $K$ | Gain factor controlled at the peripheral circuit |
| $M(q)$ | Memristor resistance |
| PSC | Post-synaptic current |
| $q$ | Electric charge |
| $R_a$ | Average surface roughness |
| $R_{bulk}$ | Bulk $Ag_2S$ resistance |
| $R_{c,\,bot}$ | Bottom contact resistance |
| $R_{c,\,top}$ | Top contact resistance |
| $R_{tot}$ | Total device resistance |
| $s_{ij}$ | Conductance at symmetry point |
| TCR | Temperature coefficient of resistivity |
| $V$ | Voltage |
| $V_{th}$ | Threshold voltage |
| $w_{ij}$ | Weight at $i^{th}$ column and $j^{th}$ row |
| $w_l$ | Learnt synaptic weight |
| $w_t$ | Target synaptic weight |
| $x_i$ | Inputs at layer i |
| $y_i$ | Outputs before activation at layer i |
| $z_i$ | Outputs before activation at layer i |
| $\gamma$ | Scalar factor |
| $\delta$ | Derivative of the error with respect to the weight |
| $\Delta g_{ij}$ | Actual conductance change |
| $\Delta g_{min}$ | Minimum conductance change |
| $\eta$ | Learning rate |
| $\rho_c$ | Contact resistivity |
| $\Phi$ | Magnetic flux |

# 1. Introduction

## 1.1 Background

Driven by technological advancements and societal trends like the proliferation of Internet of Things (IoT), cloud computing, and communication networks, today's world is grappling with an unprecedented surge of data [1]–[3]. While these developments offer opportunities for innovation, they also face challenges, particularly in terms of data congestion and latency [4]. To overcome these challenges, neuromorphic edge computing has emerged as a promising solution. Inspired by human brain's architecture, neuromorphic computing utilizes artificial neurons and synapses for information processing and transmission, which offers powerful cognitive capabilities [5], [6]. This paradigm opens up new possibilities for a wide range of artificial intelligence (AI) applications and beyond.

In a human brain, approximately $10^{11}$ neurons are interconnected via about $10^4$ synapses [7], [8]. Figure 1.1.1 illustrates the communication between two neurons through a synapse. Dendrites receive incoming signals, generate action potentials, and transmit them along axons to neighboring neurons. At the axon terminals, action potentials trigger the release of neurotransmitters into the synapse. This process regulates the connection strength between neurons, which is essential for memory and learning. The artificial counterpart of this signal transmission process is represented by the perceptron (see Figure 1.1.2), a fundamental computational unit that computes the weighted sum of inputs and generates an output using activation functions [9]. Perceptrons can be stacked in specific configurations to build up artificial neural networks (ANNs) for neuromorphic computing, as exemplified in Figure 1.1.3 [10]. Data such as images are fed as the inputs, which are processed and transformed through multiple layers. Each layer in ANNs refines the representation, and ultimately, an output layer produces results to achieve tasks like predictions and classifications [11], [12]. ANNs rely on optimizing a large number of synaptic weights to improve the task performance.

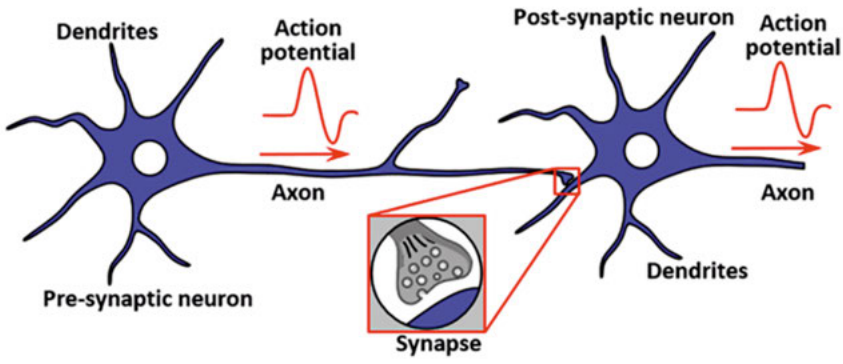


*Figure 1.1.1 Illustration of signal transmission between two neurons. Reprinted with permission from [10]. Copyright (2019) Elsevier Ltd.*

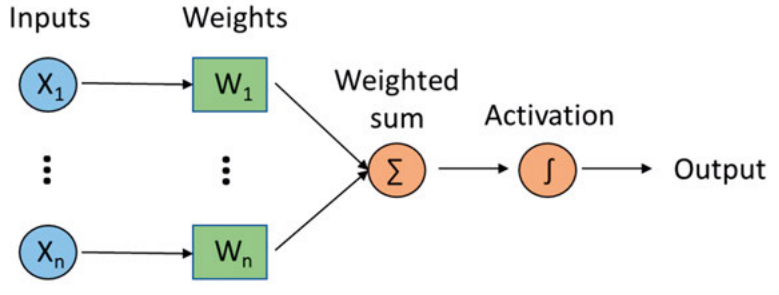


*Figure 1.1.2 Schematic illustration of a perceptron. Inputs ($x_1$, …, $X_n$) are associated with their corresponding weights ($W_1$, …, $W_n$). The weighted sum is fed to the activation function to introduce non-linearity into the perceptron. The output result represents the prediction of the perceptron, which is based on differential importance of the respective inputs.*

However, executing complex ANN models demands substantial computational resources in terms of power and time. For example, thousands of petaflops/s-days of computation is needed to train the 175 billion parameters in the GPT-3 model [13]. As depicted in Figure 1.1.4, in the classical computer architecture, central processing units (CPUs) and memories are separated by the communication bus [14]. During computing, CPU fetches data from memory units, performs operations, and sends the result back to memories. Since the processing speed of CPU is much higher than that of memory accessing, severe latency is generated, which is known as "Von Neumann bottleneck". Besides, frequent data transfer causes significant energy consumption in communication interface, which in turn requires additional thermal management in hardware design [15]. This is particularly important when executing complex computing tasks. Recognizing this bottleneck, dedicated efforts have been devoted to optimize the computing hardware. Graphics Processing Units (GPUs) and Tensor Processing Units (TPUs) have emerged as

specialized processors for parallel processing tasks, such as rendering graphics or performing matrix operations for machine learning. GPUs employ many processing cores, each with own memories to improve the computing [16], while the architecture of TPUs is optimized to achieve higher throughput for machine learning tasks [17]. However, GPUs and TPUs still have to interact with memories, and they are not immune to memory access and data transfer challenges.

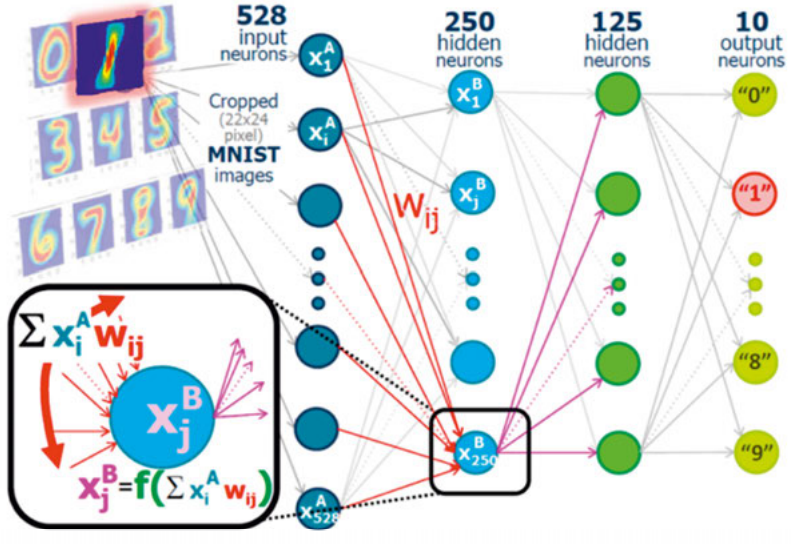


*Figure 1.1.3 Illustration of image classification using an artificial neural network. Reprinted with permission from [10]. Copyright (2019) Elsevier Ltd.*

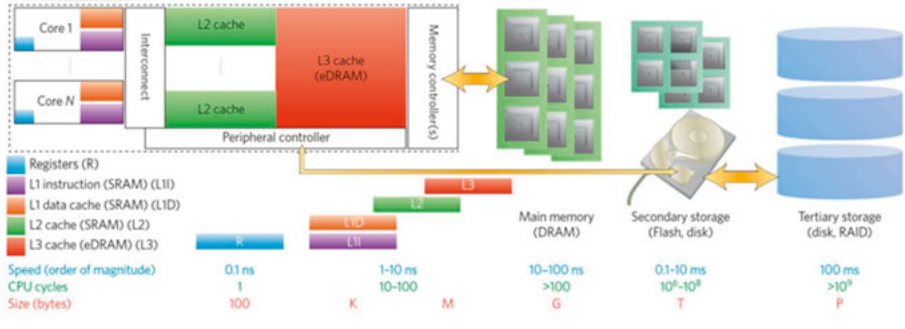


*Figure 1.1.4 Illustration of a classic computing hardware with Von Neumann architecture. The central processing unit is physically separated with different hierarchies of memories. Reprinted with permission from [14]. Copyright (2015) Springer Nature.*

To achieve in-memory computing, memristor-based computing hardware has gained increasing attention in recent decades [18]. Memristors, as the key component of this hardware revolution, are capable of modulating resistance

based on the history of electric charge applied to them, and retain their conductive states after external power is withdrawn. This characteristic enables memristors to perform both data storage and processing within integrated memristor crossbar arrays (see Figure 1.1.5). Such computing hardware can avoid the data transfer between separated memory and processing units, thus alleviating the "Von Neumann bottleneck" [15].

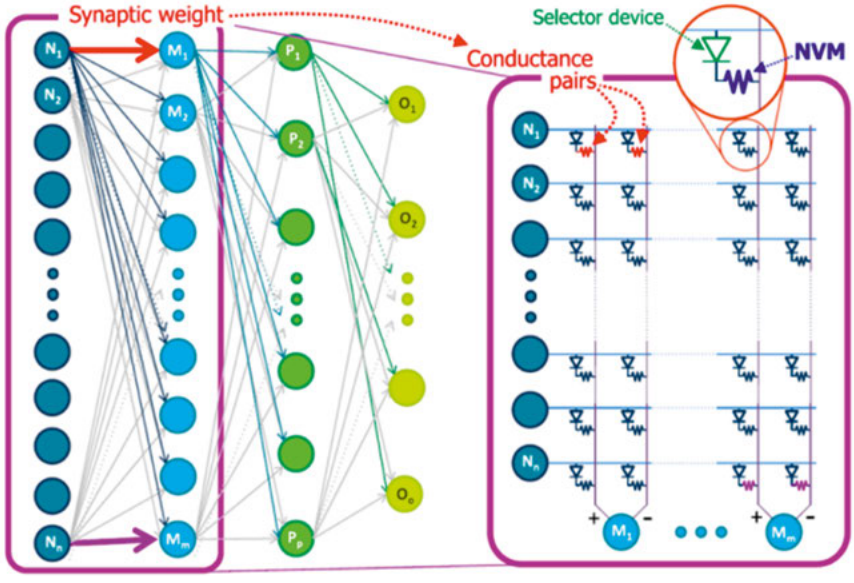


*Figure 1.1.5 Mapping a multi-layer perceptron onto a memristor hardware array. Reprinted with permission from [10]. Copyright (2019) Elsevier Ltd.*

Although memristor technology holds immense promise, it faces substantial challenges on multiple fronts. At the device level, despite their capabilities in efficient data processing and non-volatile data storage, memristors still consume much more energy than biological synapses [19]. Furthermore, device-to-device and cycle-to-cycle variabilities exist, even within memristor devices fabricated from the same batch [20]–[23]. These variabilities will inevitably degrade the accuracy in setting conductive states. Moreover, at the circuit integration level, developing large-scale memristive crossbar arrays with complementary metal-oxide-semiconductor (CMOS)-compatible technology presents significant technical hurdles [24]. Achieving computing on memristor-based hardware with a level of accuracy that meets practical computing needs remains a rare accomplishment. Dedicated research efforts must be devoted to overcome these challenges and to advance the integration of memristors into practical computing systems.

## 1.2 Thesis organization

This thesis is focused on $Ag_2S$-based memristors for neuromorphic computing. Chapter 2 introduces the fundamentals of memristors, $Ag_2S$-based conductive bridging memristors and the working principle of memristor-based computing hardware. Chapter 3 focuses on the fabrication of thick $Ag_2S$ film-based full-inorganic flexible memristor, and the study of its interface and filament combined resistance switching (RS) mechanism. In chapter 4, we investigate the device behavior under sole interface RS, demonstrating its ultra-low switching energy and small cycle-to-cycle variation. Chapter 5 introduces the wafer-scale integration of $Ag_2S$-based memristive crossbar array for energy-efficient computing. The thesis is concluded in chapter 6, and future perspectives are also proposed.

A brief summary of the appended papers is presented as following. In **paper I**, a full-inorganic flexible memristor is fabricated using thick $Ag_2S$ films. A high ON/OFF ratio of $\sim 10^6$ is achieved, and the unique resistance switching mechanism combining interface Schottky barrier height modulation and filament formation/ablation is discussed. In **paper II**, the sole interface RS under small programming voltages is demonstrated. By avoiding filament formation, an ultra-low switching energy at about 0.2 femto-joule is achieved. In **paper III**, we further demonstrate that the sole interface leads to significantly smaller cyclic variation, which helps to improve the programming accuracy during weight updating process. **Paper IV** demonstrates a wafer-scale integration of $Ag_2S$-based memristive crossbar array using CMOS-compatible processes. The integrated device exhibits a record low threshold voltage (~ 0.1 V) and a small switching energy at femtojoules, which holds the promise for energy-efficient computing.

# 2. Fundamentals

The chapter discusses the fundamentals about memristor technologies. Chapter 2.1 gives a briefly overview of memristors. Chapter 2.2 focuses on the development of $Ag_2S$-based conductive bridging memory. In chapter 2.3, the design and working principle of memristor-based computing hardware are discussed.

## 2.1 Memristors

The concept of memristor, a term derived from "memory resistor", was first introduced by Leon Chua in 1971 [25]. Chua's pioneering work focused on addressing a fundamental gap in circuit theory—the absence of a direct relationship between electrical charge and magnetic flux. In his paper titled "Memristor—The Missing Circuit Element," Chua presented a set of five foundational relationships that connect four fundamental circuit variables: voltage (V), current (I), flux (Φ), and electric charge (q). These relationships were summarized as follows (as also illustrated in Figure 2.1.1):

a. Charge (q) was defined as the integral of current (I) with respect to time.
b. Flux (Φ) was defined as the integral of voltage (V) with respect to time.
c. Voltage (V) and current (I) were linked through resistors.
d. Voltage (V) and charge (q) were connected through capacitors.
e. Current (I) and flux (Φ) were connected through inductors.

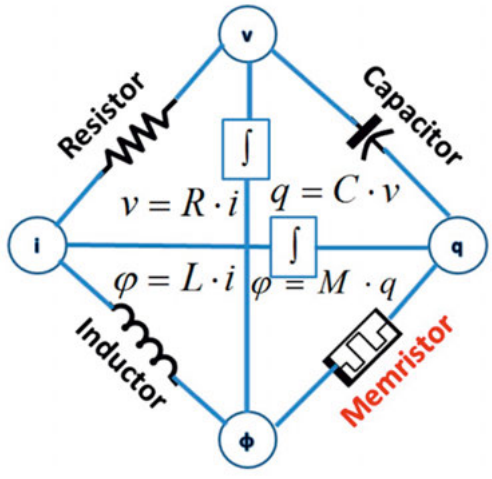


*Figure 2.1.1 Schematic diagrams of six combination relationships among voltage (V), charge (q), flux (Φ) and current (I). Reprinted with permission from [26]. Copyright (2019) Springer Nature.*

The critical observation in Chua's work was the missing relationship between electrical charge and magnetic flux. Chua proposed that a novel circuit element, denoted as memristor, should exist with the unique ability to memorize the quantity of charge that has traversed it in the past. The resistance of a memristor (M(q)) is a function of the charge passed through the device. Since the magnitude of the induced electromotive force in any closed circuit is equal to the rate of change of the magnetic flux passing through the circuit ($V = d\Phi/dt$), the resistance of a memristor can be related to the rate of change of the magnetic flux with respect to the electrical charge [26].

$$M(q) = v/i = d\Phi/(i * dt) = d\Phi/dq \quad (2.1.1)$$

Despite Chua's theoretical proposition, the practical realization of memristors remained elusive for several decades.

In a groundbreaking development in 2008, researchers led by Stan Williams and R. Stanley Williams at Hewlett-Packard (HP) Labs successfully demonstrated memristive behavior in titanium dioxide ($TiO_2$) thin films [27]. They connected the doped (with low resistance) and undoped $TiO_2$ films (with high resistance) in series (Figure 2.1.2a). Under the application of an external bias across the device, the boundary between the two regions would move due to the drift of the charged dopants. For the simplest case of ohmic electronic conduction and linear ionic drift in a uniform field with average ion mobility, they found the resistance of the memristor is a function of charge, which relates the physical $TiO_2$-based device to Chua's theory. The device exhibited a hysteresis in its current-voltage characteristics (as depicted in Figure 2.1.2b).

During the set process, the device current sharply increased when a positive voltage exceeded a certain threshold. The resulted low-resistance state (LRS) could be maintained until a specific negative voltage was applied to obtain high-resistance state (HRS) again. This experiment demonstrated the non-volatile nature, low energy consumption, and synaptic behavior of $TiO_2$-based memristors, highlighting their potential to store and process data in a manner similar to biological systems.

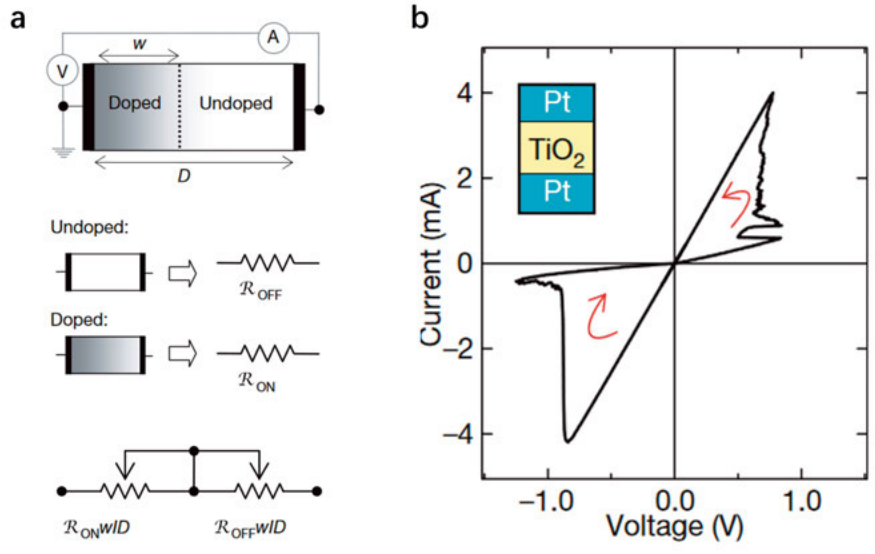


*Figure 2.1.2 (a) Illustration of the $TiO_2$-based memristor. (b) The experimental I-V characteristics of a Pt/$TiO_2$/Pt device by HP lab. Reprinted with permission from [27]. Copyright (2008) Springer Nature.*

For memristors to be utilized for diverse applications, they should meet the following crucial requirements [28]:

a. Operating voltage: The voltage that can trigger resistance switching of a memristor is noted as the operating voltage. Memristors should operate within the range of a few volts or less, offering an advantage over conventional flash memory technologies.

b. Response time: Memristors should exhibit rapid resistance switching dynamics, enabling real-time modulation of conductance. For example, to compete with Dynamic Random-Access Memories (DRAMs), the programming pulse duration should be shorter than 100 nanoseconds. High-performance static random-access memory (SRAM) can even achieve writing within 10 ns.

c. Switching energy: The switching energy consumed during programming a memristor can be estimated by integrating the product of applied voltage and device current over the programming time. Achieving energy efficiency comparable to synapses in human

brain requires that the energy consumed during each switching event remains at femtojoule levels.

d. Switching ratio: The switching ratio (also named as ON/OFF ratio or dynamic ratio) of a memristor is defined as the ratio of the maximum and minimum resistance. A high switching ratio, often exceeding 10, is essential to ensure acceptable computing accuracy in some neuromorphic computing applications.
e. Endurance: Resistance switching between LRS and HRS should be sustained with a certain number of cycles without significant deterioration. State-of-the-art memristors often withstand over millions of switching cycles.
f. Retention: Data retention evaluates the ability of a memristor to maintain its conductance when external electric bias is withdrawn. High retention is vital, especially in memory applications, where data must be preserved for extended periods. Memristors with robust retention characteristics can reliably serve as non-volatile memory elements.
g. Variation: Variation refers to the differences in performance or characteristics among multiple devices (denoted as device-to-device variation) or among multiple operations within the same device (denoted as cycle-to-cycle variation). In applications where consistent and predictable performance is critical, minimizing cycle-to-cycle and device-to-device variation is essential.
h. Multiple-level states: While some memristors are binary (capable of logically representing only 0 and 1), others offer multiple distinguishable conductive states to enable analog information processing and to support more intricate computations. Multiple-level conductive states are indispensable for the synaptic weight update within a memristor-based artificial neural network (MANN).These states play a pivotal role in efficiently performing complex computing tasks.
i. Linearity and symmetry: Linearity and symmetry ensure the precise and predictable conductance modulation in artificial neural networks. When the modulation process is linear, a proportional relationship between the input signal and the resulting change in conductance can be realized. The system can accurately represent and process information, making it easier to fine-tune the network's behavior. Symmetry implies consistent behavior in response to both positive and negative input signals. Symmetric conductance modulation is aligned with the bidirectional plasticity observed in biological synapses, allowing for dynamic and versatile learning in neuromorphic systems.
j. Flexibility: Flexible memristors (FMs) have the potential to meet the requirement in the flexible electronics community as basic

nonvolatile memories. For flexible applications such as wearable electronics, FMs may utilize solid-state or gel-based electrolytes to achieve their resistive switching behavior. These materials should maintain flexibility and resistive switching characteristics under bending or stretching, without performance degradation under long-term operations.

k. Fabrication: The fabrication of memristors should be compatible with silicon technology for monolithic integration with peripheral circuits. This is particularly challenging for the large-scale integration of FMs. FMs must be fabricated using low-temperature processes, which operate below the maximum temperature threshold of the flexible substrate. Furthermore, the choice of materials for FMs is critical. Materials used in the memristor stack have to be compatible with low-temperature process while maintaining the desired electrical properties.

Memristors can be categorized into various types based on their distinct resistance switching mechanisms. These categories include Phase Change Memory (PCM), Conductive Bridging Memory (CBM), Resistive Random-Access Memory (RRAM), Electrochemical Random-Access Memory (EC-RAM), Ferroelectric Random-Access Memory (FeRAM) and etc (Figure 2.1.3). Each type exhibits unique characteristics and operational principles.

a. PCM relies on the significant difference in electrical resistivity between the amorphous (low-conductance) and crystalline (high-conductance) phases of electrolytes [29]. In PCM, low-current pulses heat the phase-change materials to their crystallization temperature, resulting in a low-resistance state. Conversely, high-current pulses quench the material back to its amorphous phase, leading to a high-resistance state. Since setting PCM involves melting and quenching the electrolyte, it tends to be an abrupt process, leading to one-sided switching characteristics.

b. CBM is based on the metallic ion migration and redox reaction, which can electrochemically form/ablate metallic filaments (as the conductive bridge) in the solid electrolyte [30]. The CBMs are known for their short response time and high switching ratio, but the highly conductive metallic filaments often lead to large overall currents, which exacerbate the sneak current path and increase the energy consumption during memristor array operations.

c. RRAM operates by the formation and dissolution of conductive filaments within a solid-state dielectric material, often metal oxides [31]. When a voltage is applied, oxygen vacancies migrate and form a continuous filament between the electrodes, resulting in a low-resistance state. Switching the voltage polarity disrupts the filament,

returning the memristor to a high-resistance state. Similar to CBM, thick filaments in RRAM contributes to relatively large currents.

d. ECRAM relies on ion migration and intercalation within an electrolyte, but does not necessarily require the formation of continuous filaments [32]. ECRAM achieves resistance modulation through electrochemical reactions within the electrolyte layer, altering the distribution of ions, creating or disrupting conductive paths, or modifying the properties of the electrolyte or interfaces. The low-resistance states are energetically favourable, making it suitable for non-volatile memory applications. However, based on the utilized electrolyte material, the properties of ECRAMs can vary a lot. And since the electrolytes in most ECRAMs are either liquid or organic polymers, the integration of these devices is limited by their poor compatibility with CMOS technology.

e. FeRAM operates with bistable polarization states of ferroelectric materials [33]. These electrolytes can be polarized by an electric field, and get reversed under an opposite bias. FeRAM normally exhibits a high operation speed with exceptional switching endurance, making it suitable for data storage. However, it primarily operates with binary switching, meaning that complex computing on FeRAM can be difficult. Moreover, integrating FeRAM devices with CMOS technology can also be challenging.

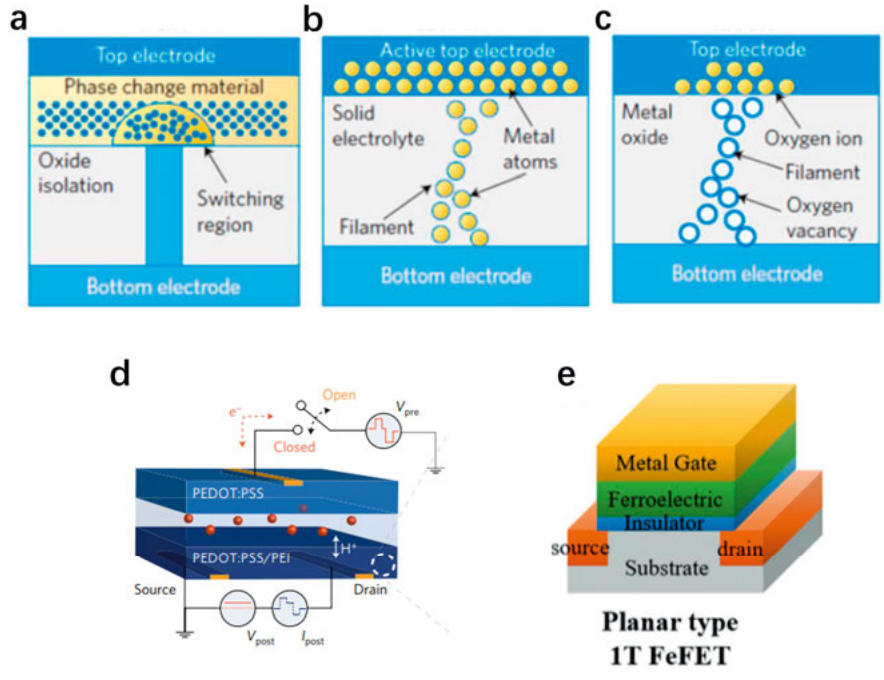


*Figure 2.1.3 Schematic illustration of (a) PCM, (b) CBM, (c) RRAM, (d) ECRAM and (e) FeRAM devices. (d) is reprinted with permission from [77]. Copyright (2017) Springer Nature.*

These diverse memristors exhibit varying properties owing to their distinct resistance switching dynamics. Table 2.1 summarizes some general properties of PCM, CBM, RRAM, ECRAM and FeRAM. It is important to note that specific performance characteristics of memristors can vary based on underlying materials and mechanisms, and most devices exhibit relatively high energy consumption compared with biological synapses for neuromorphic applications.

*Table 2.1 Comparison of resistance switching properties among state-of-the-art PCM, CBM, RRAM, ECRAM and FeRAM devices.*

| Categories | Operating voltage | Response time | Switching energy | Endurance | Retention | Multiple-level states | Number of electrodes |
|---|---|---|---|---|---|---|---|
| PCM | > 1 V | ns - µs | high | $>10^6$ | long | binary | 2 |
| CBM | 0.1~10 V | ns - µs | low | $>10^6$ | long | multiple | 2 |
| RRAM | 0.1~10 V | ns | low | $>10^6$ | long | multiple | 2 |
| ECRAM | 0.1~10 V | >µs | low | moderate | moderate | multiple | 3 (4) |
| FeRAM | > 1 V | ns - µs | moderate | $>10^6$ | long | binary | 3 (4) |

In addition to the abovementioned devices that work with forming conductive paths, memristors based on interface RS is drawing intensive research attention. Many interface-type memristors have been reported to operate by modifying Schottky barrier at the interface, without the requirement of forming conductive filaments. The barrier modification in these memristors is mainly based on trapping/detrapping of charged carriers in the interface states, or field induced oxygen vacancy migration [34], [35]. However, trapping/detrapping of charged carriers is metastable, which leads to severe conductance decay. The Ag/$CoO_x$/Ag device reported by Jianbo et al. could switch for thousands of cycles, but the conductive states decayed rapidly to an intermediate resistance state, due to the short lifetime of the metastable pinning effect caused by the interface states [36]. The research indicated that the pinning effect was dependent on the depth and density of the interface state energy levels. On the other hand, the field-induced oxygen vacancy migration demands high energy cost due to the limited mobility of oxygen vacancy in oxides electrolytes, resulting in the relatively larger energy consumption of the device. Wei et al. reported a Pd/$WO_3$/W memristive array working on the interface RS (Figure 2.1.4) [37]–[39]. The Schottky barrier width of the $WO_3$/W Schottky junction could be modulated by the movement of oxygen vacancy. However, the input pulse to trigger interface RS in the memristor required 1.4 V/400 μs, which indicated a high energy consumption at ~$10^{-10}$ J level. Besides, the relatively poor retention only allowed for short-term potentiation/depression on the device, which could be utilized to process simple information in temporal domain. For these non-filamentary memristors, stable conductive states along with low switching energy are rarely demonstrated.

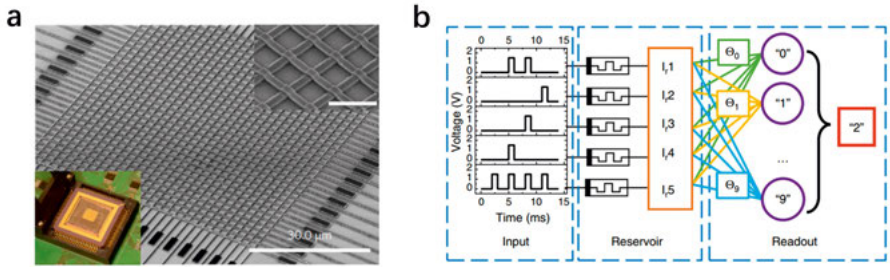


*Figure 2.1.4 (a) Scanning electron micrograph image of a fabricated memristor array used in this study. Upper right inset: magnified SEM image of the crossbar. Scale bar, 3 μm. Lower left inset: memristor chip integrated on the test board after wire-bonding. Reprinted with permission from [39]. Copyright (2017) Springer Nature Limited (b) Schematic of the reservoir computing system with pulse streams as the inputs, the memristor reservoir and a readout network. Reprinted with permission from [38]. Copyright (2017) from the authors.*

## 2.2 $Ag_2S$-based memristors

$Ag_2S$-based memristors represent a promising innovation in the realm of future non-volatile memory devices. Their appeal stems from several remarkable characteristics, including efficient electrochemical process for resistance switching, scalability down to the nanometer scale.

The study of $Ag_2S$-based memristors began in 2005 when Kazuya et al. introduced a quantized conductance atomic switch based on $Ag_2S$ thin films (see Figure 2.2.1) [40]. This work involved creating one-nanometer gap between a fixed $Ag_2S$ electrode and a Pt electrode. Through the tunnelling current across this nano-gap, silver nano-protrusions could be formed or ablated, which effectively switched the device between high and low resistance states.

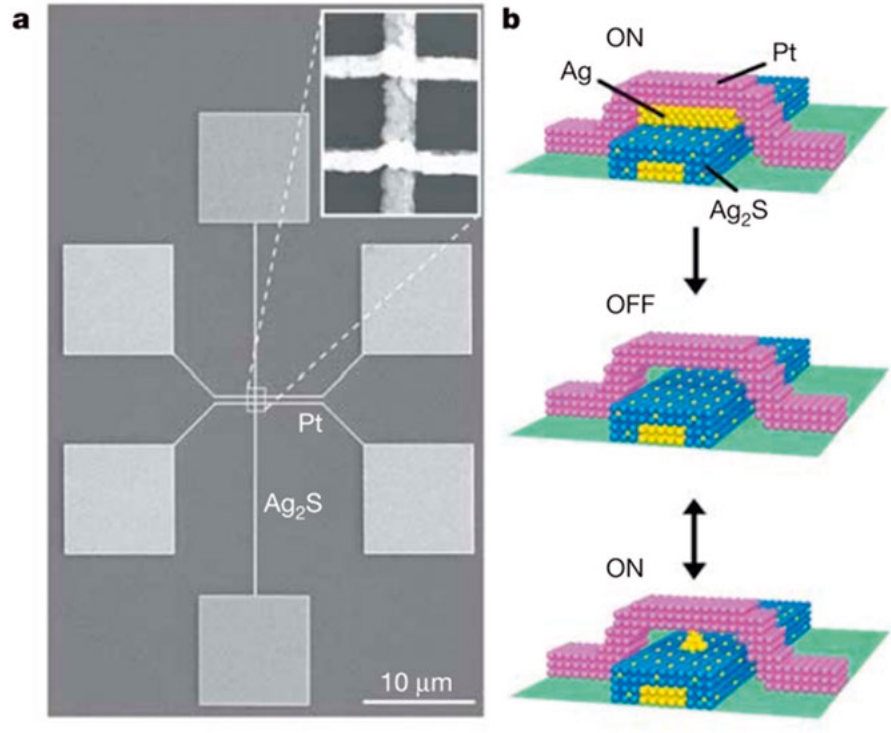


*Figure 2.2.1 (a) The scanning electron microscopy image of the $Ag_2S$-based atomic switch. (b) Schematic diagrams of the atomic switch at ON and OFF states. Reprinted with permission from [40]. Copyright (2005) Springer Nature.*

Notably, this resistance switching can be triggered with a low operating voltage of 0.6 V, at a remarkable frequency of 1 MHz, even at room temperature. Further investigations revealed an aspect: the stability of the

silver filament formed within $Ag_2S$-based atomic switches is dependent on the applied voltage pulses. By controlling the amplitude and width of the applied electrical pulses, the device can switching between short-term and long-term memory states, enabling both the forgetting and memorization of intricate data patterns within device arrays [41].

The intricate process behind this switching phenomenon unfolds in three fundamental steps:

a. Oxidation: at the anode interface, silver atoms underwent oxidation reactions, yielding positively charged silver ions according to the reaction:
   $Ag \rightarrow Ag^{+} + e^{-}$ .
b. Migration: $Ag^{+}$ ions migrated through the $Ag_2S$ thin film in response to an external electric field.
c. Reduction and electro-crystallization: at the cathode interface, reduction and electro-crystallization occurred, converting $Ag^{+}$ ions back into solid silver via the reaction: $Ag^{+} + e^{-} \rightarrow Ag$.

A more common device configuration employs a two-terminal structure (Figure 2.2.2), featuring a nanometer-thick $Ag_2S$ electrolyte sandwiched between top and bottom electrodes. By further optimization in material synthesis and device engineering, researchers achieved precise control of nanometer-scale silver filaments by nanosecond voltage pulses [42]–[44]. The resistance switching exhibited endurance more than 10,000 cycles, and retention over 10,000 seconds, and could be realized even at a low temperature of 4.2 Kelvin.

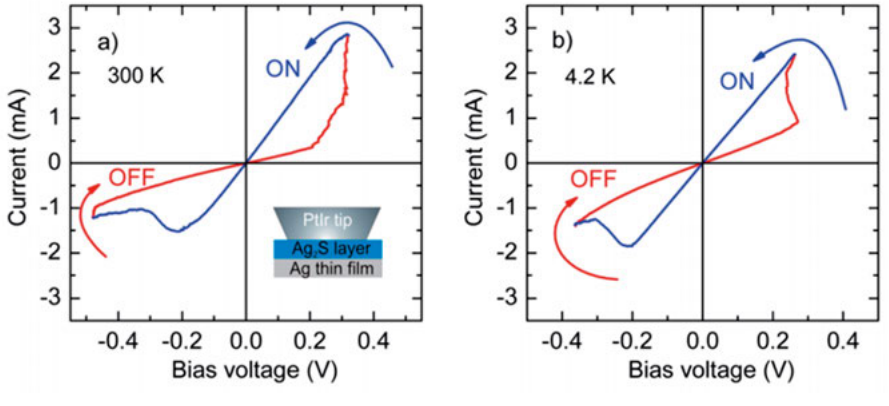


*Figure 2.2.2 Typical RS behavior of an $Ag_2S$-based memristive junctions at room temperature (a) and at 4.2 K (b). The inset in (a) illustrates the typical measurement configuration, where a metallic tip was utilized as a top electrode for material analysis. Reprinted from [44] with permission from the Royal Society of Chemistry.*

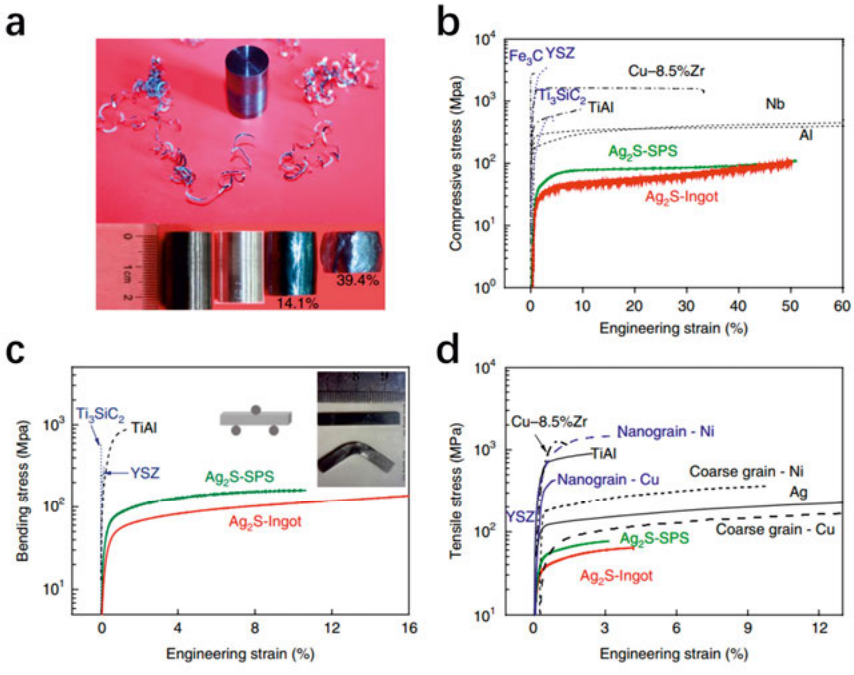


*Figure 2.2.3 (a) A machined cylinder for the compression test (top) and its deformations under hammering (bottom). The thin and winding wires are obtained during the lathing. Strain–stress curves for compression (b), bending (c) and tension (d) tests at room temperature. Reprinted with permission from [45]. Copyright (2018) from the authors.*

In addition to the electrochemical properties, monoclinic α-$Ag_2S$ exhibits extraordinary ductility at room temperature. As first reported by Xun et al. in 2018 [45], α-$Ag_2S$ material could be deformed up to 50% strain in the compression test, and allowed large elongation under bending and tensile tests without destroying the material (Figure 2.2.3). Such metal-like mechanical property was enabled by the low slipping barrier for atomic movement along slip planes, together with the strong interaction between atoms within the slip planes. Considering the intrinsic ductility of the material, Ju-Young at al. reported an $Ag_2S$-based flexible memristor for wearable electronics [46]. The device fabricated by solution processes exhibited bipolar RS behavior with exceptional mechanical stretchability, which enabled its integration with motion sensors for a wearable healthcare monitoring system (Figure 2.2.4).

However, the mentioned RS mechanism in these $Ag_2S$-based memristors only involve simplified filament formation and ablation processes, while the memristive behavior beyond filament region has never been systematically studied, which leaves some phenomena unexplained. And the follow-up research mostly stayed at material-level using simple material testing structure

with a metallic nano-tip as the top electrode. The integration of $Ag_2S$-based memristor array (especially on flexible substrate), detailed resistance switching mechanism, as well as further device performance optimization remain to be demonstrated.

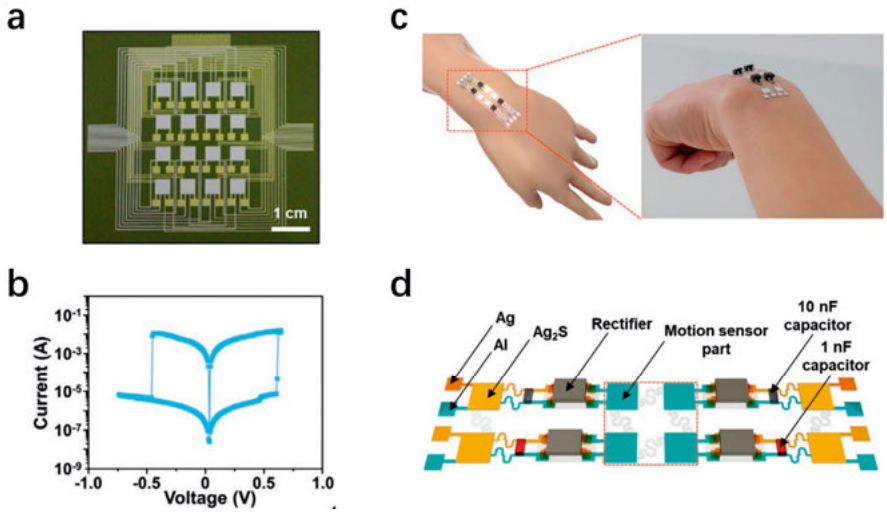


*Figure 2.2.4 (a) Photograph of the self-powered $Ag_2S$-based memristive system cell matrix with 4 × 4 pixels. (b) I–V characteristic for the Al/$Ag_2S$/Ag memory cell. (c) Schematic illustration and photograph showing the flexible/stretchable $Ag_2S$-based memristive system. b) Schematic illustration showing the corresponding device composition of the panel. Reprinted with permission from [46]. Copyright (2021) Wiley-VCH GmbH.*

## 2.3 Memristor-based computing hardware

Memristors, due to their unique ability to emulate synaptic behavior, offer a promising device option for artificial neural networks and brain-inspired computing systems. One of their most significant advantages lies in the potential for realizing computations directly within memory units, overcoming the limitations of traditional von Neumann computers. In this chapter, the operation of a deep learning neural network (DNN) on memristor arrays is illustrated.

Traditional DNN training relies on the stochastic gradient descent (SGD)-based backpropagation algorithm, which consists of three essential processes: forward propagation, backward propagation, and weight updates [47]. These processes are executed within memristor arrays equipped with peripheral circuits (refer to Figure 2.3.1), and the operations are iterated until a convergence criterion is met [48].

In the following instruction of DNN training with conventional SGD, we consider a single fully connected layer between N input neurons and M output neurons. During forward propagation, a vector-matrix multiplication ($z_j = \sum W_{ij}x$) is performed, where the vector x of length N represents the activities of the input neurons and the matrix W of size M × N stores the weight values between each pair of input and output neurons. The resulting vector $y$ of length M undergoes further processing through a non-linear activation function to generate an output ($y_j = f(z_j)$). For DNNs containing multiple layers as shown in Figure 2.3.2, the output of current layer serves as the input to the next layer until the information reaches the final output layer. To train the network, the overall error between the prediction (the final output of forward feed) and the ground truth is calculated and propagated backward through the network [49].

Similarly, the backward propagation within a single layer involves a vector-matrix multiplication using the transpose of the weight matrix ($\partial Z_k/\partial y_j = W^T\delta_k$), where the vector $\delta_k = \partial E/\partial Z_k$ of length M represents the error calculated by the output neurons, and the vector z of length N is further processed using the derivative of neuron's non-linearity and then passed to the previous layer. The key process in training involves updating the weights, which is mathematically implemented by performing an outer product of the two vectors used in the forward and the backward cycles: $\Delta W = \eta (\delta \otimes x)$, where η represents learning rate. For weight update across multiple layers, the derivative of each individual weight with respect to the error is calculated using the chain's rule:

$$\frac{\partial E}{\partial W_{kj}} = \frac{\partial E}{\partial y_l}\frac{\partial y_l}{\partial Z_l}\frac{\partial Z_l}{\partial y_k}\frac{\partial y_k}{\partial Z_k}\frac{\partial Z_k}{\partial W_{kj}} \tag{2.3.1}$$

where the derivatives of the form $\partial y_k / \partial Z_k$ correspond to the derivatives of the appropriate activation function.

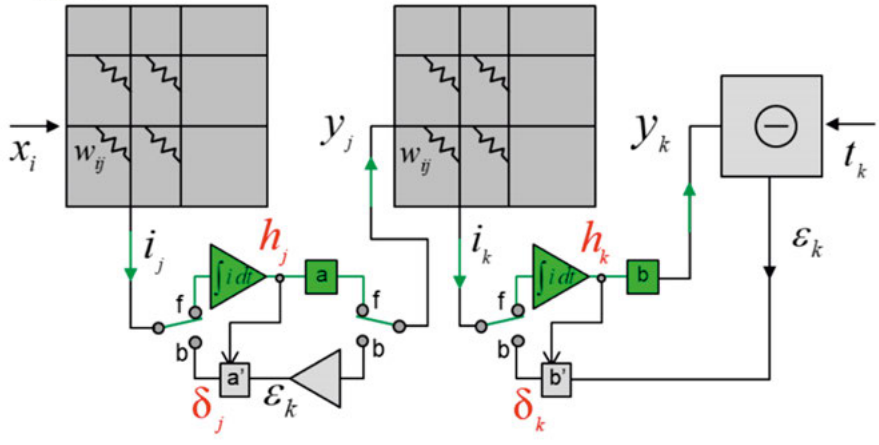


*Figure 2.3.1 Multiple layer perceptron using memristor-based computing hardware. Reprinted with permission from [10]. Copyright (2019) Elsevier Ltd.*

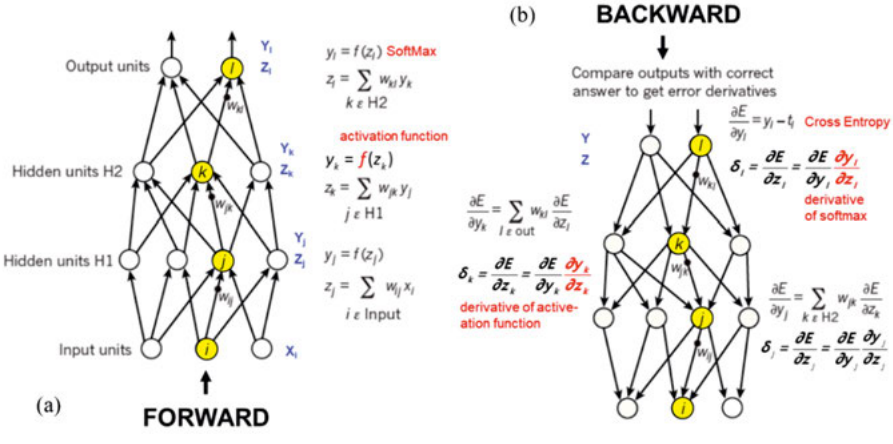


*Figure 2.3.2 The forward feed (a) and backward feed (b) in multiple layer perceptron. Reprinted with permission from [10]. Copyright (2019) Elsevier Ltd.*

The above three processes can be efficiently implemented in memristive crossbar arrays, where the stored conductance of memristors represents the weight matrix. It is worth noting that the physical conductance is always positive. To encode both positive and negative weight values, a pair of memristor devices can be coupled in differential mode:

$$w_{ij} = K(g_{ij} - g_{ij,ref}) \tag{2.3.2}$$

Here, $g_{ij}$ is the conductance value stored on the first memristor device, $g_{ij,ref}$ is the conductance value stored on the second device used as a reference, both corresponding to $i^{th}$ column and $j^{th}$ row and K is the gain factor controlled at the peripheral circuit. In the physical implementation of forward and backward propagation, the input is transmitted as reading voltage pulses through each of the columns, while the output vector is read as a differential current signal from the rows [50]. These operations perform the vector-matrix multiplications using Ohm's law and the Kirchhoff's law. To update the weight (the conductance of memristors) based on the calculated weight change, pulse streams can be effectively utilized (see Figure 2.3.3). For instance, stochastic translators adjust the pulse probabilities at the periphery to control the total number of the pulse coincidences occurring at each crossbar element.[48] In this scheme, pulse streams are simultaneously sent into the crossbar array for all rows and all columns. For each coincidence event, the corresponding memristor device changes its conductance by a small amount $\Delta g_{min}$. The total conductance change required by the algorithm is achieved as series of small conductance changes through numerous pulse coincidence events.

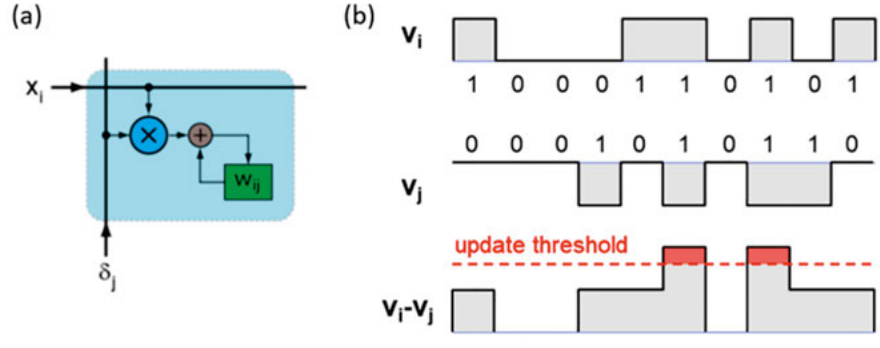


*Figure 2.3.3 (a) Stochastic update of a memristor device at the crossbar array. (b) The pulse streams applied to the array lines for weight update. Reprinted with permission from [10]. Copyright (2019) Elsevier Ltd.*

In conventional stochastic gradient descent and backpropagation algorithms, the memristive devices are required to change conductance in a symmetrical fashion when subjected to positive or negative pulse stimuli. However, the actual changes triggered by each device per pulse coincidence ($\Delta g_{ij}$) are different from the $\Delta g_{min}$ in the most reported devices [51]. Three common switching characteristics are illustrated in Figure 2.3.4. For the ideal device (as shown in Figure 2.3.4a), the change of conductance is linear and has the same value for the positive and negative branches. The hardware induced update rule simplifies back to the desired SGD update rule. The second device changes conductance in a non-linear but symmetric fashion for both potentiation and depression. For the third one illustrated in Figure 2.3.4c,

the actual device responses for positive and negative stimuli at the coincidence event are different. In most cases, their responses are dependent on the current conductance. Since the pulses generated at the periphery are common for the whole array (columns and rows), it is impossible to compensate for the mismatch between $\Delta g_{min}$ and $\Delta g_{ij}$ as each device has a different value due to device-to-device variability. This non-ideality competes with the original optimization objective of neural networks, thus degrading the computing accuracy in the practical hardware.

Gokmen et al. reported an advanced training algorithm, denoted as the "Tiki-Taka" (TT) algorithm, that eliminates the symmetry requirement in device programming [51]. In the abovementioned non-symmetric device, there is a symmetry point at which the strengths of the conductance increment and decrement are equal. As illustrated in Figure 2.3.5, if the device conductance is smaller than the symmetry point, then the conductance increments are stronger than the decrements and vice versa. Therefore, a sufficiently long alternating pulse sequence can push the device conductance toward the symmetry point independent of the initial conductance value. After applying this initial alternating pulse sequence, these conductance values at symmetry points ($s_{ij}$) are transferred to the corresponding reference devices so that $g_{ij,ref} = sij$. Consequently, $g(w_{ij} = 0) = 0$ is met for all devices in the matrix, which is denoted as the symmetry point shifting technique [52].

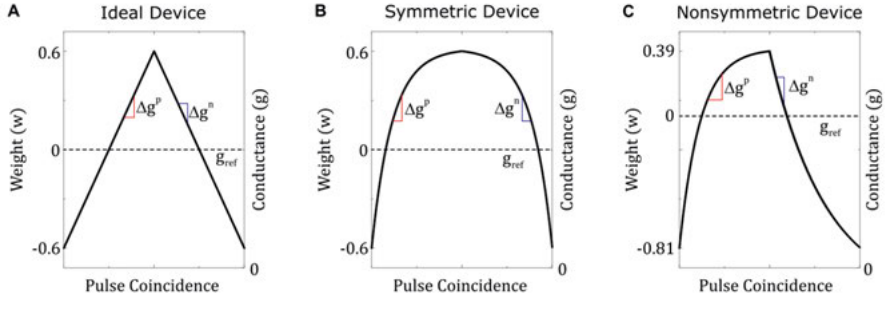


*Figure 2.3.4 Three different device switching characteristics. (a) Ideal device: conductance increments and decrements are equal. (b) Symmetric device: conductance increments and decrements are equal in strength, but both have a dependence on device conductance. (C) Non-symmetric device: conductance increments and decrements are not equal, and both have different dependencies on device conductance. Reprinted with permission from [51].*

In TT algorithm, each weight matrix of the neural network is represented by a linear combination of two matrices:

$$W = \gamma A + C \tag{2.3.3}$$

where A is the first matrix, C is the second matrix and γ is a scalar factor. The elements of A and C matrices are also encoded by a pair of devices as

discussed before. All elements in matrix A are implemented with symmetry point shifting technique to ensure $a_{ij} = 0$. Afterwards, conventional SGD is utilized to calculate the gradient information and the weights in A are updated accordingly. Notably, the weight in C is sparsely updated, with the value changed only in a single column while the remaining elements are kept constant. In this algorithm, the noise in updates due to the random sampling of the data examples pushes the elements of A toward zero, while the sign of the average gradient information in A is very likely to be correct thanks to the symmetry point shifting. The true average gradients represented as the correct sign information are transferred to C. Although the memristors in C are non-ideal as well, the sparse updates significantly mitigate the impact of the artifact. Simulation results on DNNs show that the accuracy achieved using the TT algorithm with non-symmetric device switching characteristics is comparable to the conventional SGD algorithm with symmetric device

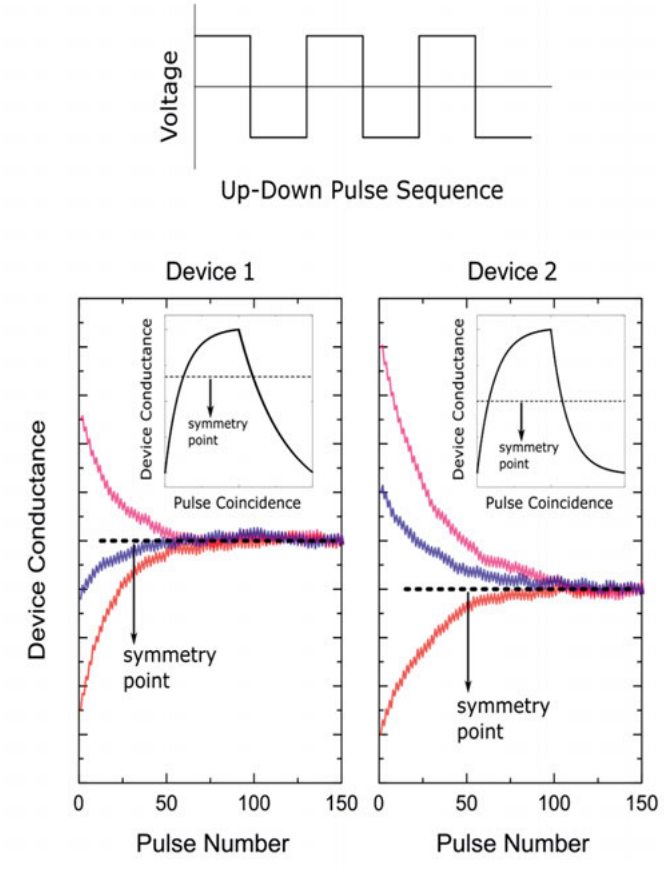


*Figure 2.3.5 Response of two separate devices to the alternating (up and down) pulse sequence starting from different initial conductance values. Reprinted with permission from [51].*

switching characteristics (as shown in Figure 2.3.6). Moreover, all the array operations are still parallel and therefore the hardware implementation maintains the power and speed benefits.

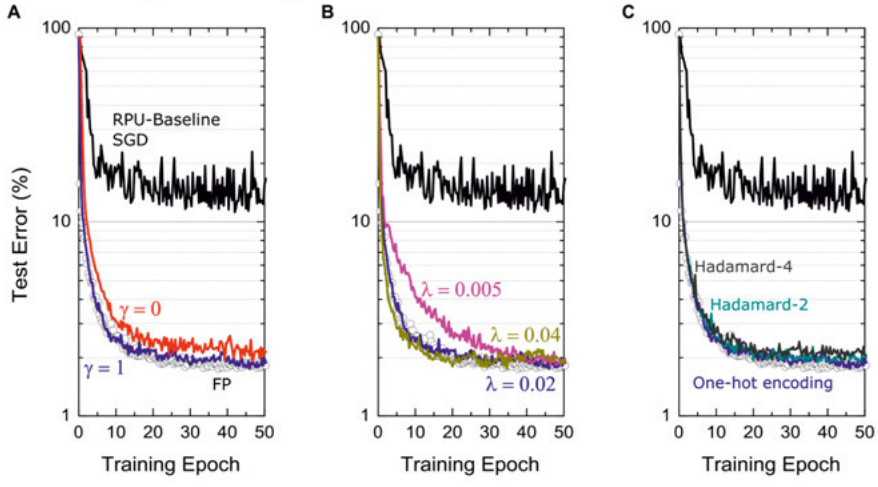


*Figure 2.3.6 Test error of fully connected neural networks on Modified National Institute of Standards and Technology (MNIST) dataset trained using TT algorithm. The comparison of the training results with different mixing terms (a) $\gamma = 1$ and $\gamma = 0$, and different learning rates on C matrix (b) $\lambda = 0.005$, 0.02 and 0.04, as well as different choices of vectors (c) in sparse update of C. Reprinted with permission from [51].*

In a more advanced algorithm, TTV2, the noise tolerance of memristor devices is further increased [53]. Unlike Tiki-Taka, TTV2 uses an additional digital matrix H between A and C as a low-pass filter (as shown in Figure 2.3.7a). The algorithm first employs symmetry point shift technique to ensure that positive and negative updates are treated symmetrically on A. The gradient information is then accumulated on H's corresponding row. When the magnitude of any element in H exceeds the threshold, the corresponding elements are reset back to zero, and a single pulse is applied to C to update the weights. After sufficient training, the weight in matrix C converges to the optimized value. Compared with TT, TTV2 requires only tens of device conductance states, and increases the noise tolerance to the device conductance modulations by about 100 times. Simulation results show that TTV2 can train various neural networks close to their ideal accuracy even at extremely noisy hardware settings (as shown in Figure 2.3.7b).

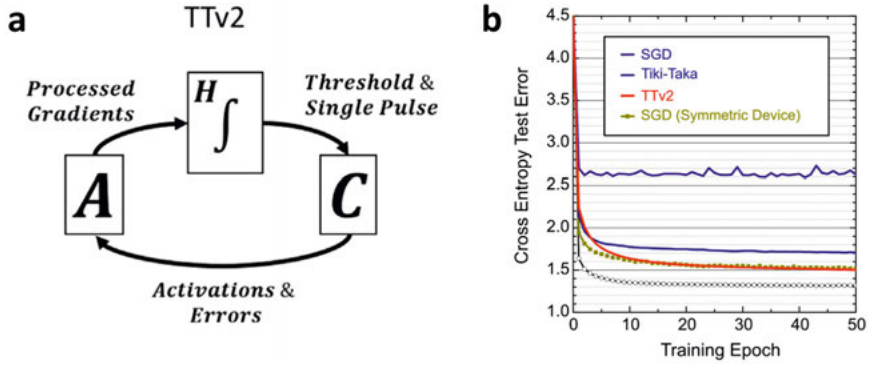


*Figure 2.3.7 (a) Schematics of TTV2 dynamics. (b) Training simulations for SGD, Tiki-Taka, and TTV2 algorithms. Reprinted with permission from [53].*

# 3. Resistance Switching in Flexible Memristors Based on Thick $Ag_2S$ Films

In this chapter, we demonstrate a full-inorganic flexible memristor based on thick $Ag_2S$ films. In chapter 3.1, the synthesis of thick $Ag_2S$ films is introduced. Subsequently, chapter 3.2 outlines the fabrication process for flexible memristors on the obtained thick $Ag_2S$ films. Finally, in chapter 3.3, the resistance switching mechanism of the $Ag_2S$-based flexible memristor is discussed. Understanding RS mechanism plays a vital role in optimization of device performance.

## 3.1 Synthesis of thick $Ag_2S$ films

The free-standing α-$Ag_2S$ films was obtained from bulk $Ag_2S$ ingots, a process elucidated in this section. The used bulk $Ag_2S$ ingots were meticulously prepared through solid-state reactions, ensuring the high purity of the materials. The details of the $Ag_2S$ film synthesis are summarized as below:

a. First, high-purity elemental Ag (99.999%, Alfa Aesar, shots) and S (99.999%, Alfa Aesar, powders) were combined in a stoichiometric ratio of 2:1, resulting in an admixture of approximately 8 grams.
b. This admixture was sealed within an evacuated quartz tube, which was then heated to a temperature of 1000 °C. It was allowed to dwell at this temperature for 12 hours before undergoing a slow furnace cooling process over 25 hours, ultimately reaching 100 °C.
c. Subsequently, the tube was annealed for a period of 5 days at 450 °C to yield the final $Ag_2S$ product.
d. The dense $Ag_2S$ ingot was directly cut into pieces with a thickness of approximately 1 millimeter.
e. These $Ag_2S$ pieces were thoroughly cleaned using acetone and ethanol.
f. The cleaned $Ag_2S$ pieces were then transformed into films by employing a roller-pressing technique. This process continued until the film attained the desired thickness, such as 100 μm.
g. During the rolling process, the edges of the samples were carefully trimmed.

To characterize the obtained film, X-ray diffraction (XRD) and Rutherford backscattering spectrometry (RBS) were employed. The XRD results shown in Figure 3.1.1a agree well with the patterns from $Ag_2S$ single crystals, indicating a successful synthesis of polycrystalline $Ag_2S$ film in monoclinic phase. The measured RBS signal aligns with the simulation results (Figure 3.1.1b), where the atomic ratio of Ag:S gives a stoichiometry at 2:1. Moreover, the $Ag_2S$ film, with a thickness of 100 μm, possesses impressive mechanical properties. It can withstand an elongation of 2.1% under a tensile stress of approximately 100 MPa, as depicted in Figure 3.1.2. This small tensile modulus value is comparable to some metallic materials, showcasing the remarkable mechanical strength and flexibility [45].

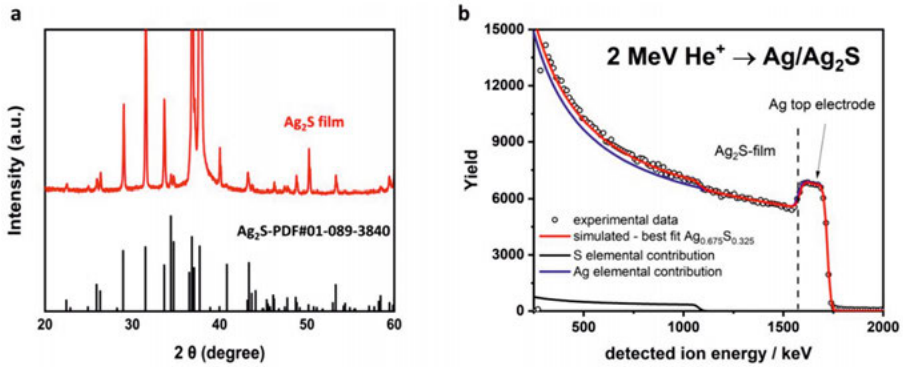


*Figure 3.1.1 Characterization of the thick $Ag_2S$ film. (a) X-ray diffraction pattern of a 100 μm-thick $Ag_2S$ film, which is consistent with α-$Ag_2S$ (01-089- 3840). (b) Experimental RBS-spectrum recorded from an $Ag_2S$ film (with an Ag top electrode as reference) using a microbeam of 2 MeV $He^+$ ions (open circles). The best fit to the experiment (red line) yields a composition of $Ag_{0.675}S_{0.325}$, which is close to the target stoichiometry of $Ag_2S$.*

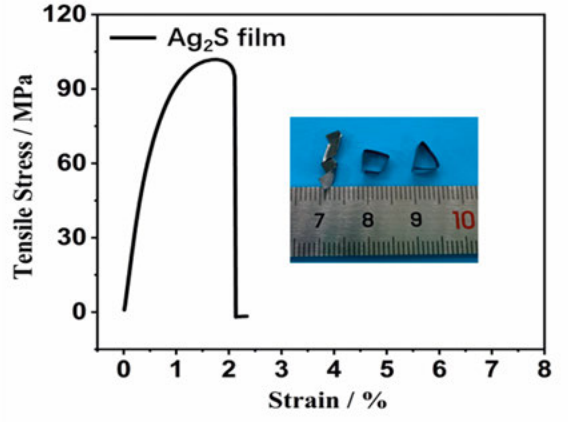


*Figure 3.1.2 Mechanical tension of the thick $Ag_2S$ film at room temperature. The inset shows the bended film.*

## 3.2 Fabrication of thick $Ag_2S$ film-based flexible memristor

In this section, we detail the fabrication process of flexible memristors directly on free-standing α-$Ag_2S$ films, without the need for additional polymer substrates in our device demonstration. Figure 3.2.1a provides an overview of the fabrication process for these flexible memristors. The steps involved are as follows:

a. A 100 nm-thick blanket silver layer was deposited as the bottom electrode using thermal evaporation under a vacuum of $5 \times 10^{-6}$ Torr, with a deposition rate of 0.1 nm/s.
b. On the top side of the film, a 5 nm-thick $HfO_2$ layer was deposited at 170 °C by atomic layer deposition (ALD).
c. Nano contact holes were then precisely patterned using electron-beam lithography (EBL), followed by a reactive ion etching (RIE) process to etch through the $HfO_2$ layer.
d. Finally, 100 nm-thick silver top electrodes were formed through the nano contact holes using a silver evaporation and lift-off process.

Notably, our approach departs from the conventional symmetric memristor device with a crossbar structure. Instead, we employ an asymmetric device structure. The nanoscale top contacts, formed in the 100 nm contact holes through the 5 nm-thick cap $HfO_2$ layer (as depicted in Figure 3.2.1b, a top-view scanning electron microscopy (SEM) image of the 100 nm contact hole array), are approximately 10 orders of magnitude smaller than the bottom contacts ($1 \times 1$ $cm^2$ contact size). This asymmetry in contact size ensures that the top contact dominates the total resistance of the device and takes all the voltage bias to the device, if the device is measured in the vertical configuration between the top and bottom contacts. The contribution from contact resistance at the bottom interface is effectively negligible.

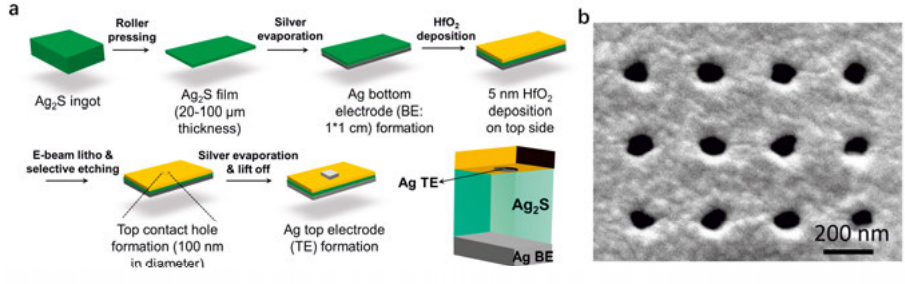


*Figure 3.2.1 (a) Process flow of $Ag_2S$-based memristor device fabrication. The dimensions shown are not scaled to the actual size. (b) Top-view scanning electron microscopy image for a 100 nm nano-hole array fabricated on top side of α-$Ag_2S$ film. In each memristor device, only one contact hole was formed for top contact.*

## 3.3 Interface and filament combined resistance switching

The obtained device exhibits a typical bipolar memristive characteristics when measured in vertical configuration, as illustrated in Figure 3.3.1a. The current (I)-voltage (V) characteristics were recorded by scanning the voltage through a sequence of: 0 V→ −0.5 V → 0.5 V → 0 V on top electrode. Under negative bias (-0.5 V), the memristor switches into a low-resistance state (tens of ohms), and maintains this state until reset to a high resistance state (about 10 MΩ) with a positive bias. The ON/OFF ratio achieved is about $10^6$, an ultra-high value compared to previously reported flexible memristors, especially considering the low setting voltage (Figure 3.3.1b) [40], [46], [54]–[68].

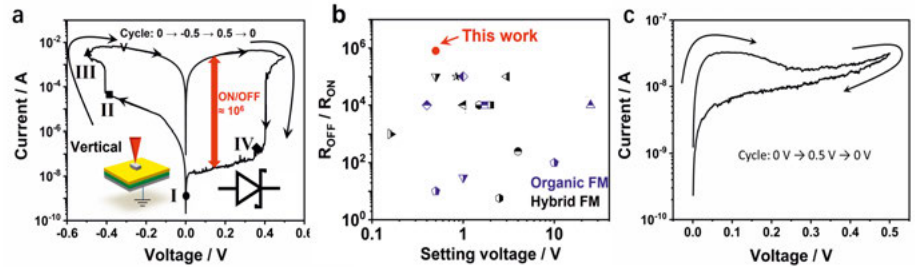


*Figure 3.3.1 (a) Current (I)-voltage (V) characteristics of $Ag_2S$-based memristor in vertical configuration. Different stages of the resistance switching processes are marked by I, II, III, IV in the curve. (b) Comparison of the ON/OFF ratio under different setting voltages between $Ag_2S$-based memristor and the recently reported full-organic and hybrid flexible memristors. (c) The current-voltage curves recorded by applying electric bias to top electrode of an initial memristor device.*

The asymmetric device structure clearly outperforms conventional symmetric $Ag_2S$-based devices in dynamic ratio. Furthermore, our experimental results challenge the simplified filament formation/ablation models proposed for RS in the literature. Notably, the exponential decrease in resistance before the sharp current jump at approximately -0.4 V (between stages I and II in Figure 3.3.1a) cannot be attributed solely to filament formation since no abrupt current increase is observed. It is also evident from the resistance increase observed when a positive bias is applied to an initial memristor device without any pre-existing filament (Figure 3.3.1c). To investigate the resistance switching mechanism, we model the relevant resistances in our device. At the initial stage of the vertical configuration measurement, the total device resistance ($R_{tot}$) consists of three components: contact resistances at the top ($R_{c,\,top}$) and bottom ($R_{c,\,bot}$) Schottky contacts, along with bulk $Ag_2S$ resistance ($R_{bulk}$).

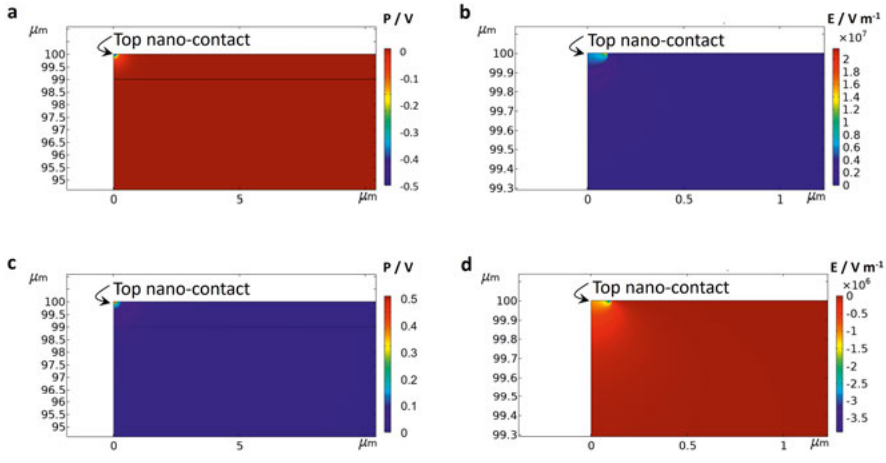


*Figure 3.3.2 Simulated electric potential and electric field distribution of vertical configuration device using finite element analysis. (a) The potential distribution under -0.5 V bias. The result shows that the top nano-contact interface takes most of the setting bias. (b) The simulated electric field distribution under a -0.5 V setting bias. (c) The potential distribution under 0.5 V bias. When a 0.5 V bias is applied on top, this top Schottky contact is forwardly biased. The top interface remains taking the main applied bias due to its extremely small nano-contact area comparing to the bottom contact, which is responsible for the formation of $Ag^+$ depletion region. (d) The simulated electric field of device under a 0.5 V resetting bias. The bias was applied on the top electrode.*

$$R_{tot} = R_{c,top} + R_{bulk} + R_{c.bot} = \frac{\rho_{c,top}}{A_{top}} + R_{bulk} + \frac{\rho_{c,bot}}{A_{bot}} \quad (3.3.1)$$

Where $R_{c,\,top}$ and $R_{c,\,bot}$ can be expressed by $\rho_c/A$, and $\rho_c$ is the contact resistivity and A is the contact area. Notably, $R_{c,\,bot}$ is negligible due to its contact area (being 10 orders of magnitude larger than $R_{c,\,top}$). During the negative setting voltage application, the reversely biased top $Ag/Ag_2S$ Schottky junction dominates, overpowering $R_{bulk}$ in the setting process as shown in the simulation (Figure 3.3.2). This results in a substantial electrical field that accumulates $Ag^+$ ions at the top $Ag/Ag_2S$ interface to form a strong interfacial dipole [69], [70], and thus reduces the electron Schottky barrier height (SBH), as depicted schematically in Figure 3.3.3a (Ag accumulation - stage II). Simultaneously, $Ag^+$ ions are reduced to Ag atoms, forming filaments that grow towards the bottom electrode. As these filaments reach the bottom electrode, they create a conductive path that effectively shunts both bulk $Ag_2S$ and contact resistances, resulting in the sudden current jump at approximately -0.4 V (see metallic contact stage III in Figure 3.3.3a).

The dependence of resistance on temperature at stages I, II, and III further validates the SBH modification (Figure 3.3.3b). Stages I and II exhibit typical Schottky junction conduction behavior [71], dominated by the thermionic emission process. As seen in the inset, the electron SBH decreases from 0.206 to 0.120 eV from stage I to stage II. In contrast, stage III demonstrates a stable temperature coefficient of resistivity (TCR) of 0.00135 $K^{-1}$, indicating the formation of continuous silver filaments.

During the reset process under positive bias, the formed Ag filaments are oxidized to $Ag^+$ ions at the top electrode and get ablated at approximately 0.4−0.5 V, leading to an abrupt drop in current. Subsequently, the strong local electrical field induced by the reformed top Schottky contact drives away $Ag^+$ ions, leaving negatively charged Ag vacancies at the top interface. The negatively charged Ag vacancies further bends the energy band upward and increases the barrier height at the top contact interface, as indicated by the further exponential decrease of the current in Figure 3.3.3a-IV. Low-temperature measurements also confirm that the electron SBH indeed increases to 0.407 eV after the reset process. The increased SBH leads to enlarged OFF state resistance compared to its initial value. These findings suggest a new interface-filament combined resistance switching mechanism in our $Ag_2S$ memristors, where sequential SBH modifications and filament formation/ablation processes synergistically contribute to a substantial resistance change, resulting in a large ON/OFF ratio.

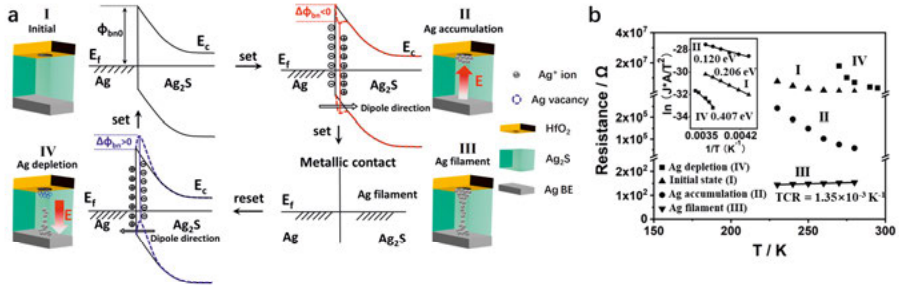


*Figure 3.3.3 (a) Schematic illustration of resistance switching mechanism (The corresponding stages I, II, III, IV are also indicated in I−V curve in Figure 3.3.1a). (b) Temperature dependence of the device resistance at initial (I), $Ag^+$ accumulation (II), filament (III), and $Ag^+$ depletion (IV) stages measured under low temperatures. The inset shows electron Schottky barrier height extraction for stages I, II, IV.*

The interface-filament combined mechanism in our flexible memristor demonstrates densely populated conductive states. As illustrated in Figure 3.3.4a, a series of writing pulses, each with a constant duration of 20 ms but increasing amplitudes, gives discrete nonvolatile states. This dynamic progression, characterized by silver depletion, accumulation, and filament formation, effectively reflects the resistance switching processes at both the interface and filament regions. With a more sophisticated pulse program, as depicted in Figure 3.3.4b, we can further expand the multiple conductive states. By applying small pulses with a fixed amplitude of -0.2 V but variable durations ranging from 2 to 800 ms, 28 states are identified within the range of $3.5 \times 10^{-6}$ S to $3.5 \times 10^{-5}$ S in the interface resistance switching region. This signifies the potential for fine-tuning and continuous adjustment of conductive states.

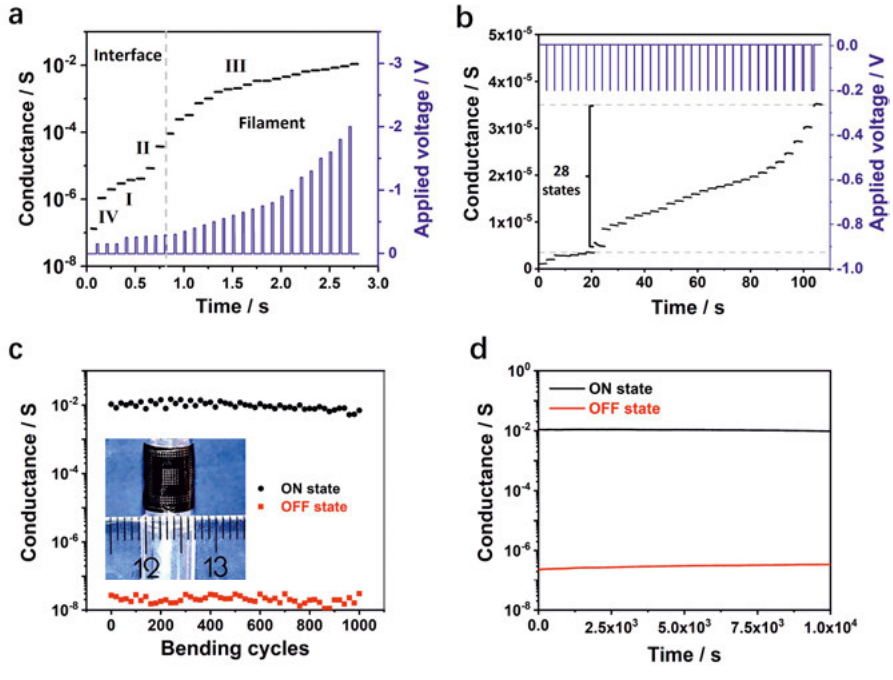


*Figure 3.3.4 (a) Conductive states evolution (read at 5 mV) under pulse voltage stimulations (with 20 ms constant duration and variable amplitude from −0.15 V to −2.0 V). The obtained high density working states cross both interface and filament regions. (b) Conductive states evolution (read at 5 mV) under pulse voltage (with a fixed −0.2 V amplitude and variable width from 2 to 800 ms) (c) Resistance variation before and after mechanical bending with 3 mm curvature radius as shown in the inset. (d) The in-situ data retention recorded when the device was kept in bending state with 3 mm curvature radius.*

To investigate the RS behavior under deformation, we bended the device to a curvature radius of 3 mm, and recorded the conductance after returning it to a flat state. As illustrated in Figure 3.3.4c, during 1000 repetitive bending

tests, the conductance of both the ON and OFF states remained consistent at their respective levels. Even when the device was maintained in a bent configuration, it exhibits exceptional state stability, as evidenced by the retention test shown in Figure 3.3.4d. The reliable RS behavior along with deformation tolerance demonstrates the potential of the $Ag_2S$-based FMs for flexible applications.

# 4. Sole Interface Resistance Switching for Neuromorphic Computing

As discussed in chapter 3, the thick $Ag_2S$ film-based FM undergoes sequential processes of Schottky barrier height modification at the contact interface and filament formation inside the electrolyte. High-voltage pulses (over the threshold voltage ~ 0.4 V) set the memristor into the $10^{-4}$ to $10^{-2}$ S range by forming/ablating Ag filaments, while low-voltage pulses drive the device to a relatively lower conductance range (about $10^{-6}$ to $10^{-4}$ S) by modifying the SBH. Considering the beneficial of utilizing lower conductance for reducing energy consumption, we further investigate the sole interface resistance switching in this $Ag_2S$-based FM. The sole interface RS behavior is introduced in chapter 4.1, and its energy consumption and cyclic variations are discussed in chapter 4.2 and chapter 4.3, respectively.

## 4.1 Sole interface resistance switching in $Ag_2S$ Memristors

As depicted in Figure 4.1.1a, the observed high ON/OFF ratio is a result of sequential processes involving Schottky barrier modification at the contact interface (set bias below -0.4 V) and the formation of nanoscale Ag filaments within the electrolyte (set bias above -0.4 V). An abrupt reduction in resistance marks the transition between these two processes, as illustrated in the inset of Figure 4.1.1a. Schottky barrier modification relies on $Ag^+$ ion accumulation at the top contact interface, whereas the continuous formation of Ag filaments within the electrolyte demands extensive electrochemical reduction of $Ag^+$ ions at the cathode. Consequently, resistive switching based on Ag filaments is more energy-intensive. Here we record the I-V characteristics of our $Ag_2S$ FMs under sole interface Schottky barrier modification. As shown in Figure 4.1.1b, reversible RS is achieved under a bias sequence of 0 V → -0.2 V → 0.2 V → 0 V, where the setting and resetting processes are exclusively induced by the reduction/increase of the SBH at the top interface. Notably, no abrupt current increase is observed during the set process, indicating the absence of filament formation within the $Ag_2S$ electrolyte (Figure 4.1.1b).

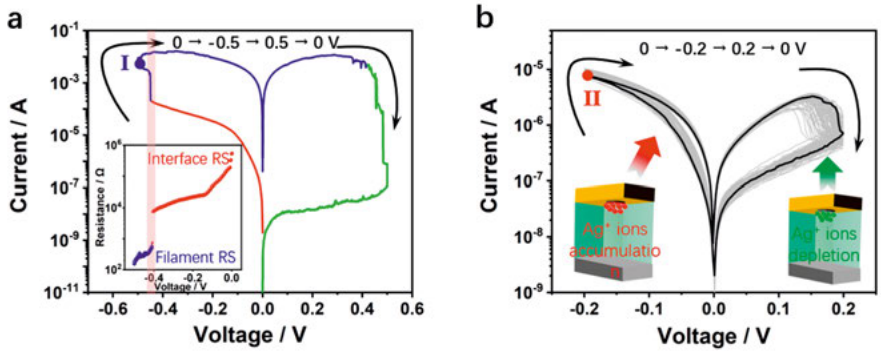


*Figure 4.1.1 (a) Current (I)−voltage (V) characteristics of FM under 0 V → −0.5 V → 0.5 V → 0 V voltages applied to the Ag TE. The inset shows resistance reduction under negative setting bias, where interface RS (setting bias < −0.4 V) is observed before filament formation. Device set by −0.5 V bias is marked by stage I in the curve. (b) I−V characteristics of the device under 0 V → −0.2 V → 0.2 V → 0 V voltages applied to the Ag TE. As schematically illustrated, the device is set by the $Ag^+$ ion accumulation-induced SBH reduction and reset by the $Ag^+$ ion depletion-induced SBH increase at the top contact interface. Device set by −0.2 V bias is marked by stage II in the curve.*

To further validate this, we conducted in situ cryogenic measurements to monitor changes in device resistance (after setting) under varying temperatures. As shown in Figure 4.1.2, the device set with a -0.2 V voltage exhibits an exponential resistance-temperature relationship (stage II). This behavior signifies typical carrier transport through thermal emission processes. It confirms that device resistance is primarily governed by the Schottky junction at the Ag/$Ag_2S$ interface following a -0.2 V setting. In direct contrast, the device resistance after a -0.5 V voltage (stage I, after Ag filament formation) shows a weak dependence on temperature, indicative of phonon scattering effects typically observed in metallic conductors [18], [72], [73].

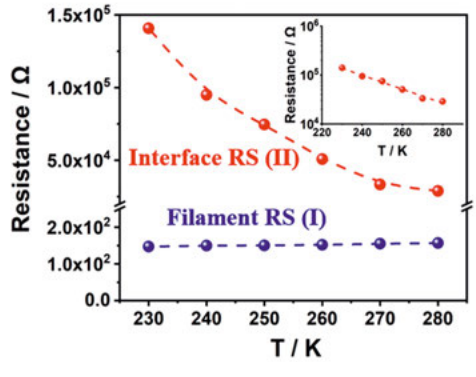


*Figure 4.1.2 Device resistance evolution under temperature variations.*

## 4.2 Ultra-low energy consumption of interface RS

Low conductance states hold the promise for reducing energy consumption during memristor array operation. With this understanding, we further conducted an extensive investigation into the tunability, stability, and switching energy of interface RS states. The efficient modulation of low-conductance states is demonstrated by applying −0.2 V pulses with varying durations (refer to Figure 4.2.1a). Besides, the nonvolatility of 20 multiple-level states is further verified by the retention measurements, as shown in Figure 4.2.1b. The tunability and stability of multiple conductive states promise the programming reliability of interface RS for the synaptic weight update in MANN. More importantly, the switching energy of interface RS in the $Ag_2S$-based device is significantly lower than the reported filament RS-based FMs. As summarized in Figure 4.2.1c, the pulse energy required to trigger interface RS with different ON/OFF ratios is benchmarked with recently reported filamentary FMs [74]–[80]. This benchmarking reveals a remarkable reduction in switching energy, achieving a decrease of several orders of magnitude. An ultralow switching energy of only ~0.2 fJ is needed to attain a 5 ON/OFF ratio with the interface RS in our $Ag_2S$ FM. The result demonstrates a promising strategy to reduce memristor power dissipation with this new RS mechanism.

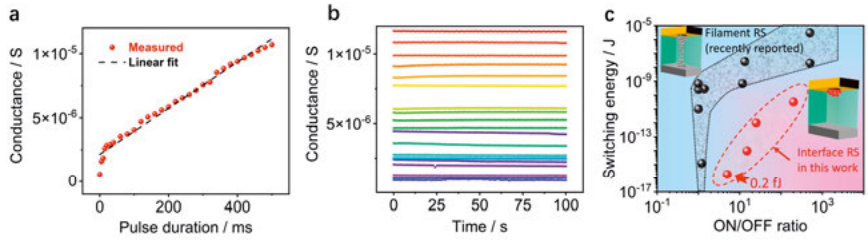


*Figure 4.2.1 (a) Conductance evolution of $Ag_2S$ device under −0.2 V setting pulses. (b) Retention of 20 interface RS conductive states. (c) Comparison of switching energy between $Ag_2S$ device (with interface RS) and recently reported filamentary devices. A significant reduction of switching energy is demonstrated with interface RS.*

We demonstrated multiply-accumulate (MAC) operations on a single-dot device array, which can be logically regarded as a 1 × N crossbar structure. As shown in Figure 4.2.2a, the convolutional kernel values for "sharpening" and "softening" operations were mapped to the FM conductance in an $Ag_2S$ device array. For comparison, we encoded the kernel values utilizing filament or interface RS, respectively (additional details can be found in **Paper II**). The pixel values of the original image, ranging from 0 to 255, were linearly transformed into reading voltages, with amplitudes ranging from 0 to 25.5 mV. Since the device array shares a common bottom electrode, we collected the output current resulting from the voltage-conductance multiplication and

subsequent current addition. This output current represents the convoluted feature map, which can be decoded into the grayscale output image for visualization. Figure 4.2.2b illustrates the decoded output images obtained from both software simulations (i and iv) and hardware processing (ii, iii, v, and vi). The simulation results were derived from precisely designed kernels and serve as a reference for evaluating the hardware's processing performance. In the outputs generated by filament-type memristors (FTMs) and interface-type memristors (ITMs), the sharpening operation significantly enhances the contrast between the subject (e.g., the "horse") and its surroundings, while the softening operation imparts a smoother appearance to the subject and its adjacent pixels. The close alignment between experimental and simulation results shows the potential of the $Ag_2S$ device for artificial neural network hardware.

Interface RS exhibits superior energy efficiency compared to FTM in hardware-based computing. In this image processing demonstration, the total energy consumption arises from both the convolutional operation and the kernel encoding processes. During convolutional operations, multiplication and addition occur naturally after applying reading voltages, with power density directly scaling with the device conductance. Consequently, the ITM array (with $\sim 10^{-5}$ S conductance) substantially reduces energy consumption by two orders of magnitude compared to FTM (with $\sim 10^{-3}$ S conductance). Furthermore, we calculated the power consumption of the kernel encoding process by integrating the power of the setting pulse over the device's setting time. ITM-1 consumes $9.95 \times 10^{-10}$ J, approximately 300 times less than the energy consumed by FTM-1 (refer to Figure 4.4.2c and d). This significant reduction in energy consumption, coupled with processing accuracy comparable to simulations, demonstrates the advantages of employing low-conductance interface RS for energy-efficient computation. Finally, it is essential to note that the dot-point device array utilized in this study serves as a proof-of-concept for computing demonstrations based on interface RS-enabled FM hardware. The practical application will need integrating crossbar memristor array with peripheral circuits.

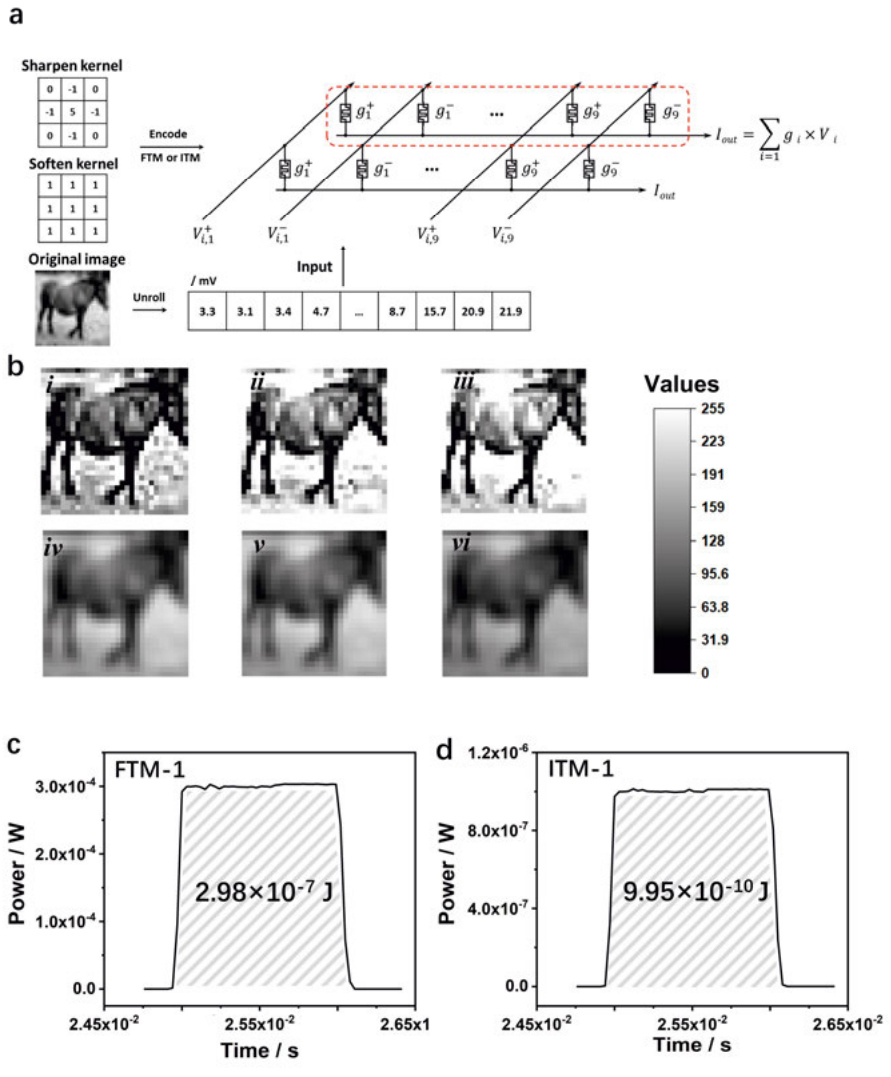


*Figure 4.2.2 (a) Convolutional kernel values are encoded into either an FTM or ITM $Ag_2S$ device array. The grayscale value of each pixel of the original image is mapped to the input voltage, which is fed to the top electrodes of different devices via a 3 × 3 input block. The postsynaptic current after MAC operation is recorded at the bottom electrode and back-transferred to grayscale values to generate the output image. (b) Software-based simulation result (i) and hardware outputs of FTM (ii) and ITM (iii) after sharpening operation. Software-based simulation result (iv) and hardware outputs of FTM (v) and ITM (vi) after softening operation. (c) Pulse power against elapsed time in the kernel encoding process for FTM-1. The energy consumption is calculated by integrating the pulse power against the device setting time. (d) Pulse power against elapsed time in kernel encoding process for ITM-1.*

## 4.3 Reduced cyclic variation of interface RS

Currently, many memristors employ the filamentary resistance switching mechanism for operation. However, the formation of conductive filaments necessitates the application of high-energy electrical pulses (as discussed in chapter 4.2), which result in the generation of significant overshoot currents within nanoseconds [81]. Consequently, precise control over filament size becomes challenging, thereby diminishing the tunability of conductance. Additionally, it has been well-established that the joule heating produced by these overshoot currents can lead to severe degradation of multiple minuscule filaments (formed within disordered defects and grain boundaries in amorphous or polycrystalline electrolytes). Consequently, these filament-based devices unavoidably exhibit substantial cycle-to-cycle variations due to the abundance of residual filaments [82], [83]. The stochastic nature of filament RS significantly undermines the computing accuracy of neural networks, especially when subjected to frequent weight update processes.

In this chapter, we demonstrate another advantage of filament-free interface resistance switching in $Ag_2S$-based memristors, showing its remarkable ability to significantly reduce cyclic variations. As shown in Figure 4.3.1a, when subjected to forward scanning voltage sweeps (ranging from 0 to -0.4 V), the device current exhibits an exponential increase by SBH modification at the $Ag_2S$/Ag interface. This interface resistance switching at the top nano-contact effectively turns on the $Ag_2S$ memristor. Upon reaching approximately -0.5 V, the Ag filament bridges the top and bottom electrodes, as indicated by a sudden and pronounced current jump in the plot. However, when subjected to repetitive triangle ±0.5 V setting/resetting biases, the residual filament effect becomes apparent. The threshold voltage for filament formation varies between -0.1 to -0.5 V across different cycles, introducing stochasticity and resulting in a wide distribution of ON state conductance. By reducing the setting/resetting biases to ±0.2 V, highly conductive filaments are no longer formed, effectively mitigating stochastic behavior and overshoot current. Consequently, the uniformity of switching under interface RS is significantly enhanced, as illustrated in Figure 4.3.1b. To quantitatively assess the cycle-to-cycle variation in RS, we conducted an endurance test spanning 10,000 cycles for both interface and filament RS, as summarized in Figure 4.3.1c. A statistical analysis of the ON state conductance (as depicted in Figure 4.3.1d) unequivocally reveals a substantially narrower conductance distribution for interface RS compared to filament RS. The ultra-small coefficient of variation ($C_v$), computed as 1.4% (obtained by dividing the standard deviation by the population mean to evaluate data dispersion), extracted from the interface RS data stands in direct contrast to the 28.9% of $C_v$ observed for filament RS.

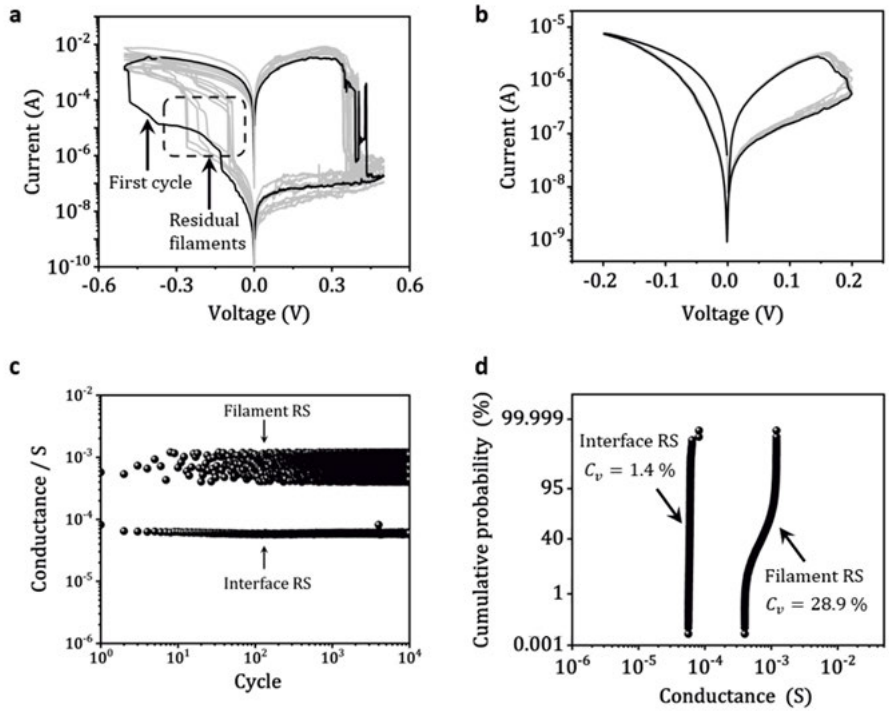


*Figure 4.3.1 (a) I-V characteristics of the filament RS in the $Ag_2S$ memristor under 10 repetitive 0→-0.5→0.5→0 V d.c. pulses. The filament RS leads to a wide distribution of forming voltage and ON state conductance. (b) I-V characteristics of the interface RS in the $Ag_2S$ memristor under 10 repetitive 0→-0.2→0.2→0 V d.c. pulses. The interface RS shows significantly improved switching uniformity. (c) The ON state conductance (read at 5 mV) of interface (under ± 0.2 V biases) and filament RS (under ± 0.5 V biases) during $10^4$ switching cycles. (d) The cumulative probability of the ON state conductance of the interface and filament RS during $10^4$ switching cycles. The coefficient of variation ($C_v$) is calculated to evaluate the dispersion of conductance.*

The reliable interface RS enables the $Ag_2S$-based memristors to emulate the synaptic plasticity for neuromorphic applications. Herein, we show that both short-term potentiation (STP) and long-term potentiation (LTP) can be realized by interface RS, and the transition between them can be controlled by the spike train applied to the device. Figure 4.3.2a shows the current response under a sequence of seven consecutive weak pulses (with an amplitude of -0.3 V, a duration of 100 μs, and a pulse interval of 100 μs). This sequence results in transient conductance increments, demonstrating a typical STP process. LTP can be achieved by extending the pulse duration to 1 ms (Figure 4.3.2b). Here, the post-synaptic current (PSC) exhibits a multi-step increase under consecutive strong pulses and stabilizes over a period of tens of seconds. We show

that the transition from STP to LTP can also be achieved by either increasing the pulse amplitude or reducing the pulse interval, as demonstrated in Figures 4.3.2c and d, respectively. With the capacity for controllable synaptic plasticity, the $Ag_2S$ artificial synaptic device array enables the demonstration of psychological "memory and forgetting" behavior. For demonstration, letters "I" and "L" were encoded into the same $Ag_2S$ memristor array (Figure 4.3.2e). This encoding is achieved by applying -0.3 V pulses in distinct patterns, with durations of 10 ms for "I" and 0.5 ms for "L". Afterwards, the conductance of each pixel was recorded as the memristor array was bent with a curvature radius of 3 mm. The letter "L" gradually fades after the input pulse and nearly gets removed within 30 seconds. By contrast, the letter "I" is exceptionally well-maintained in the LTP mode, exemplifying the dynamic capacity of the artificial synaptic device to mimic memory formation and retention.

To further evaluate the computing performance of interface RS, we conducted an image learning simulation of a 28 × 28 memristor-based neural network [84]. In this simulation (Figure 4.3.3a), the image sensor detects the pixel value of the input image and linearly maps the greyscale value to the target conductance. The presynaptic neurons are fully connected to the postsynaptic neurons via 28 × 28 synaptic devices, with the learnt synaptic weights updated towards the target conductance value. In each learning cycle, if the learnt synaptic weight ($w_{l(i)}$) is smaller than the target value ($w_{t(i)}$), a presynaptic spike is sent ahead of the postsynaptic spike, and vice versa. The initial states of 28 × 28 memristors were randomly distributed between 0 and 1. During each learning cycle, one integrated pulse containing pre-synaptic and post-synaptic spikes is sent to the memristors, and the synaptic weights of memristors evolve towards the corresponding target values to improve the learning accuracy. Different cycle-to-cycle variations in interface and filament RS, which were extracted in endurance characterization (see more details in **Paper III**), were introduced into the weight update process in the simulation.

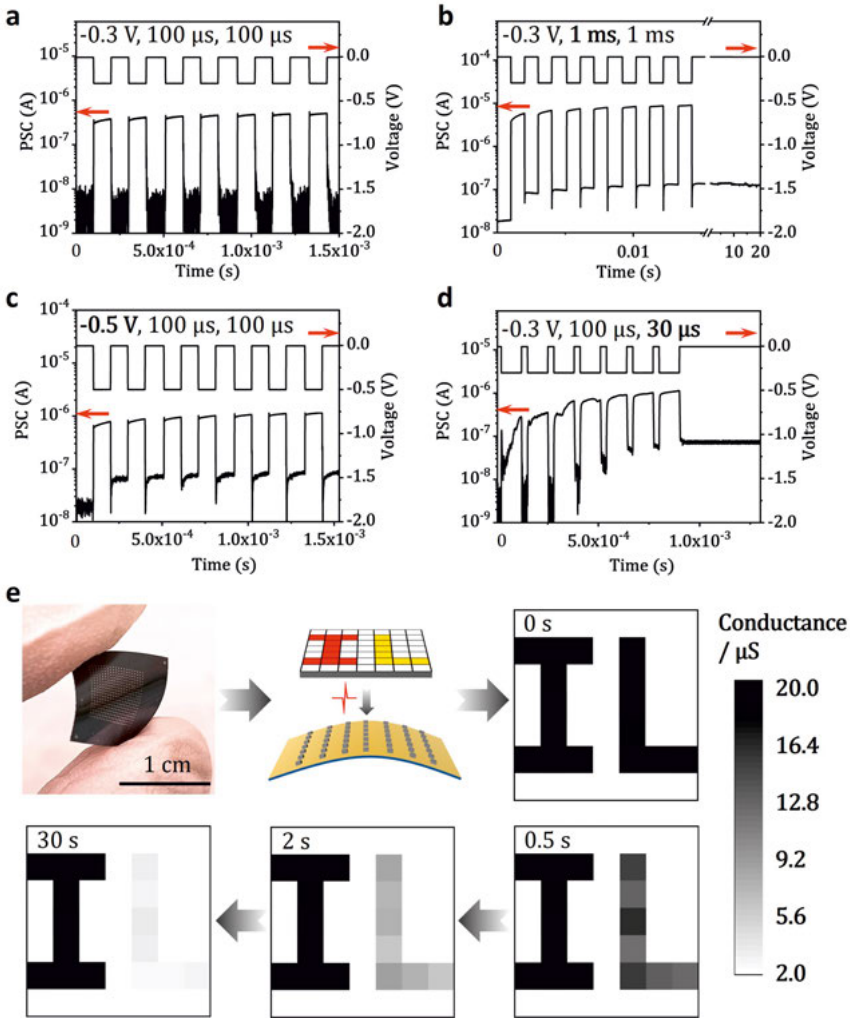


*Figure 4.3.2 Transition from STP to LTP under interface RS. (a) The recorded post-synaptic current during the application of pulses with -0.3 V amplitude, 100 µs duration and 100 µs interval, showing STP behavior. (b) The recorded post-synaptic current during the application of pulses with -0.3 V amplitude, 1 ms duration and 1 ms interval, showing LTP behavior. (c) The recorded post-synaptic current during the application of pulses with -0.5 V amplitude, 100 µs duration and 100 µs interval, showing LTP behavior. (d) The recorded post-synaptic current during the application of pulses with -0.3 V amplitude, 100 µs duration and 30 µs interval, showing LTP behavior. (e) Demonstration of "memory and forgetting" behavior on Ag2S device array. The enclosed optical photograph shows a bended device array. The letters "I" and "L" were encoded into a 7×7 $Ag_2S$ device array, with conductance evolution of each device against the elapsed time recorded.*

Figure 4.3.3b shows the calculated accuracy against the learning cycles. The neural network operated with interface RS exhibits rapidly improved accuracy in the first 30 cycles, and reaches a saturated value of 99.6 %. By contrast, the one operated with filament RS shows a smaller slope in the accuracy curve and a reduced saturation value of 94 %, indicating the degradation of learning ability caused by the large cycle-to-cycle variation. The visualization of the updated synaptic weights shown in Figure 4.3.3c provides the direct comparison of the learning ability between interface and filament RS. The pattern gradually gets recognizable and remains stable after 50 learning cycles, with more dead pixels observed in filament RS.

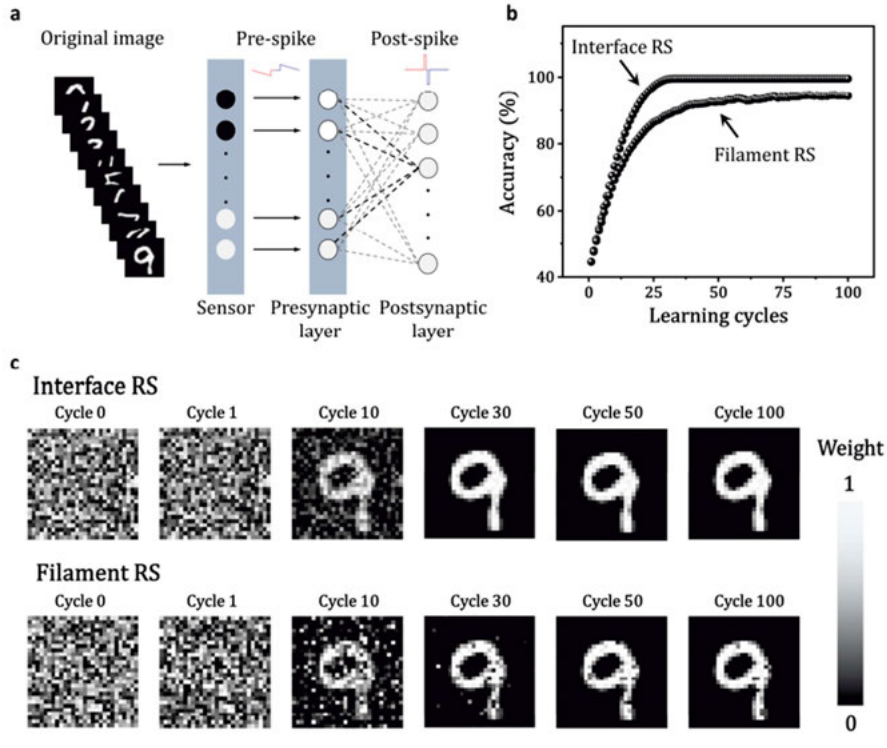


*Figure 4.3.3 The image learning demonstration on the neural network simulation. (a) The schematic illustration of the network structure. (b) The learning accuracy of networks operating with interface-type and filament-type synaptic devices. (c) The visualization of learnt patterns in different learning cycles.*

# 5. Integration of Wafer-Scale $Ag_2S$-Based Memristive Crossbar Array

Although some standalone memristors exhibit low switching-energy, most reported devices in crossbar arrays still consume much more energy than biological synapses (as discussed later in chapter 5.2) during device programming [29], [81], [84], [85]. This is mostly due to the slow kinetics in forming conducting paths inside the solid-state electrolyte. Some three-terminal ECRAMs can reduce their switching energy by limiting gate leakage current, but their fabrication is more complicated than 2-terminal devices, and is typically incompatible with CMOS technology for large-scale array integration [77], [86], [87]. CMOS-compatible memristive crossbar arrays with energy efficiency comparable to biological synapses are greatly desired for future energy-efficient computing.

In this chapter, we further demonstrate wafer-scale integration of $Ag_2S$-based memristive crossbar arrays, fabricated with a fully CMOS-compatible process. The switching-energy of the integrated memristive unit is approaching the one for biological synapses. Chapter 5.1 introduces the synthesis of $Ag_2S$ thin films and the fabrication of $Ag_2S$-based memristive crossbar array. The RS behavior and its kinetics behind of the obtained devices are discussed in chapter 5.2. We also demonstrate flexible memristor array on polymer substrates, and conduct computing applications on it, as shown in chapter 5.3.

## 5.1 Fabrication of $Ag_2S$-based memristive crossbar array

Figure 5.1.1a illustrates the $Ag_2S$ thin film synthesis through reactive sputtering technique. Before the deposition, the sputter chamber was evacuated to reach a high vacuum level of approximately $10^{-7}$ Torr to ensure the purity of the deposited films. After introducing Argon (Ar) gas into the chamber, radio frequency (RF) power was applied to initiate the formation of an Ar plasma, which was directed towards the high-purity silver target to eject Ag atoms. With complete reaction with hydrogen sulfide, these ejected Ag atoms yielded the as-synthesized $Ag_2S$ compounds. As the sputtering process continued, the $Ag_2S$ film grew on the rotating substrates, with a stable deposition rate of approximately 6 nm/s (detailed recipe can be found in **paper IV**).

To demonstrate large-scale film synthesis, we deposited an $Ag_2S$ film on a 4-inch $SiO_2$/Si wafer. The film morphology was analyzed utilizing AFM. The average surface roughness of the obtained film is ~3.5 nm, which is slightly larger than that of a $SiO_2$/Si substrate (~ 1 nm). This film uniformity is also evidenced by the mirror-like film surface (see Figure 5.1.1b and its insets). To analyze the chemical composition, RBS was conducted on the obtained film. The measurement result (Figure 5.1.1c) shows robust silver and sulfur signals at channel number ranges of 750-900 and 450-620, respectively. The best fit from quantitative simulation shows an Ag:S stoichiometry of 2:1, indicating the complete reaction between the ejected Ag atoms and $H_2S$ precursors. To set the phase structure, we annealed the as-deposited film at different temperatures (up to 160 $^oC$ for 3 hours in $H_2S$ ambient), and conducted XRD analysis. As shown in Figure 5.1.1d, the film after 160 $^oC$ annealing displays sharp peaks in the XRD diffractogram, which aligns well with the PDF for α-$Ag_2S$ crystals. The results demonstrate the wafer-scale synthesis of a polycrystalline $Ag_2S$ thin film in monoclinic phase.

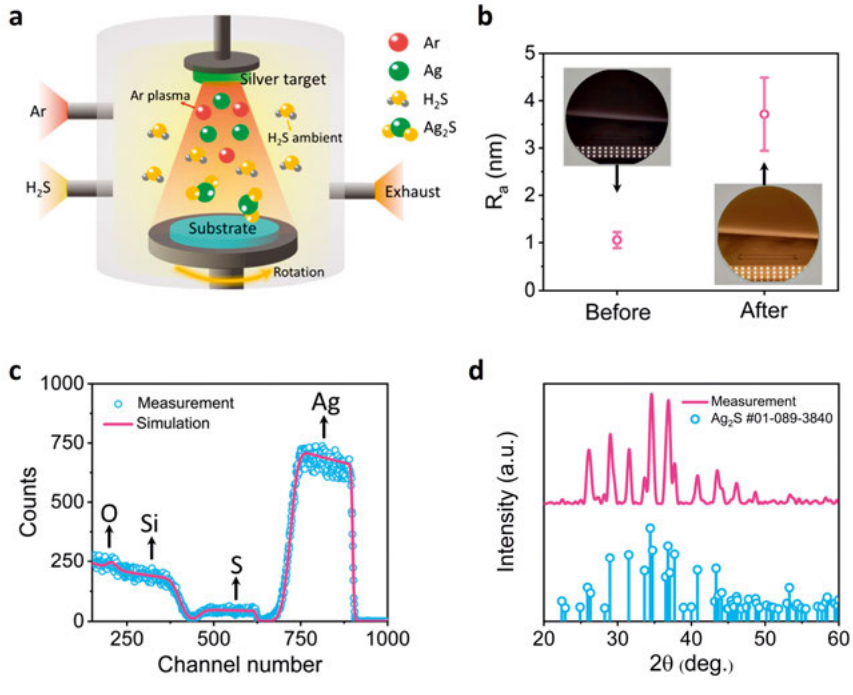


*Figure 5.1.1 (a) The schematic illustration of reactive sputter process for $Ag_2S$ thin film synthesis. (b) The average surface roughness before and after 50 nm $Ag_2S$ film deposition. The insets show optical photographs of the wafer before and after deposition. (c) The RBS spectra of the $Ag_2S$ film grown on $SiO_2$/Si substrate. (d) The XRD pattern of the $Ag_2S$ film (annealed at 160 °C) and the monoclinic $Ag_2S$ crystal.*

The synthesis of $Ag_2S$ films through low temperature reactive sputter retains the CMOS compatibility for the fabrication of $Ag_2S$-based memristive crossbar arrays. The fabrication started with forming bottom gold electrodes (50 nm thick) via consecutive metal deposition and lift-off processes on $SiO_2$/Si substrates. Subsequently, the $Ag_2S$ film was sputtered on the whole wafer, followed with a lift-off process to create square $Ag_2S$ islands at the cross-points. After forming top silver electrodes, post annealing processes were performed to set the microstructure of the $Ag_2S$ electrolyte. A global view of the fabricated memristor arrays on a 4-inch wafer is shown in Figure 5.1.2a. In each array, 150×150 $Ag_2S$-based devices (each with a lateral dimension of 5×5 $\mu m^2$) are formed at the cross-points between the top and bottom electrodes (Figure 5.1.2b). The memristive crossbar array is a promising candidate for in-memory computing. By applying voltages to specific columns, the selected memristive unit in crossbar array can be programmed to store information, and device currents can be collected at corresponding rows to conduct analogue data processing, as schematically illustrated in Figure 5.1.2c. The zoomed-in SEM images (Figure 5.1.2d and e) provide further insights of the crossbar array, with the sandwiched layer stack of a single Au/$Ag_2S$/Ag cell unit revealed by the cross-sectional SEM image in Figure 5.1.2f.

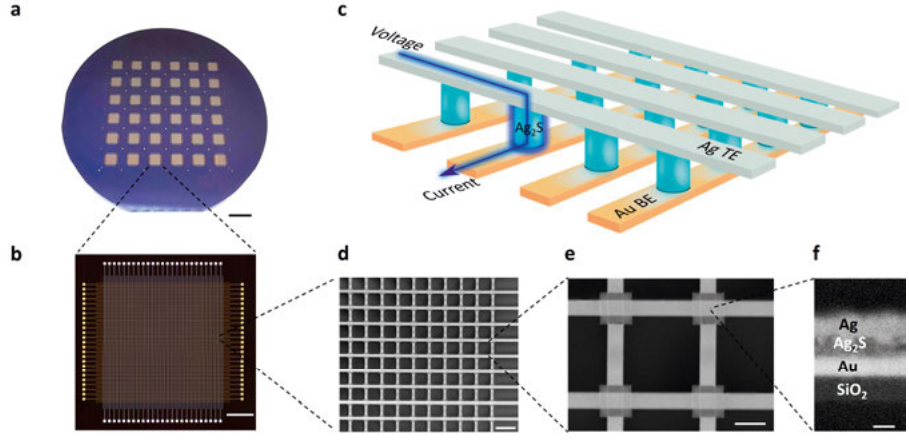


*Figure 5.1.2 (a) The optical image of the $Ag_2S$-based memristor crossbar arrays fabricated on 4-inch $SiO_2$/Si wafer. Scale bar, 1 cm. (b) The optical micrograph of a 150×150 memristive array. Scale bar, 1 mm. (c) Schematic illustration of the crossbar structure. At each cross-point, the $Ag_2S$ electrolyte is sandwiched between a silver top electrode (Ag TE) and a gold bottom electrode (Au BE). (d) The SEM images of a sub-array. Scale bar, 30 μm. (e) The SEM images of a 2×2 sub-array. Scale bar, 10 μm. (f) The cross-sectional SEM image of an Au/ $Ag_2S$/Ag memristive unit. Scale bar, 50 nm.*

## 5.2 RS characteristics of the $Ag_2S$-based memristor

To investigate the memristive behavior of the fabricated device, we conducted d.c. I-V measurements by applying voltages to the top silver electrode (with the bottom electrode grounded). As depicted in Figure 5.2.1a, an Au/$Ag_2S$ (50 nm thick)/Ag unit exhibits a typical bipolar RS behavior. Negative voltage can accumulate $Ag^+$ ions at cathode $Ag_2S$/Ag interface and reduces them to continuous silver filaments, as characterized by an abrupt increase in current at approximately -0.3 V. The resulted LRS remains stable until a positive voltage is applied to reset the device back to HRS, offering a substantial dynamic range over six orders of magnitude. Notably, the device demonstrates a low threshold voltage ($V_{th}$) for continuous filament formation (read out as the voltage at which the sudden increase in current occurs in the d.c. operation). A statistical analysis of the $V_{th}$ from 30 devices (as summarized in Figure 5.2.1b) demonstrates a distribution ranging from -0.1 V to -0.4 V, with an average value of -0.22 V from a Gaussian fit. This mean $V_{th}$ is significantly lower than values observed in state-of-the-art 2D material-based memristors (typically ~1V). The highest LRS conductance of the device could reach milli siemens (mS) regime, with a device-to-device variation (evaluated by coefficient of variation $C_v$) approaching 0.6 as shown in Figure 5.2.1c. Such variations are resulted from the inherent stochastic nature of filament formation along the defects and grain boundaries inside the electrolyte [21], [88], [89]. To mitigate this variation in practical array operation, selectors (e.g. transistors) or peripheral circuits are often integrated to improve the tunability of RS in memristors [90]. Here we demonstrate the modulation of the LRS conductance by implementing current compliance ($I_{cc}$) during d.c. settings. As summarized in Figure 5.2.1d, $I_{cc}$ could reduce $C_v$ to below 0.1, decreasing mean conductance value by two orders of magnitude. Furthermore, the conductance of these states (read by 5 mV bias) remains stable over 1000 seconds (Figure 5.2.1e). This LRS conductance modulation with exceptional retention allows devices operating at lower conductance range, which is crucial for reducing both sneak path currents and switching energy [91], [92]. Moreover, the device was subjected to repeated RS across the full dynamic range, revealing robust switching endurance over $10^4$ write-read cycles (Figure 5.2.1f).

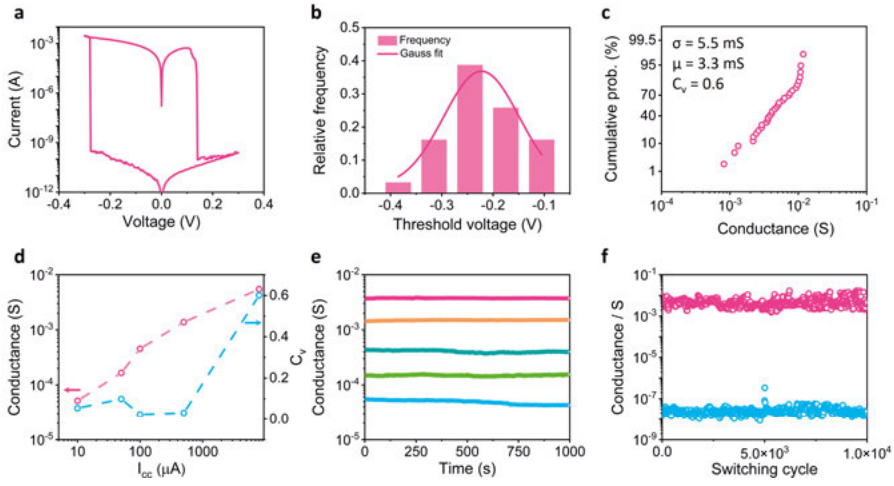


*Figure 5.2.1 (a) The I-V characteristics of the device under 0→-0.3→0.3→0 V d.c. bias. (b) The distribution of Vth measured from 30 devices and its Gauss fit. (c) The cumulative probability of the highest LRS conductance. The mean value (σ), standard deviation (μ) and coefficient of variation ($C_v$) are calculated. (d) The mean conductance value (red-marked) and their coefficient of variation (blue-marked) under different current compliance (10 μA, 50 μA, 100 μA and 500 μA) during d.c. settings. (e) The retention of conductance read under 5 mV bias. (f) The endurance of the device under $10^4$ switching cycles.*

The small $V_{th}$ value suggests fast kinetics of $Ag^+$ migration and redox processes within our $Ag_2S$-based device. To provide deeper insights, we conducted in-situ SEM observations of the electrochemical process in polycrystalline $Ag_2S$ films. The repeated electron beam scanning during SEM imaging could induce $Ag^+$ migration (towards the film surface) and subsequent reduction (at the surface). This was evidenced by the rapid growth of silver clusters on $Ag_2S$ film surface under SEM imaging (Figure 5.2.2a and b). Furthermore, Figure 5.2.2c displays a silver particle induced during SEM analysis, whose chemical composition was confirmed by energy-dispersive spectroscopy (EDS). Silver clusters were also observed during cross-sectional SEM analysis of an Au/$Ag_2S$/Ag memristor cell, as highlighted by dashed lines in Figure 5.2.2d. The direct observation of Ag clusters within the memristor reflects the fast $Ag^+$ migration and reduction, which aligns with the small $V_{th}$ observed in electrical measurements.

Early material studies concluded that dominant ion carriers in monoclinic $Ag_2S$ are the Frenkel defect-induced interstitial $Ag^+$ ions, which effectively migrate between adjacent tetrahedral and octahedral sites in their crystals [93]–[96]. This process within the crystal lattice (instead of the grain boundary)

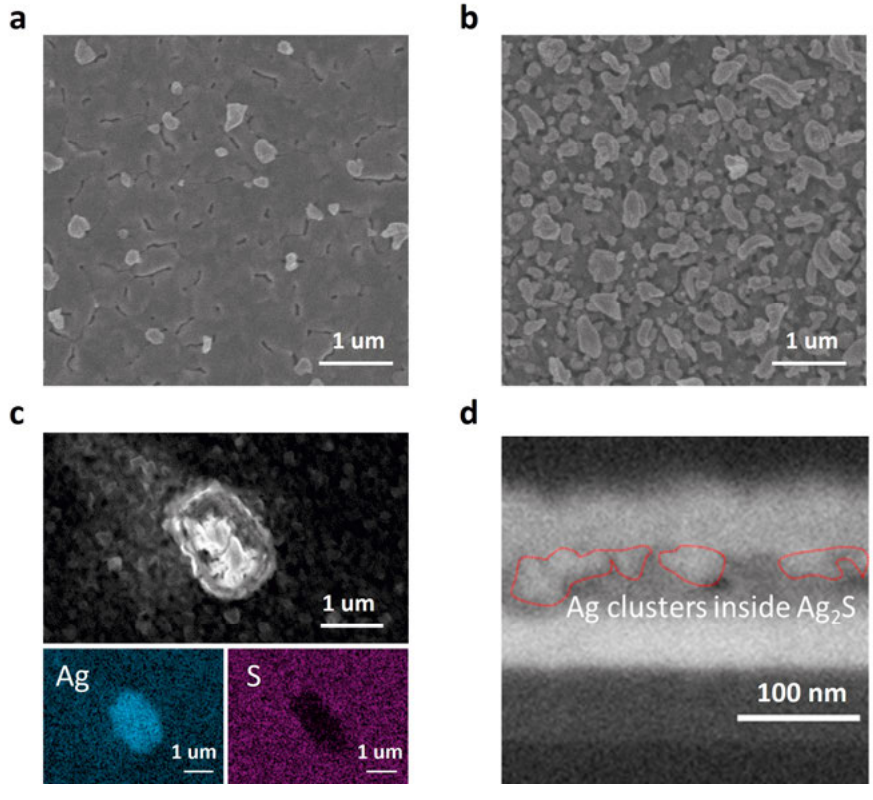


*Figure 5.2.2 In situ SEM (with accelerating voltage at 4.5 kV) images of an $Ag_2S$ film surface taken before (a) and after (b) repeated electron beam scanning for 40 s. (c) SEM (with accelerating voltage at 4.5 kV) image of the $Ag_2S$ film (top), with a participated silver cluster on the surface, and the corresponding EDS images (bottom-left for Ag signals and bottom-right for S signals). (d) Cross-sectional SEM image of an Au/$Ag_2S$/Ag cell taken under 2 kV accelerating voltage. The red dash line highlights the electron-beam induced silver clusters in the $Ag_2S$ layer.*

suggests that larger grain sizes could lower the energy barrier for $Ag^+$ ion migration. Based on this understanding, we post-annealed the deposited $Ag_2S$ films with varying temperatures to modulate the film microstructure. Considering the susceptibility of $Ag_2S$ films to electron beams, we utilized AFM to investigate the surface morphology. Compared with the as-deposited film, the one after 160 $^oC$ post-annealing clearly exhibits larger grain size (Figure 5.2.3a). Devices fabricated with higher post-annealing temperatures indeed required smaller setting voltages to form continuous silver filaments, as summarized in Figure 5.2.3b. To further confirm the impact of grain structure, we examined devices with varying thicknesses of $Ag_2S$ electrolytes. AFM analysis revealed that as film thickness increased from 50 nm to 200 nm (after 160 $^oC$ post annealing), the average surface roughness linearly increased,

indicating larger grain sizes in thicker films. Experimental results show that devices with thicker $Ag_2S$ electrolytes exhibit further reduced $V_{th}$ (Figure 5.2.3c). Notably, the Au/$Ag_2S$ (200 nm, 160 $^oC$ annealed)/Ag memristor devices displayed a $V_{th}$ at approximately -0.1 V (see I-V characteristics in Figure 5.2.3d), representing the lowest reported value to our knowledge.

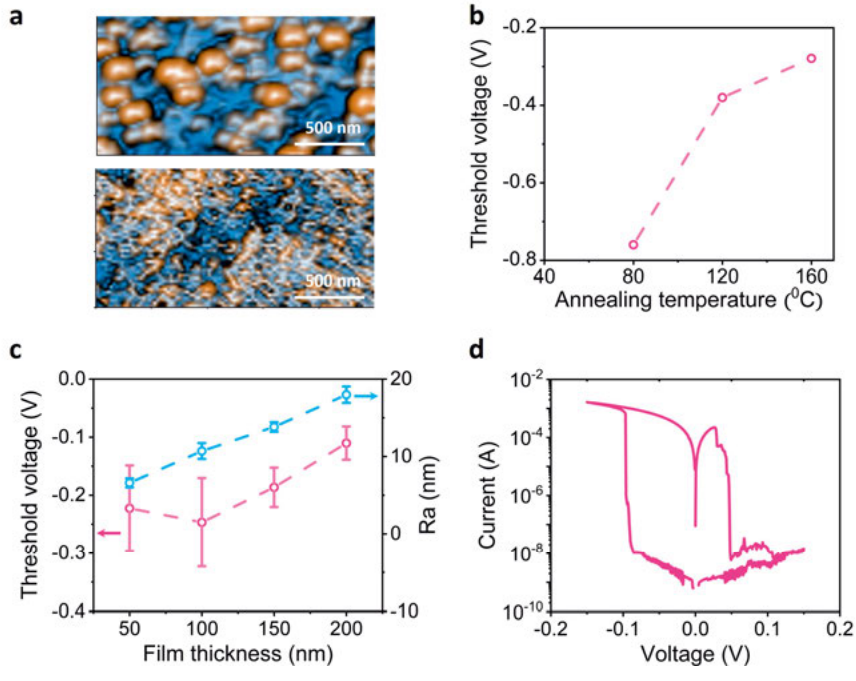


*Figure 5.2.3 (a) Color-coded AFM images of the raw $Ag_2S$ film (bottom) and the 160 °C-annealed $Ag_2S$ film (top). (b) The threshold voltage of the $Ag_2S$ (50 nm)-based memristors fabricated with different annealing temperatures. (c) The threshold voltage of the $Ag_2S$ (160 °C-annealed)-based memristors fabricated using $Ag_2S$ films with different thickness. (d) The I-V characteristics of the device with 200 nm $Ag_2S$ films (160 °C-annealed).*

Given the fast kinetics of $Ag^+$ ion migration and redox, our $Ag_2S$-based memristors hold the promise for rapid and energy-efficient operations. We applied short write-read pulses to Au/$Ag_2S$ (200 nm, 160 $^oC$-annealed)/Ag devices, and monitored the current response. Figure 5.2.4a shows that three successive write pulses (-0.3 V, 1 μs) gradually increase the peak device current. A zoomed-in view at the reading process (Figure 5.2.4b) further demonstrates the discrete conductive states under fast programming. The switching energy of each rapid writing process was calculated to be approximately 20 fJ, which is comparable to the energy consumed per synaptic event in human synapses. Compared with recently reported CMOS-

compatible memristive crossbar arrays, our device exhibits the lowest switching energy (Figure 5.2.4c) [90], [97]–[101].

It is crucial to note that the operation speed of the memristor is not only limited by conductance modulation but also by conductance readouts. During fast programming, the transition from write to read pulses (as green-shaded Figure 5.2.4a and b) induces a current recovery process. This transient behavior, known as resistor-capacitor delay [90], arises as the parasitic capacitance of the memristor starts to charge/discharge during the voltage switching, which stabilizes after complete charge transfer. Our Au/$Ag_2S$ (200 nm, 160 $^oC$-annealed)/Ag device exhibits a recovery time of about 5 µs, suggesting a write–read operation frequency approaching sub-megahertz in the crossbar array. It is worth noting that the lateral device dimension directly correlates the device current and the parasitic capacitance, and thus both the energy efficiency and the programming speed of our $Ag_2S$-based memristive crossbar array could be further improved by device downscaling.

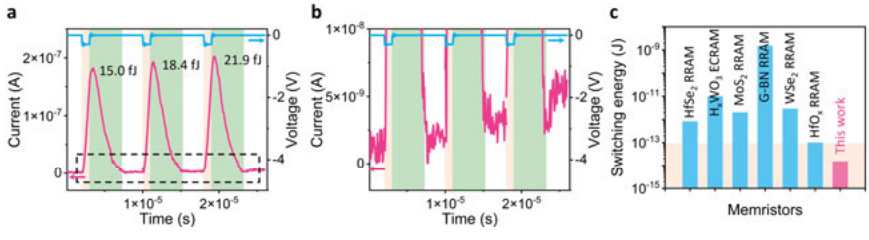


*Figure 5.2.4 (a) The current trace of the $Ag_2S$-based device (200 nm, 160 °C-annealed) under write (-0.3 V, 1 µs)-read (5 mV) pulses. The switching energies of each writing pulse are calculated by integrating the product of the voltage and the current over the writing time. The pink and light green shadings highlight the writing and the recovery time, respectively, and the regime in black dashed line is zoomed-in as (b). (c) Comparison of switching energy between the $Ag_2S$-based device and recently reported memristors in their CMOS-compatible arrays. The pink shading marks the switching energy of biological synapses per synaptic event.*

## 5.3 Demonstration of neuromorphic computing using $Ag_2S$-based flexible memristive crossbar array

The low temperature (≤ 160 °C) fabrication of the $Ag_2S$-based memristive crossbar array retains the full compatibility with CMOS technology and makes it promising for integration in wearable electronics. To validate this potential, we fabricated the same selector-less $Ag_2S$-based memristive array on flexible polyimide substrates (see Figure 5.3.1a), and conducted the on-chip MAC operations on it. In this demonstration, 3×3 digital kernels for vertical and horizontal edge detection were encoded into the analogue conductance of 18 memristors in the crossbar, with a differential pair of devices to represent both positive and negative kernel values. The pixel values (ranging from 0 to 255) of input images were then linearly transferred into the voltage of read bias (ranging from 0 to 25.5 mV), which was fed to different rows of crossbar array. Consequently, an overall current, weighted from the encoded conductance, can be collected in the shared column. This current represents the output of a convolution process utilizing analogue MAC operation. Convoluting across the entire input image results in an output image, as illustrated in Figure 5.3.1b). Notably, the 6 LRS memristive units representing the kernel values of those "1" and "-1", dominate the overall output current in a MAC operation, while the units at HRS representing those "0" contribute negligible differential currents. This is illustrated by the significant difference between the encoded "1" (red-marked), "0" (green-marked) and "-1" (blue-marked) in vertical edge detection kernel (Figure 5.3.1c). In Figure 5.3.1d, we show the differential currents of the 6 encoded LRS memristive units in the flexible array (bent with a 3 mm radius). Their linear I-V relationships under the entire input voltage window validate the analogue MAC operations through Ohm's law and Kirchhoff's current law. As a proof-of-concept demonstration, we established a dataset of MAC operations based on the differential currents of these 6 memristors, allowing the reference of corresponding output currents for any input voltages. Figure 5.3.1e and f provide a comparison of output images between hardware processing and software simulation for vertical edge detection and horizontal edge detection, demonstrating the tolerable device-to-device variation in our flexible memristive array during image processing.

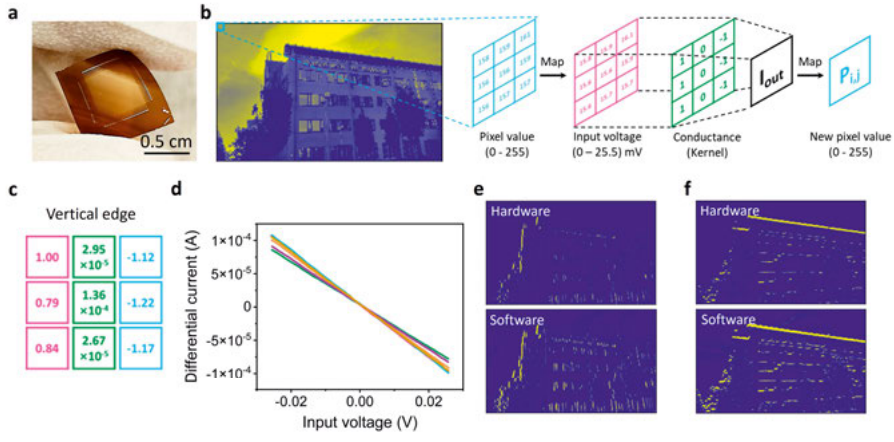


*Figure 5.3.1 (a) (a) Optical photography of a flexible memristive crossbar array fabricated on polyimide substrate. (b) Schematic illustration of image processing on the memristive crossbar array. (c) The encoded kernels for vertical edge detection. Red, green, and blue-marked values represent the "1", "0" and "-1" respectively. (d) The differential currents of 6 dominant LRS memristors, whose conductance represents the kernel values of those "1" and "-1". (e) The output image from hardware and software processing after vertical edge detection. (f) The output image from hardware and software processing after horizontal edge detection.*

In addition to MAC operations (for data propagation), we also demonstrate continuous potentiation/depression (for weight updates) in the flexible array. As depicted in Figure 5.3.2a, programming a memristive unit under a 3 mm bending radius was achieved through 1200 up-and-down pulses (±0.3V, 1 µs for 30-cycle potentiation/depression). The maximum conductance during this 1200-step modulation exhibited a $C_v$ at 6%, and the inherent non-linear switching characteristics were also evident in repeated weight update cycles. Based on this, we simulated an image classification task using the Modified National Institute of Standards and Technology (MNIST) dataset. The 4-layer DNN architecture, illustrated in Figure 5.3.2b, contains 784 input neurons, 256 and 128 hidden neurons, and 10 output neurons. The experimental conductance modulation results, considering non-linearity, asymmetry, and variations, were utilized as the characterization of non-ideal synaptic devices to control the synaptic strength between neurons. After training 10 epochs with conventional SGD algorithm, the DNN with $Ag_2S$-based memristors achieved a recognition accuracy of 78.4% on the testing dataset, which is lower than the 93.2% accuracy achieved by ideal devices (without non-linearity and asymmetry). We show that the impact of inherent non-ideality can be compensated by a specialized in-memory SGD training algorithm, referred as TTV2 [51], [53]. This advanced DNN employs two matrices (A and C) to

store weight information, and connects them with a low-pass filter (H), as illustrated in Figure 5.3.2b. By employing the symmetry point shifting technique during weight update in matrix A, the randomness from the input data (unintended features, acting as short-term noise) was significantly reduced. After further filtering by the low-pass function of matrix H, true features were effectively propagated to matrix C, updating the weights towards their optimized values. The simulation results of our $Ag_2S$-based advanced DNN reach a remarkable saturation accuracy of 92.6%, despite the inherent non-idealities in the memristive units. Moreover, the accuracy of the $Ag_2S$-based DNN with TTV2 converged quickly after 3 training epochs, in direct comparison with that from conventional SGD. This result demonstrates that the TTV2 algorithm compensates for the intrinsic non-idealities of the integrated memristors, significantly improving both the training accuracy and training speed.

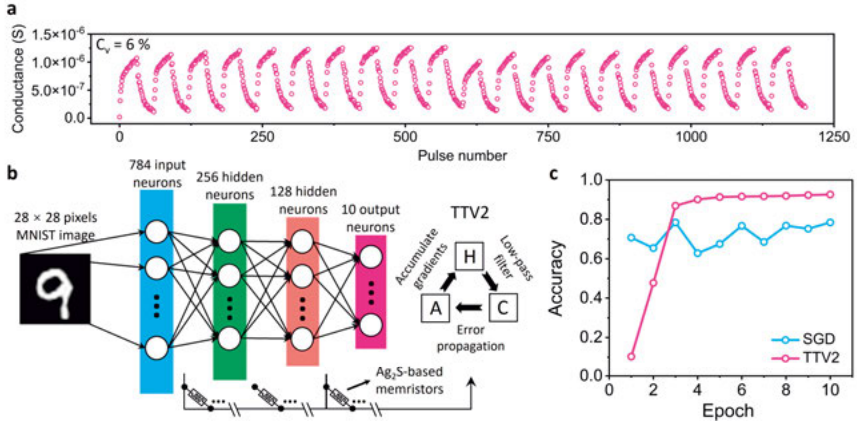


*Figure 5.3.2 (a) Programming of the $Ag_2S$-based flexible memristors by consequent 30 potentiation pulses (-0.3 V, 1 µs) and 30 depression pulses (0.3 V, 1 µs). Cv of 6 % was calculated from the maximum conductance during 1200-step programming to evaluate cycle-to-cycle variation. (b) Schematic illustration of the DNN architecture. The conventional SGD and TTV2 are utilized as training algorithms, respectively. In TTV2, the weights are stored in two matrices (A and C), and matrix H serves as a low-pass filter to minimize the randomness from the inputs. (c) The simulation accuracy of DNN with the $Ag_2S$-based memristors using SGD or TTV2 as the training algorithm.*

# 6. Conclusions and Future Perspectives

The main purpose of this thesis is to study the resistance switching behavior of $Ag_2S$-based flexible memristors, and to explore their applications in neuromorphic computing. To pursue the goal, we start with fabricating flexible memristors (FMs) using thick $Ag_2S$ films, and investigate their resistance switching (RS) mechanism. Afterwards, the CMOS-compatible integration of wafer-scale $Ag_2S$-based memristor crossbar array is achieved, and its computing capabilities are demonstrated. The conclusions are summarized as follow:

1. Full-inorganic FMs are demonstrated utilizing free-standing thick $Ag_2S$ films. The devices exhibit a remarkable ON/OFF ratio of $10^6$ at ±0.5V setting/resetting bias, and operate with high-density non-volatile conductive states. The stable RS can be retained when FMs are bent with 3 mm curvature radius, with exceptional endurance (over 1000 cycles) and retention (over $10^4$ s). It is confirmed that the RS in the thick $Ag_2S$ film-based FMs is induced by the sequential Schottky barrier height (SBH) modulation at the $Ag/Ag_2S$ interface and the continuous silver filament formation inside the electrolyte, which can be realized by an asymmetric contact geometry as demonstrated in this thesis.
2. Sole interface RS by SBH modulation is achieved in the same thick $Ag_2S$ film-based FMs. This unique RS only relies on $Ag^+$ ion migration and accumulation/depletion at the cathode interface, eliminating the need for continuous filament formation. Compared with conventional filamentary memristors, an ultra-low switching energy of ~0.2 fJ is achieved in the FM. The hardware-based image processing of interface RS indeed consumes two orders of magnitude lower energy than filament RS measured in the same devices.
3. The click variation in thick $Ag_2S$ film-based FMs can be significantly reduced by interface RS, due to the avoided stochasticity in filament formation and ablation. And the synaptic functions such as short-term potentiation (STP), long-term potentiation (LTP) and psychological "memory and forget" behavior can be emulated by the interface RS in the device. An artificial neural network simulation further confirms the reduced cycle-to-cycle variations in interface RS improve the image learning ability of artificial neural network.

4. Wafer-scale integration of $Ag_2S$-based memristive crossbar arrays with low thermal budget under 160 $^oC$ is demonstrated. The $Ag_2S$ thin films are synthesized by reactive sputtering and the memristors are fabricated using CMOS-compatible processes. The integrated $Ag_2S$-based memristive unit exhibits a record low threshold voltage of ~ -0.1V in d.c. operation to form continuous silver filaments. Under fast operation at sub-megahertz frequency, the device achieves an ultra-small switching energy of ~15 fJ, which is comparable to that of biological synapses in human brains. The same crossbar array is demonstrated on polyimide substrates for flexible electronics application. The obtained flexible device array enables analogue multiply-accumulate calculations for image processing, and their inherent non-linear switching characteristics can be significantly compensated by the advanced training algorithm in deep learning neural networks (DNNs). The image recognition simulation yields an impressive image recognition accuracy of 92.6%, demonstrating its potential for fast and energy-efficient neuromorphic computing.

Based on the studies discussed in this thesis, the fabrication of memristive crossbar array is developed, basic knowledge on resistance switching inside $Ag_2S$ materials is accumulated, and the corresponding computing application is demonstrated. In future work, dedicated efforts should be devoted to explore the following issues.

1. The interface RS by SBH modulation is realized by forming asymmetric contact geometry to ensure that the contact resistance at cathode interface dominates the total device resistance. The same purpose can be potentially achieved by forming a stable ohmic contact at the counter anode interface in a symmetric contact geometry. The strategy holds the promise to induce interface RS in memristive crossbar array for further performance optimization.
2. The $Ag^+$ ion migration and redox play a vital role in resistance switching. More studies should be conducted to explore the details of the electrochemical process. For example, the impact of $Ag_2S$ film microstructure on $Ag^+$ ion migration and redox needs to be further investigated and characterized. A deeper understanding on the kinetics helps to both improve device operation speed and reduce device switching energy.
3. Memristive crossbar array should be monolithically integrated with peripheral circuits as a deep learning accelerator for neuromorphic computing. In this thesis, selector-less memristive crossbar array is demonstrated. And the CMOS-compatible integration of selectors should be explored to better controlling RS in memristive units.

# Sammanfattning på svenska

Huvudsyftet med denna avhandling är att studera det resistiva switchningsbeteendet hos $Ag_2S$-baserade flexibla memristorer och att utforska deras tillämpningar inom neuromorfiska beräkningar. För att uppnå detta mål börjar vi med att tillverka FM-enheter med tjocka $Ag_2S$-filmer och undersöka deras RS-mekanism. Därefter färdigställs den CMOS-kompatibla integrationen av en $Ag_2S$-baserad memristormatris på en kiselskiva och dess beräkningsförmåga demonstreras. Slutsatserna sammanfattas enligt följande:

1. Helt oorganiska FM-enheter demonstreras genom användning av fristående tjocka $Ag_2S$-filmer. Enheterna uppvisar ett anmärkningsvärt PÅ/AV-förhållande på $10^6$ vid ±0.5 V inställnings-/återställningsförspänning och arbetar med hög densitet av icke-flyktiga ledande tillstånd. Den stabila RS kan bibehållas när FM-enheter böjs med en krökningsradie på 3 mm, med exceptionell uthållighet (över 1000 cykler) och retention (över $10^4$ s). Det bekräftas att RS i FM-enheter baserade på tjocka $Ag_2S$-filmer induceras av sekventiell SBH-modulering vid gränssnittet mellan Ag/$Ag_2S$ och kontinuerlig silverfilamentbildning inne i elektrolyten, vilket kan realiseras genom en asymmetrisk kontakgeometri vilket demonstrerats i denna avhandling.
2. RS enbart vid gränssnittet genom SBH-modulering uppnås i samma FM-enheter baserade på tjocka $Ag_2S$-filmer. Detta unika RS förlitar sig endast på $Ag^+$-jonmigration och ackumulering/uttömning vid katodgränssnittet och eliminerar behovet av kontinuerlig filamentbildning. Jämfört med konventionella memristorer baserade på filamentbildning uppnås en extremt låg switchningsenergi på ~0.2 fJ i FM-enheten. Hårdvarubaserad bildbehandling av RS vid gränssnittet förbrukar så lite som två storleksordningar mindre energi än filamentbaserad RS uppmätt på samma enheter.
3. Klickvariationen i FM-enheter baserade på tjocka $Ag_2S$-filmer kan minskas betydligt genom RS vid gränssnitet på grund av undvikandet av stokasticitet i filamentbildning och ablation. Och synaptiska funktioner som STP, LTP och psykologiskt "minnas och glömma"-beteende kan emuleras av RS i gränssnittet i enheten. En simulering av artificiella neurala nätverk bekräftar ytterligare att de minskade

cykel-till-cykel-variationerna hos RS i gränssnittet vilket förbättrar bildinlärningsförmågan hos artificiella neurala nätverk.

4. Integration av $Ag_2S$-baserade memristormatriser med låg termisk budget under 160 °C på kiselskiva demonstreras. De tunna $Ag_2S$ filmerna syntetiseras med reaktiv sputtring och memristorerna tillverkas med hjälp av CMOS-kompatibla processer. Den integrerade $Ag_2S$-baserade memristorenheten uppvisar en rekordlåg tröskelspänning på ~-0.1 V vid likströmsdrift för att bilda kontinuerliga silverfilament. Under snabb drift vid frekvenser under megahertzområdet uppnår enheten en extremt liten switchningsenergi på ~15 fJ, vilket är jämförbart med biologiska synapser i mänskliga hjärnor. Samma korsstångsmatris demonstreras på polyimidsubstrat för böjbara elektroniktillämpningar. Den erhållna flexibla matrisen möjliggör analoga multiplikationsackumuleringsberäkningar för bildbehandling, och deras inneboende icke-linjära switchningsegenskaper kan till stora delar kompenseras av den avancerade träningsalgoritmen i DNN. Bildigenkänningssimuleringen ger en imponerande bildigenkänningsnoggrannhet på 92.6%, vilket visar dess potential för snabb och energieffektiva neuromorfiska beräkningar.

# Acknowledgement

First and foremost, I would like to express my deepest gratitude to my main supervisor, Professor Zhen Zhang, for the invaluable guidance and unwavering support throughout my entire PhD study. The essence of scientific research lies in unravelling and proving the unknown: a journey that is challenging but meaningful under your guidance. I recall moments when faced with complex experimental phenomena, and you always encourage me to persist in exploration. Your dedication and sense of responsibility towards my research work offer new perspectives to me in every discussion. It is with deep appreciation that I acknowledge your indispensable contribution to the content of this thesis.

I extend my sincere appreciation to my co-supervisor, Professor Xun Shi. Your insightful feedback, constructive criticism, and collaborative spirit have significantly enriched the depth and quality of my research. Despite the geographical distance, your timely assistance has been a constant support to me. Throughout our collaborative journey over the past years, I have not only acquired a lot of specific knowledge through our discussions but also gained valuable insights into visualizing scientific research. I am grateful for the expertise and dedication you have brought to my PhD study.

I would like to thank all the people involved in my research project. Thank you, Dr. Si Chen, for your invaluable assistance in cryogenic measurements and insightful discussions throughout my PhD study. Thank you, Dr. Paul Solomon and Dr. Malte Rasch for your support in deep learning. Your guidance has been instrumental in expanding my knowledge of neuromorphic computing, spanning from its fundamental physical principles to practical applications. Thank you, Dr. Tomas Nyberg, for your technical support in reactive sputter. The time we spent together in the clean room is impressive, providing me with profound insights to the vacuum technology and the thin film deposition. Thank you, Prof. Daniel Primetzhofer, for the fruitful cooperation on material analysis. Your expertise and collaborative spirit significantly enriched my research experience. Thank you, Prof. Leif Nyholm. Your erudite knowledge in electrochemistry has greatly enhanced my understanding of the ion migration and redox inside our $Ag_2S$-based memristors, and I thoroughly enjoy our discussions. Thank you, Prof Andreas Lindblad, for the generous assistance on X-ray photoelectron spectroscopy analysis. I learn a lot from the discussions with you. Thank you, Dr. Örjan

Vallin, Dr. Amit Patel and all the staffs in Myfab. I want to express great thanks for your technical supports in the clean room.

I am deeply grateful to all my colleagues in the division. Thank you, Prof. Shili Zhang. As the division head, your enduring passion and cautious attitude towards scientific research have inspired us to consistently overcome challenges in our projects. Thank you, Ida Näslund, Maria Brandt and Linn Eriksson, for your constant help in various administrative aspects, including product purchases, visa applications and document processing. Thank you, Dr. Tomas Kubart, for the fruitful discussions in seminars and courses. Thank you, Dr. Dragos Dancila, for your efforts in organizing and holding our Friday seminars. I would like to thank Ted Johansson, Zhibin Zhang, Ngan Pham, Michelle Marie Villamayor, Robert Zando, George Alhoush, Tereza Kosutova and all other colleagues who have contributed to the collaborative spirit within our division. Your diverse perspectives and collective efforts have played a vital role in creating a vibrant and intellectually stimulating research environment, making the research journey not only productive but also enjoyable.

Great acknowledgement is given to the Swedish Strategic Research Foundation, the Swedish Research Council, and the Wallenberg Academy Fellow Program for the financial support.

I would like to express my appreciation to my home country, China. The values and culture of China have shaped my identity and provided a strong foundation for my academic pursuits.

I am thankful to my friends in Sweden. Thank you, Xingxing Xu, Qitao Hu, Shuangshuang Zeng, Jiaqi Lu, Shiyu Li, Renbin Tong, Libo Chen, Chenyu Wen, Yao Yao, Yupeng Yang, Lei Tian, Rui Sun, Huan Wang, Shengyang Zhou, Bei Wang, Pei Fu, Yawen Liu, Zhenhua Liu, Jing Xu, Chen Chen, Yuan Cui, Qian Shi, Yu Pan, Shan Jiang, Jiaqi Xing, Yingtao Yu, Zheqiang Xu, Funing Liu, Yihan Wang et al. The activities and moments we have had together are the most cherished time in the past years.

A special thank you to my girlfriend, Xueying Kong. The Swedish winter, with its long nights and cold embrace, has been transformed into a time filled with light and warmth by your understanding and support. I may not always find the right words to articulate my feelings, but I want to take this moment to deliver the love and the appreciation for you. Just as this thesis represents a significant chapter in my journey, your companionship has been an inseparable part of my life. I eagerly anticipate a future filled with happiness, where our mutual support propels us towards the realization of our dreams and aspirations.

最后，向我的爸妈，家人们表达最深的感谢。你们的理解与支持陪伴我一路走到现在，并将给予我继续向前的动力。

Yuan Zhu

祝渊

2023-11-21, Uppsala

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