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Design and Simulation of Power Converter for a grid connected 24 MW Floating Offshore Wind Turbine

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Abstract

This thesis addresses how to convert the highly variable electrical output of a very-large (24 MW) floating wind turbine into grid-compliant power with high efficiency and power quality. We study an AC–DC–AC chain composed of a passive 6-pulse rectifier, a multilevel DC–DC boost stage, and a modular multilevel inverter (MMI), sized for a 60 kV DC link and 33 kV three-phase grid connection. The work develops physics-based models in PLECS/Simulink for the generator, rectifier, boost converter, and inverter, together with a control architecture that combines wind-side power following, DC-link regulation, and grid-side dq current control with PLL synchronization. A MATLAB toolbox is built to post-process simulation data and quantify power-quality indices (THD, TDD, VUF, PF) and DC-link ripple under realistic wind-speed profiles.

Simulation results show that the proposed converter can track power set-points while maintaining a stiff DC link and low ripple, and deliver grid-side current with near-unity power factor and low harmonic distortion across operating conditions. The study also contrasts the chosen passive rectifier + boost topology with an active rectifier alternative, highlighting device stress and trade-offs at this power and voltage level. Overall, the approach demonstrates a technically feasible and practically attractive conversion path for very-high-power floating wind turbines, and provides a reproducible modelling and analysis framework for future design iterations.

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Acronyms

AC – Alternating Current

DC – Direct Current

FET – Field Effect Transistor

FRT – Fault Ride-Through

HVDC – High Voltage Direct Current

IGBT – Insulated Gate Bipolar Transistor

LCOE – Levelized Cost of Energy

MMC – Modular Multilevel Converter

MMI – Modular Multilevel Inverter

MPPT – Maximum Power Point Tracking

MPC – Model Predictive Control

PCC – Point of Common Coupling

PF – Power Factor

PLECS – Piecewise Linear Electrical Circuit Simulation

PMSG – Permanent Magnet Synchronous Generator

PR – Proportional Resonant (controller)

PQ – Power Quality

PWM – Pulse Width Modulation

RMS – Root Mean Square

SiC – Silicon Carbide

SM – Submodule

THD – Total Harmonic Distortion

TDD – Total Demand Distortion

Vpp – Peak-to-Peak Voltage

VSI – Voltage Source Inverter

VUF – Voltage Unbalance Factor

1. Introduction

The Counter Rotating Floating Tilted turbine (CRAFT) is an innovative concept for floating offshore wind power that integrates the vertical-axis wind turbine (VAWT) topology with the aerodynamically dominant tilted horizontal-axis wind turbine (HAWT) design. Positioned between VAWT and HAWT configurations, CRAFT aims to leverage the benefits of both technologies while reducing platform, mast, and generator costs. Its unique architecture features a single spar buoy supporting two counter-rotating, tilted three-bladed turbines connected to a counter-rotating direct-drive generator. This setup enables a compact and cost-effective generator design with reduced torque requirements, enhancing system robustness and simplifying control via electrical converters. The generator, housed at or below sea level, uses ferrite permanent magnets to lower costs and contribute to system ballast, further improving stability. Overall, the CRAFT concept offers a promising pathway to reduce maintenance, transmission losses, and the levelized cost of energy (LCOE) for offshore wind systems.

Wind power is a rapidly growing contributor to renewable electricity production, with offshore wind offering particularly strong potential due to consistent and powerful wind resources at sea. Two turbine concepts dominate commercial deployment: the horizontal-axis wind turbine (HAWT) and the vertical-axis wind turbine (VAWT). HAWTs currently dominate because of their high aerodynamic efficiency, but their large nacelles, yaw systems, and pitch mechanisms make them costly and difficult to maintain offshore. VAWTs, in contrast, feature simpler structures and generators located near sea level, reducing tower and drivetrain costs, but they generally exhibit lower aerodynamic efficiency and suffer from unsteady aerodynamic loading [1]. Extensive research on large-scale VAWTs has highlighted their potential for offshore applications [1], yet the aerodynamic performance gap relative to HAWTs remains a challenge.

The CRAFT turbine has been proposed as a hybrid solution to bridge this gap. While aerodynamically closer to a tilted HAWT, its mechanical and electrical integration resembles VAWT principles. By combining two counter-rotating, tilted three-bladed rotors on a spar buoy with a counter-rotating direct-drive generator, the concept leverages HAWT-like efficiency together with the structural and maintenance advantages of VAWTs. A key innovation is the counter-rotating generator, patented by Bernhoff and Knutsen [2] and further developed in later studies [3], [4], [5], [6], [7]. Located at or below sea level, the generator reduces platform loads, uses ferrite permanent magnets to cut costs and improve stability, and benefits from torque sharing between two rotors, which allows a lighter and more compact machine. These design features aim to lower both capital and operational costs, making CRAFT a strong candidate for next-generation offshore wind systems.

Realizing such turbine concepts requires advanced electrical conversion systems to connect large permanent magnet synchronous generators (PMSGs) to the grid. PMSGs are widely used in modern wind turbines due to their high efficiency, robustness, and suitability for variable-speed operation without gearboxes. However, their raw electrical output must be processed before transmission: rectified, stepped up in voltage, and converted into high-quality alternating current at the grid voltage and frequency. For turbines in the 10–15 MW class and wind farms producing hundreds of megawatts, the power conversion system must continuously handle tens of kilovolts and tens of megawatts while ensuring efficiency, power quality, and controllability.

Conventional solutions based on active rectifiers and two- or three-level voltage source inverters have proven effective but face significant challenges at higher voltage and power levels, including high semiconductor stresses, reduced efficiency at partial load, and complex thermal management. To address these limitations, research has increasingly turned toward multilevel and modular converter topologies. In particular, combining a passive rectifier, a multilevel DC–DC boost converter, and a modular multilevel inverter (MMC) offers an attractive pathway. This architecture achieves very high DC-link voltages (e.g., 60 kV), distributes voltage stress across multiple devices, reduces harmonics, and improves fault tolerance.

The objective of this thesis is to design, model, and evaluate such a multistage conversion system for a large PMSG-based wind turbine, targeting 24 MW at 60 kV DC and 33 kV AC grid connection. The challenge lies in not only delivering the required power transfer but also ensuring stable DC-link operation, high power factor, low harmonic distortion, and robustness under varying wind conditions. The system was implemented in PLECS and MATLAB/Simulink, with each stage—the passive rectifier, the multilevel DC–DC boost converter, and the MMC inverter—modeled, tuned, and integrated. Control strategies for current and voltage regulation were developed and tested under variable wind profiles.

The results demonstrate that the proposed architecture can achieve the design target of 24 MW, maintaining stable 60 kV DC-link operation and nearly unity power factor at the inverter output, with acceptable harmonic distortion. These findings confirm that modular and multilevel converter topologies can scale to very high power and voltage levels without requiring prohibitively large components. The architecture offers clear advantages in efficiency, flexibility, and fault handling compared with conventional solutions, while also highlighting future challenges in control coordination and hardware implementation.

2. Background

Wind energy has become a cornerstone of the global transition to renewable electricity. With the increasing size of modern wind turbines—moving from single megawatt machines in the 1990s to more than 20 MW concepts today—the electrical conversion systems that connect turbines to the grid must handle unprecedented voltage and power levels [1], [6], [7]. This creates new challenges in efficiency, reliability, and scalability, particularly for offshore wind farms where accessibility for maintenance is limited [5].

Traditionally, wind turbines have relied on active rectifiers combined with voltage source inverters to connect permanent magnet synchronous generators (PMSGs) to the grid. This approach provides excellent controllability: the generator current can be shaped to maximize power extraction (MPPT) and to provide reactive power support to the grid [8], [9], [10]. Moreover, active rectifiers ensure that the generator sees nearly sinusoidal currents, which reduces torque ripple and mechanical stress [9].

However, as turbine power ratings approach 20–30 MW and generator voltages exceed 10–15 kV, this conventional approach faces critical limitations. Active rectifiers require large semiconductor devices that must withstand very high currents. At such high power levels, the switching and conduction losses become significant, while the number of parallel devices and their cooling systems drive up cost and reduce reliability [11]. Furthermore, the complexity of high-power active rectifier systems increases electromagnetic interference (EMI) issues, complicates harmonic filtering, and ultimately limits scalability for future ultra-large wind turbines [12], [13], [14].

To address these challenges, alternative topologies have been proposed that move away from fully controlled rectifiers at the generator interface. One promising concept is the combination of a passive diode rectifier, a multilevel DC–DC boost converter, and a modular multilevel converter (MMC) inverter. In this architecture, the diode rectifier provides a simple and highly robust interface with the generator. The multilevel boost converter then steps the rectified voltage up to very high DC levels (e.g., 60 kV), distributing the voltage stress across many semiconductor devices and allowing the use of commercially available components. Finally, the MMC inverter delivers high-quality 33 kV AC to the grid, with excellent harmonic performance, modularity, and scalability.

This study employs a dedicated electrical power conversion chain to interface the generator with the grid. The conversion train consists of three main stages:

1. A six-pulse diode rectifier,
2. A high-voltage DC–DC boost converter, and
3. A modular multilevel converter (MMC) inverter.

2.1 Rectifier Stage

The generator output is first converted into DC using a six-pulse diode rectifier. Each diode in the bridge conducts for 120º of the electrical cycle, carrying a fraction of the DC current.

2.2 Boost Converter Stage

The boost converter raises the DC bus voltage to the required inverter input level. Its duty cycle is expressed as:

$$V_{dc,out} = \frac{V_{dc,in}}{1 - D} \tag{1}$$

$$D = 1 - \frac{V_{dc,in}}{V_{dc,out}} \tag{2}$$

The output current is

$$I_{out} = \frac{P_{out}}{V_{out}} \tag{3}$$

The average inductor current is

$$I_{L,avg} = \frac{I_{out}}{1 - D} \tag{4}$$

The DC–DC boost stage is the central component of this work. Conventional boost converters cannot directly handle tens of kilovolts due to the voltage stress limitations of available semiconductors. Therefore, a multilevel non-inverting buck–boost topology was selected [15].

The advantages include:

- Distribution of voltage stress across stacked devices [12].
- Reduced inductor current ripple, lowering filter requirements [15].
- Scalability to very high DC voltages using stacked commutation cells [12].

2.3 MMC Inverter Stage

For AC grid integration, a Modular Multilevel Inverter (MMI) is used. The modular multilevel converter (MMC) synthesizes the AC output voltage waveform from the boosted DC bus.

Each phase leg consists of an upper arm and a lower arm, and each arm contains five submodules (SMs) connected in series. Every submodule includes a capacitor and semiconductor switches (either a half-bridge or full H-bridge), which can either insert the capacitor voltage into the arm or bypass it. By selectively inserting or bypassing submodules, the inverter synthesizes a staircase approximation of a sinusoidal AC voltage [11].

The instantaneous phase output voltage is defined as

$$v_{phase} = v_{upper} - v_{lower} \tag{5}$$

where v_{upper} and v_{lower} are the instantaneous voltages of the upper and lower arms. These arm voltages are determined by the number of submodules that are inserted at any instant.

- At the positive peak of the output sine, most submodules in the lower arm are inserted while the upper arm submodules are bypassed, yielding a high positive phase voltage.
- As the sine wave decreases toward zero, submodules are gradually exchanged between the upper and lower arms so that the phase voltage decreases in discrete steps.
- At the zero crossing, equal numbers of submodules are inserted in both arms, resulting in a phase voltage close to zero.
- During the negative half-cycle, more submodules are inserted in the upper arm while fewer are active in the lower arm, creating negative voltage steps.

This controlled switching sequence produces a staircase waveform that closely follows the sinusoidal reference.

In a modular multilevel inverter, the number of output voltage levels per phase is given by [11]:

$$N_{levels} = 2 \times N_{SM} + 1 \tag{6}$$

where N_{SM} is the number of submodules per arm.

2.4 Power Quality and Harmonic Distortion

The PQ analysis was performed using MATLAB scripts on simulated data.

2.4.1 RMS and Power Calculation

The instantaneous three-phase power is:

$$p(t) = v_a i_a + v_b i_b + v_c i_c \tag{7}$$

The average real power is:

$$P_{true} = \frac{1}{T}\int_0^t p(t)dt \tag{8}$$

2.4.2 THD and TDD

The Total Harmonic Distortion (THD) is computed as:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1} \tag{9}$$

where V_h are harmonic RMS voltages and V_1 is the fundamental.

For current, Total Demand Distortion (TDD) (IEEE-519) is:

$$TDD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_{rated}} \tag{10}$$

2.4.3 Voltage Unbalance Factor (VUF)

Positive and negative sequence voltages were extracted, and the Voltage Unbalance Factor was calculated:

$$VUF = \frac{|V_2|}{|V_1|} \times 100 \tag{11}$$

where V_1 and V_2 are positive and negative sequence phasors

2.5 Total Loss Calculation

The efficiency of the proposed power conversion system is determined by estimating the conduction and switching losses in the main components of the power train: the passive diode rectifier, the DC–DC boost converter, and the modular multilevel inverter (MMC). Loss mechanisms that are expected to be negligible compared with these dominant terms (such as capacitor dielectric loss or snubber dissipation) are omitted to maintain focus and clarity.

2.5.1 Diode Rectifier

For the three-phase diode rectifier, the primary loss mechanism is conduction. Each diode is modeled using the static voltage drop plus a resistive slope characteristic:

$$P_{cond,diode} = V_{T0} I_{avg} + r_T I_{rms}^2 \tag{12}$$

Where V_{T0} is the threshold voltage, r_T is the differential resistance, and I_{avg} and I_{rms} are the average and RMS currents conducted by each diode. Since each diode conducts for one-third of the fundamental cycle, the average and RMS currents are obtained directly from the simulated DC current. Other effects such as reverse recovery losses are neglected, as they are minimal at grid frequency compared with conduction losses.

2.5.2 DC–DC Boost Converter

For this stage, two dominant contributions are considered:

- **Conduction loss (IGBT):**

$$P_{cond,boost} = N_{cond} V_{CE(sat)} I_{avg} \tag{13}$$

where $V_{CE(sat)}$ is the saturation voltage of the IGBT at the considered current, I_{avg} is the inductor current, and N_{cond} is the number of IGBTs conducting in the current path.

- **Switching loss (IGBTs):**

$$P_{sw,boost} = N_{sw} f_s (E_{on} + E_{off}) \tag{14}$$

where E_{on}, E_{off} are the turn-on and turn-off energies per device, f_s is the switching frequency, and N_{sw} is the number of IGBTs switching per cycle.

- **Inductor losses:**
  Boost inductors experience copper (winding) loss and core loss. In this study only copper loss is considered, approximated as

$$P_{cu,L} = R_{dc} I_{rms}^2 \tag{15}$$

where R_{dc} is the winding resistance of the inductor I_{rms} is the current through it. Core losses are neglected for simplicity.

- **Capacitor losses:**

The DC-link capacitor bank has equivalent series resistance (ESR), which causes power loss under ripple current. Dielectric losses are neglected. The ESR loss is given by:

$$P_{ESR} = R_{ESR} I_{rms}^2 \tag{16}$$

where I_{rms} is the capacitor ripple current and R_{ESR} is the equivalent series resistance of the bank.

2.5.3 Inverter

In this study, the inverter is modeled in MATLAB/Simulink using controlled sources instead of detailed semiconductor switch models. This choice allows the simulation to capture the averaged electrical behavior of the modular multilevel converter (MMC) without going into the complexity of individual IGBT conduction states, switching events, or device parasitics. The benefit of this approach is that it keeps the model computationally efficient and makes it easier to study system-level aspects such as output waveforms, harmonic distortion, power quality, and the effectiveness of control strategies. The trade-off, however, is that the model cannot provide reliable estimates of switching losses or device-level performance, since those effects are not explicitly represented. In practice, this makes the model well suited for control and system studies, but not for detailed loss analysis or thermal design.

2.5.4 Overall Efficiency of diode and rectifier

The total loss is obtained by summing the contributions of all stages and passive elements:

$$P_{loss} = P_{cond,diode} + P_{cond,boost} + P_{sw,boost} + P_{ESR} + P_{cu,L} \tag{17}$$

The overall system efficiency is then expressed as:

$$\eta = \frac{P_{out}}{P_{out} + \sum P_{loss}} \tag{18}$$

Overall, this approach shifts the control focus away from the generator interface and towards the DC–DC converter and MMC. While the passive rectifier sacrifices direct control of generator currents, the system benefits from much greater efficiency, robustness, and scalability. Importantly, the modularity of both the boost converter and the MMC allows for fault-tolerant operation, which is highly valuable in offshore wind farms where unscheduled maintenance is prohibitively expensive.

3. Method

This chapter presents the methodology used to design, simulate, and analyze a high-power wind energy conversion system consisting of a passive rectifier, for a simplified proof of concept a 2- level DC–DC boost converter, and a 11 - level inverter. The Permanent Magnet Synchronous Generator (PMSG) parameters considered for this study are given in Table 1. The methods cover the simulation environment, converter design, control strategies, and power quality analysis.

Table 1 PMSG parameters.

Symbol	**Description**	**Value**
L_d	d-axis inductance (H)	1.3 mH
L_q	q-axis inductance (H)	1.3 mH
R_s	Resistance of the stator windings (Ω)	334.37 mΩ
ω_m	Angular mechanical velocity of the motor (rad/s) (primary generator)	1.2566 rad/s
λ_{pm}	Permanent magnet flux linkage (Wb)	5.42 Wb
P	Number of pole pairs	85
K_e	Back electromotive force (EMF) (Vpk_LL/krpm) – MATLAB/Simulink	2.5 MV/krpm
K_e	Back electromotive force (EMF) (Vpk/rpm) – PSCAD	30 kV/rpm
J	Combined inertia of motor and load (kgm²)	345e6 kgm²
B	Combined viscous friction of motor and load (N·m/(rad/s))	0.005 N·m/(rad/s)
T_e	Electromagnetic torque (Nm)	20 MNm
T_f	Mechanical shaft static friction torque (Nm)	0

3.1 Variable Shaft Speed Generation

To realistically model the effect of varying wind conditions on the wind turbine shaft, a time-varying shaft speed profile was generated in MATLAB. The nominal shaft speed was defined as 1.2566 rad/s, with upper and lower limits corresponding to ±20% variation around this value. Stochastic fluctuations were introduced using a normally distributed random noise signal, which was low-pass filtered to ensure smooth variations and avoid unrealistically fast oscillations.

To capture the effect of mechanical inertia, a slew-rate limiter was applied to restrict the maximum rate of change of shaft speed, preventing abrupt accelerations or decelerations that would be physically infeasible for a large rotating system. The generated shaft speed was further constrained within the predefined minimum and maximum limits, ensuring realistic operating behavior.

A long-duration profile of 8960 seconds was first generated to represent extended operating conditions. To facilitate simulation within practical timeframes, the complete dataset was then time-compressed to fit within a 15-second window without filtering or resampling, thereby preserving all statistical and dynamic features of the original profile.

The resulting signal provides a physically realistic variable shaft speed trajectory that reflects both wind stochasticity and turbine inertia. This profile was used as an input to the simulation model to represent variable wind speed conditions. Finally, the generated shaft speed profile was saved for later use in the model. The MATLAB code for the variable shaft speed generation is given in the Annex.

3.2 Simulation Environment

All system-level modeling was carried out in PLECS Standalone, integrated with MATLAB/Simulink. PLECS was selected because it enables device-level switching simulations at high power levels, while maintaining computational efficiency. Unlike averaged models, PLECS provides accurate capture of switching harmonics, circulating currents, and voltage balancing, which are critical when studying multilevel converters.

Alternative tools such as PSCAD/EMTDC or PSIM were considered, but PLECS was chosen due to its specialized component libraries for multilevel topologies, efficient handling of high-voltage switching, and direct integration with MATLAB for post-processing.

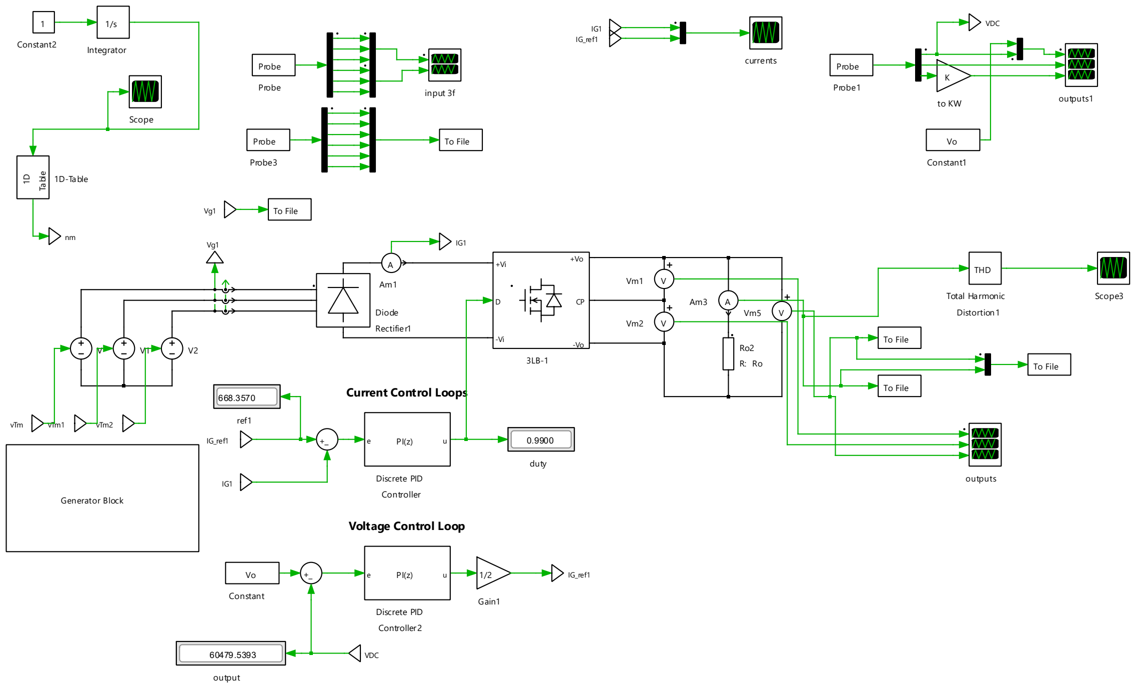

Figure 1 Rectifier and 2-level DC-DC boost converter schematic in PLECS

The generator block as seen in Figure 1 and Figure 2 generates an AC voltage with variable amplitude and frequency depending on the variable shaft speed, n_m

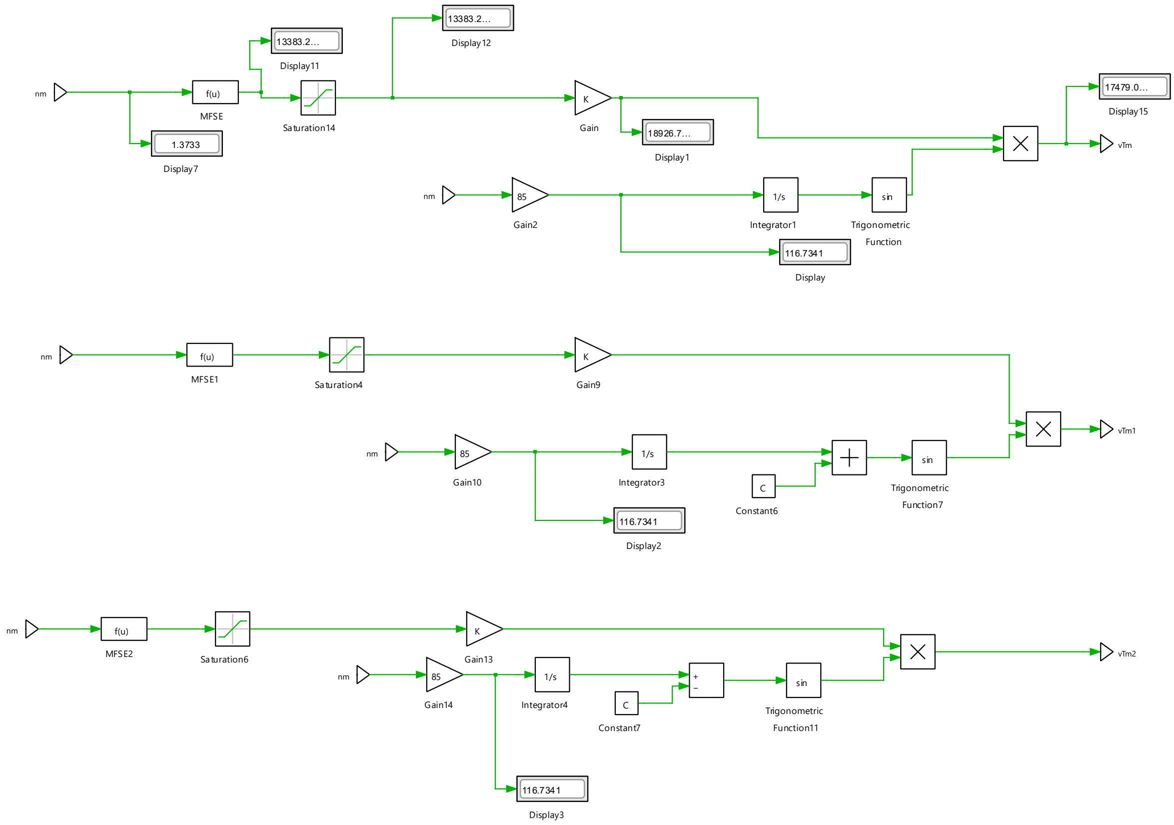

Figure 2 Inside the Generator Block

Inside the generator block as can be observed from Figure 2 the shaft speed n_m is multiplied by the rms phase voltage of 9745 V obtained from the back electromotive force (EMF) of 2.5 MV/krpm of the Permanent Magnet Synchronous Generator (PMSG). The result rms voltage is then multiplied with square root of 2 to get the peak voltage. The frequency and phase angle, which is required for the sinusoidal part of the voltage waveform is found from the product of the shaft speed and the number of pole pairs which gives the electrical angular velocity, ω_e which is then used to generate the sinusoidal component. The product of the amplitude and sinusoidal component will then generate the final voltage waveform.

3.3 Converter Topology and Design

3.3.1 Rectifier Stage

A three-phase passive diode full wave rectifier is employed at the generator output. While active rectifiers such as PWM-controlled topologies offer improved power factor control [9], they require a larger number of switching devices, complex modulation, and incur higher switching losses at MW power levels. At 24 MW and 60 kV DC, a passive diode rectifier offers simplicity, robustness, and proven industrial use.

3.3.2 Multilevel DC–DC Boost Converter

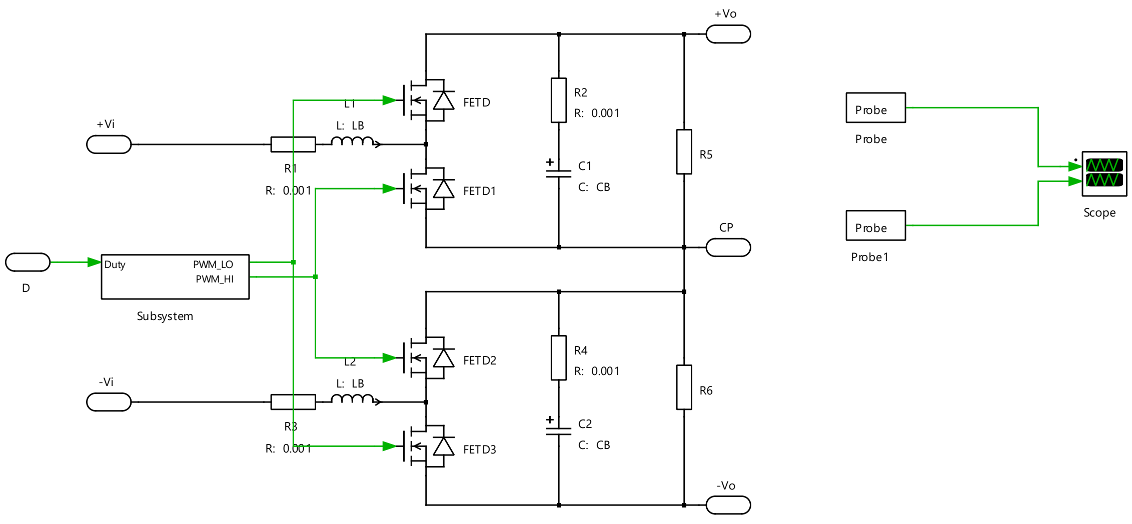

Figure 3: DC-DC boost converter topology

The voltage control loop generates the reference current IG_ref according to the converter output voltage Vdc and the reference voltage Vdc_ref. The reference current is used to control the input current, IG entering the converter. The difference between IG and IG_ref is taken as the duty cycle of the converter. From Figure 3 it is observed that the duty cycle is used to generate the PWM_Hi and PWM_Lo signals that operate the MOSFETs FETD and FETD3 responsible for charging and FETD1 and FETD2 responsible for discharging through the capacitors respectively. The inductors discharge through the capacitors in PWM_HI state and boost the voltage.

The switching frequencies of the converters were chosen to balance efficiency, loss distribution, and power quality requirements. For the DC–DC boost stage, a relatively high switching frequency of 16 kHz was selected to reduce inductor size and limit current ripple on the high-power DC link. High switching frequency improves dynamic performance and ripple attenuation, but at the cost of increased switching loss.

3.3.3 Multilevel Inverter

For AC grid integration, a modular multilevel inverter (MMI) was used as shown in Figure 4 and adapted to a 60 kV DC bus. The inverter used in this project is a modular multilevel inverter (MMI) configured for 11 output levels per phase. The inverter was operated at 2 kHz, which strikes a balance between maintaining acceptable ripples and power quality.

With five submodules per arm, each phase can therefore generate

$$N_{levels} = 2 \times 5 + 1 = 11$$

voltage levels.

With a DC bus of 60 kV, each submodule capacitor is balanced to approximately

$$V_{C,SM} = \frac{V_{dc}}{2 \times N_{SM}} = \frac{60}{10} \approx 6$$

so the staircase increments are about 6 kV each. The resulting phase voltage can step through values such as –30 kV, –24 kV, –18 kV, …, 0, …, +24 kV, +30 kV, providing a total of 11 levels.

The use of an 11-level inverter offers several advantages over conventional two-level or three-level designs [11]:

- **Low harmonic distortion:** The staircase waveform closely approximates a sine wave, reducing THD and filter requirements.
- **Lower dv/dt stress:** Each switch only handles around 6 kV instead of the full 60 kV, lowering stress on semiconductors and insulation.
- **Scalability:** More submodules can be added per arm to increase the number of levels without redesigning the main circuit.
- **Fault tolerance:** Faulty submodules can be bypassed, allowing the inverter to continue operating in degraded but functional mode.
- **Direct medium-voltage interfacing:** With 11 levels, the inverter can connect directly to a 33 kV grid without requiring a bulky transformer.

Therefore, the inverter operates by gradually inserting and bypassing capacitor submodules in its arms to create a staircase waveform with 11 discrete voltage levels. This topology provides high-quality AC output, reduces device stress, and enables direct medium-voltage grid connection at the scale of 24 MW and 60 kV DC link voltage.

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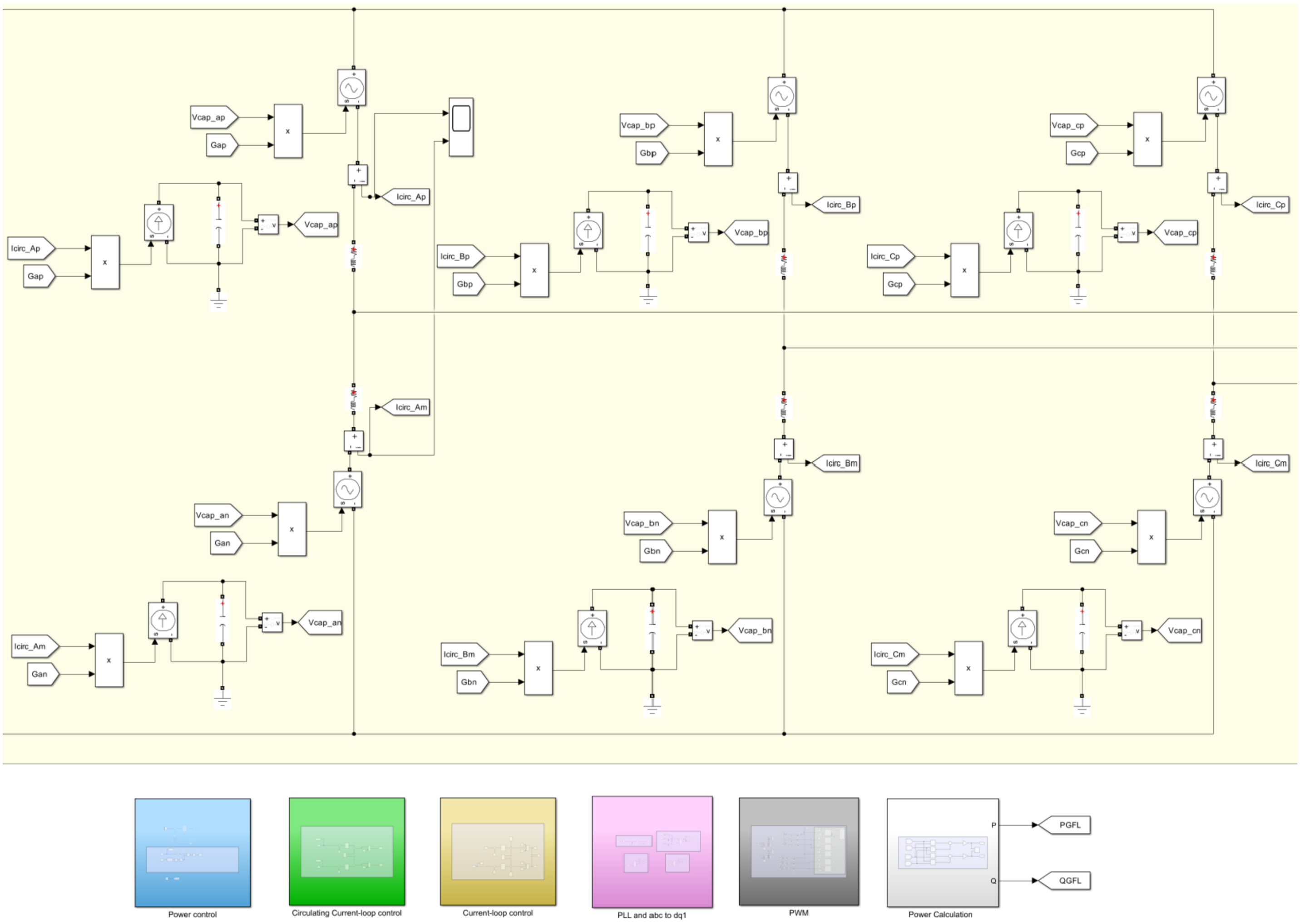

Figure 4: 11- level inverter topology

3.4 Control Strategy

3.4.1 Active Power Control Mode

The inverter is set to operate in active power control mode while the DC-DC boost converter will operate under voltage control mode. This is done so that both the inverter and boost converter do not contradict each other over control of the DC link voltage. The DC-DC boost converter will keep the DC link voltage constant while the inverter is tasked with target power output.

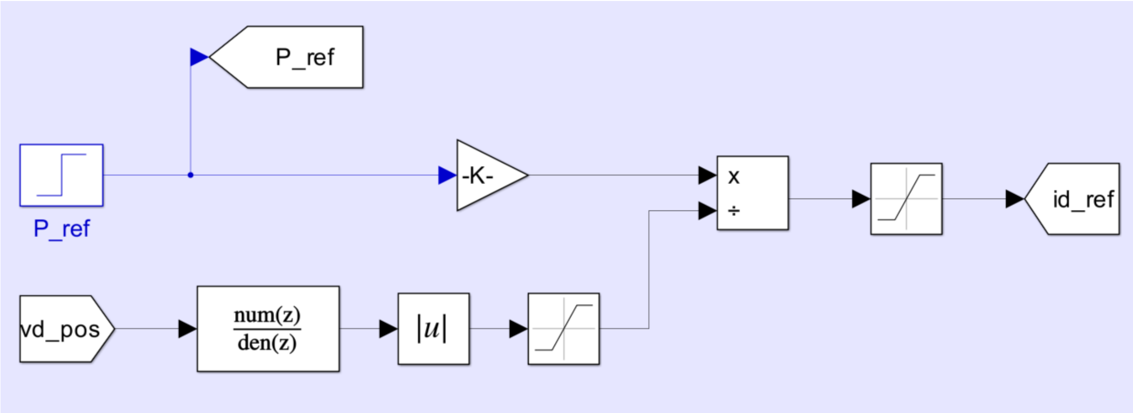

Figure 5: Inverter Power control system

To decouple from DC bus fluctuations, a power-follower mode was implemented. The reference i_d^{ref} was generated directly from the desired active power P_{ref} [14] as shown in Figure 5:

$$i_d^{ref} = \frac{P_{ref}}{1.5 \times V_d}$$

with V_d being the d-axis voltage. The q-axis current was set to zero for unity power factor:

$$i_q^{ref} = 0$$

This ensures that the inverter delivers constant active power to the grid regardless of small DC bus variations.

3.5 Power Quality and Harmonic Analysis

A central objective in the evaluation of wind turbine power conversion systems is to ensure that the quality of the generated electrical power meets grid requirements. Power quality is typically assessed in terms of waveform distortion, harmonic content, power factor, and overall efficiency of conversion. In this study, emphasis is placed on harmonic analysis of the DC–DC boost converter and the inverter stage, as these subsystems have the most significant impact on waveform quality. The analysis is conducted using the mathematical framework provided by equations (*7*) – (*11*), which define the total harmonic distortion (THD), root-mean-square (RMS) quantities, and power quality indices used throughout the study.

For the DC–DC boost stage, the analysis is carried out directly on the DC-link voltage and current waveforms. Although these quantities are expected to contain primarily low-frequency ripple, the switching process introduces higher-frequency components which contribute to harmonic distortion. Equations (*7*) – (*11*) are applied to the simulated boost converter waveforms to quantify these harmonics, providing a measure of the residual distortion seen at the DC-link interface. This analysis is important because any distortion present at the DC-link will propagate through the system and potentially affect the performance of the inverter and grid-side interface.

The inverter stage is a more critical source of harmonics, as it directly synthesizes the three-phase AC voltage for grid connection. To evaluate inverter performance, the line-to-line voltages and phase currents are analyzed in detail using the same harmonic analysis framework. In this work, the harmonic content is computed before the RL filter, which is placed at the inverter output. This design choice is intentional: the RL filter is specifically designed to smooth the inverter output waveforms, attenuating switching harmonics and yielding nearly sinusoidal voltages and currents. As a result, the harmonic content measured after the filter is extremely small, and the corresponding voltage THD can be considered effectively zero. By contrast, evaluating the inverter output before the filter provides insight into the inherent switching characteristics of the converter and allows for a more meaningful comparison of modulation strategies and device-level effects.

The power quality indices considered include the RMS value of the fundamental voltage and current components, Voltage Utilization Factor (VUF), the RMS values of the harmonic components, and the total harmonic distortion. THD is computed as the ratio of the RMS value of the harmonics to the RMS value of the fundamental component, as expressed in equation (*9*). This provides a normalized measure of distortion that is independent of absolute amplitude. In addition, the active and reactive power delivered by the inverter are computed to determine the power factor, using equations (*10*) and (*11*). Together, these metrics provide a comprehensive assessment of the inverter's ability to deliver high-quality power to the grid.

The complete implementation of the harmonic analysis procedure has been carried out in MATLAB. A dedicated function was written to process the simulated voltage and current waveforms, extract the fundamental and harmonic components, and compute the associated power quality indices. This function is provided in the Annex for reference. By automating the harmonic analysis, consistent and repeatable evaluation of multiple simulation scenarios is ensured, including cases with varying wind speeds and generator operating conditions.

Overall, the power quality and harmonic analysis in this thesis is based on equations (*7*)–(*11*), applied to both the DC–DC boost converter and the inverter stage. For the inverter, the analysis is performed before the RL filter to capture the true distortion introduced by switching, while recognizing that the filter reduces the delivered voltage THD to negligible levels. This methodology ensures a comprehensive understanding of the harmonic performance of the proposed power conversion system under realistic operating conditions.

3.6 Total Loss and Overall Efficiency Calculation

The total losses in the conversion system are determined by summing the contributions from conduction losses, switching losses, inductor copper losses, and capacitor ESR losses. These are calculated using equations (*12*)–(*18*), which define the dominant loss mechanisms for the rectifier, DC–DC boost converter, inverter, and passive components. Negligible loss components, such as dielectric loss in capacitors or snubber dissipation, are omitted in this study.

A value of R_{ESR}=2 mΩ is used in this study. This is representative of large film capacitor stacks in the MW range, where ESR values typically lie between 0.5 and 2 mΩ depending on construction and the number of parallel elements [16], [17].

For large-scale power inductors operating at medium frequencies (10–20 kHz), the winding DC resistance R_{dc} typically lies between 1–3 mΩ, depending on the number of turns, conductor cross-section, and mean length per turn [18]. This study assumes R_{dc}=1 mΩ as a representative value for the boost inductors. Core losses are neglected.

In the simulation model, the DC–DC boost converter is represented as a two-level structure with one switch per arm. However, at the considered voltage and current levels, this is not feasible because no single semiconductor device exists that can block tens of kilovolts and simultaneously conduct several hundred amperes. In practice, more levels and hence more switches are required in stacked configurations to meet voltage and current requirements.

As an illustrative example, losses are calculated for an 11-level boost converter using SiC IGBTs operating at a switching frequency of 16 kHz. With an output DC voltage of 60 kV, the per-submodule voltage is approximately

$$V_{SM} = \frac{V_{out}}{N_b} = \frac{60\ kV}{11} \approx 5.5\ kV$$

which is within the blocking capability of commercially available 6.5 kV SiC IGBTs. From equation 3, the inductor current of approximately 800 A is shared across paralleled devices in each submodule.

The inverter was modeled in MATLAB/Simulink using controlled sources rather than detailed semiconductor switch models. As such, the model represents the averaged electrical behavior of the MMC but does not resolve individual IGBT conduction states, switching transitions, or device parasitics. This approach is sufficient for assessing output waveforms, power quality, and control performance, but it prevents accurate estimation of inverter losses.

The passive rectifier and dc-dc boost converter calculation of the loss breakdown, total losses, and efficiency has been automated using MATLAB code, which is provided in the Annex.

4. Results

4.1 Results Obtained

The simulations of the complete wind power conversion chain — comprising a passive diode rectifier, a stacked multilevel DC–DC boost converter, and a cascaded multilevel inverter — have successfully demonstrated the capability of the system to deliver the rated 24 MW output power at 33 kV AC line-to-line RMS.

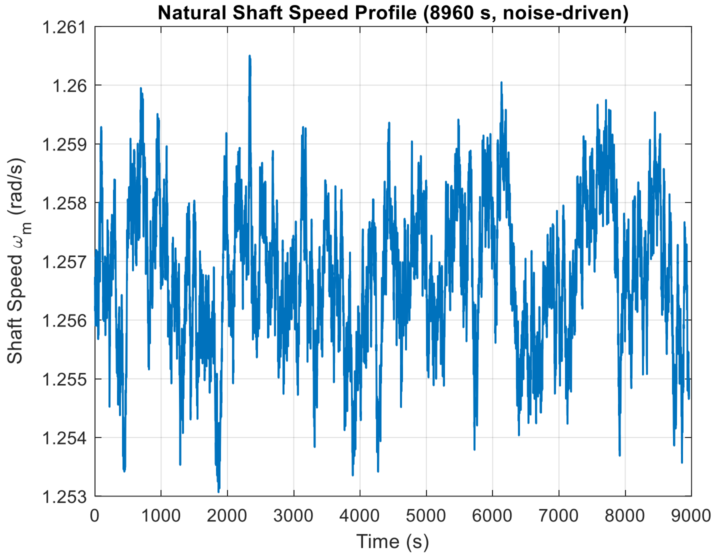

Figure 6: Variable Shaft Speed Profile

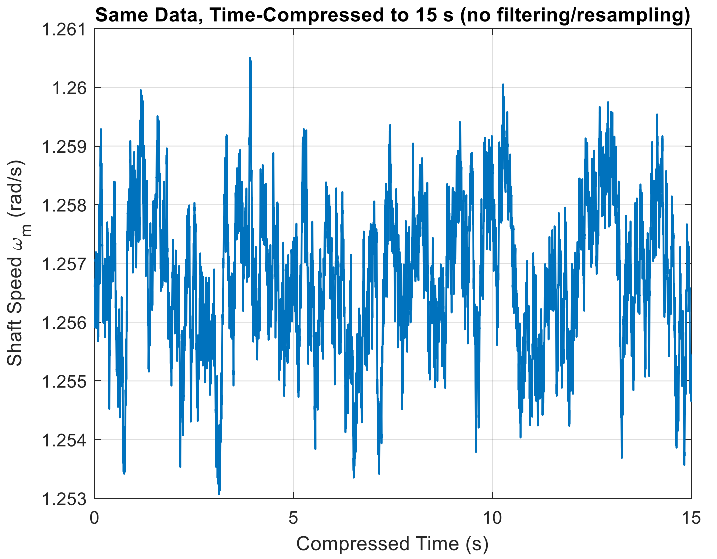

Figure 7: Variable Shaft Speed Profile (compressed)

The variable shaft speed, nm as seen in Figure 6 and Figure 7, generated using the RAND function in MATLAB is used to generate the variable voltage profile from the generator block (Figure 1). The variable voltage profile is shown in Figure 8.

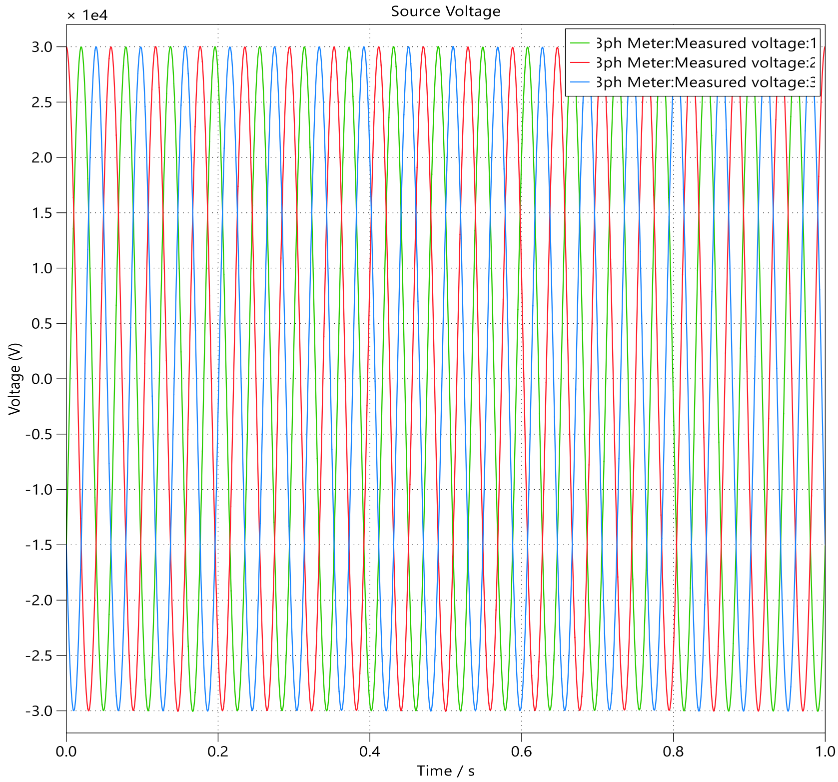

Figure 8 Output voltage from the generator block

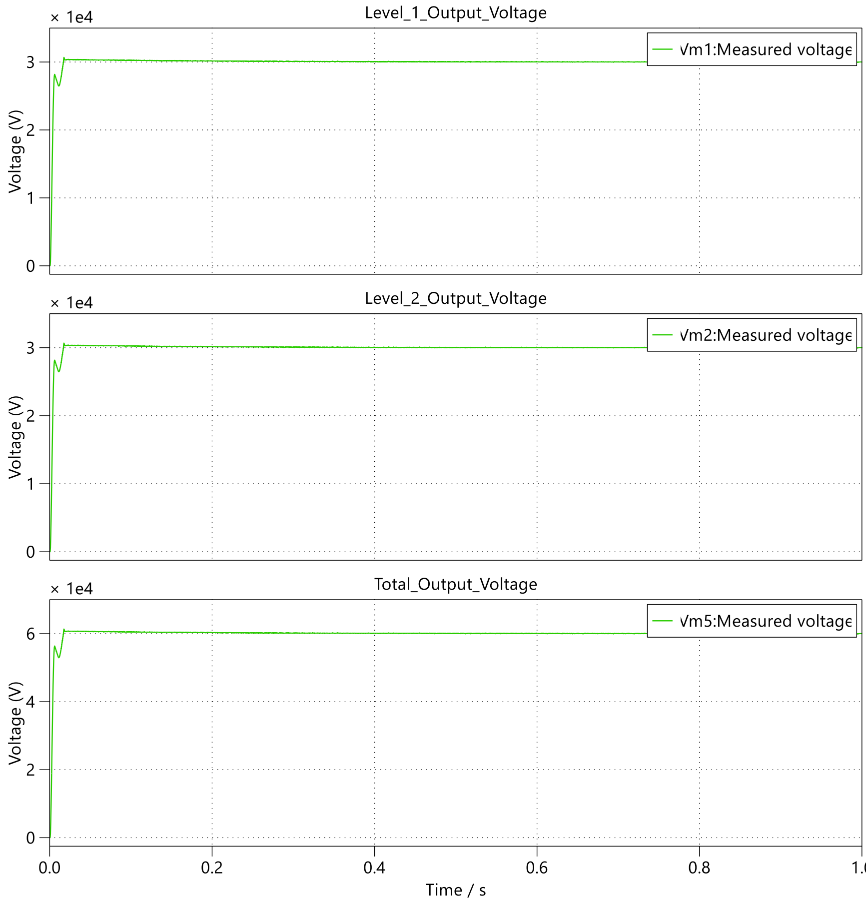

Figure 9: DC-DC boost converter output voltage. The top 2 graphs are individual level voltage and the bottom graph is total voltage.

On the DC side, the boost converter maintained a regulated output voltage of 60 kV despite significant variations in generator shaft speed as can be seen from Figure 9.

Table 2: DC-DC boost converter output voltage power quality and THD analysis

Metric	Value	Unit	Relative Value
Mean DC Voltage (V_dc,mean)	60,030	V	–
Voltage Ripple RMS (V_ripple,rms)	26.5	V	0.044 %
Voltage Ripple Peak-to-Peak (Vpp)	160	V	–
Voltage Ripple THD (2 Hz harmonics)	53.76	%	–
Switching Band RMS @ 16 kHz	4.32	V	–
Switching Band RMS @ 32 kHz	0.27	V	–
Switching Band RMS @ 48 kHz	0.41	V	–
Mean DC Current (I_dc,mean)	400.2	A	–
Current Ripple RMS (I_ripple,rms)	0.177	A	<0.05 %
Average DC Power (P_avg)	24	MW	–
Power Ripple RMS (P_ripple,rms)	21	kW	0.088 %

The DC-link performance results in Table 2 demonstrate that the boost converter successfully regulates the DC voltage at the desired 60 kV, with excellent stability.

4.1.1 DC-Link Power Quality Analysis

The performance of the DC–DC boost converter output was evaluated in terms of DC-link voltage and current quality, ripple content, and harmonic spectrum. The results are summarized below.

DC-Link Voltage

The average DC-link voltage is measured at 60.03 kV, which is very close to the design target of 60 kV. The RMS ripple voltage is 26.5 V, corresponding to 0.044% of the mean DC voltage, while the peak-to-peak ripple is 160 V. These values indicate excellent voltage stability, with only small deviations relative to the nominal value.

The harmonic analysis of the low-frequency ripple (at 2 Hz, corresponding to the generator frequency) shows a ripple THD of 54%, which reflects the dominance of the fundamental 2 Hz component and its harmonics in the ripple waveform. Despite the high THD figure, the absolute ripple magnitude remains small compared with the DC voltage (well below 0.1%).

At higher frequencies, the switching-related harmonics are effectively controlled. The RMS values in the switching frequency bands are 4.3 V at 16 kHz, 0.3 V at 32 kHz, and 0.4 V at 48 kHz. These are several orders of magnitude smaller than the mean DC voltage, confirming that the switching harmonics do not significantly impact the DC-link quality.

DC-Link Current

The average DC current is 400.2 A, consistent with the expected value for 24 MW output at 60 kV. The RMS current ripple is only 0.18 A, which represents less than 0.05% of the mean current, indicating very stable current delivery from the boost converter.

DC Power Stability

The average DC power is 24MW, matching the design rating. The RMS power ripple is 21 kW, corresponding to 0.09% of the average power. This demonstrates that the DC-link power is extremely stable, with negligible oscillations relative to the overall power transfer.

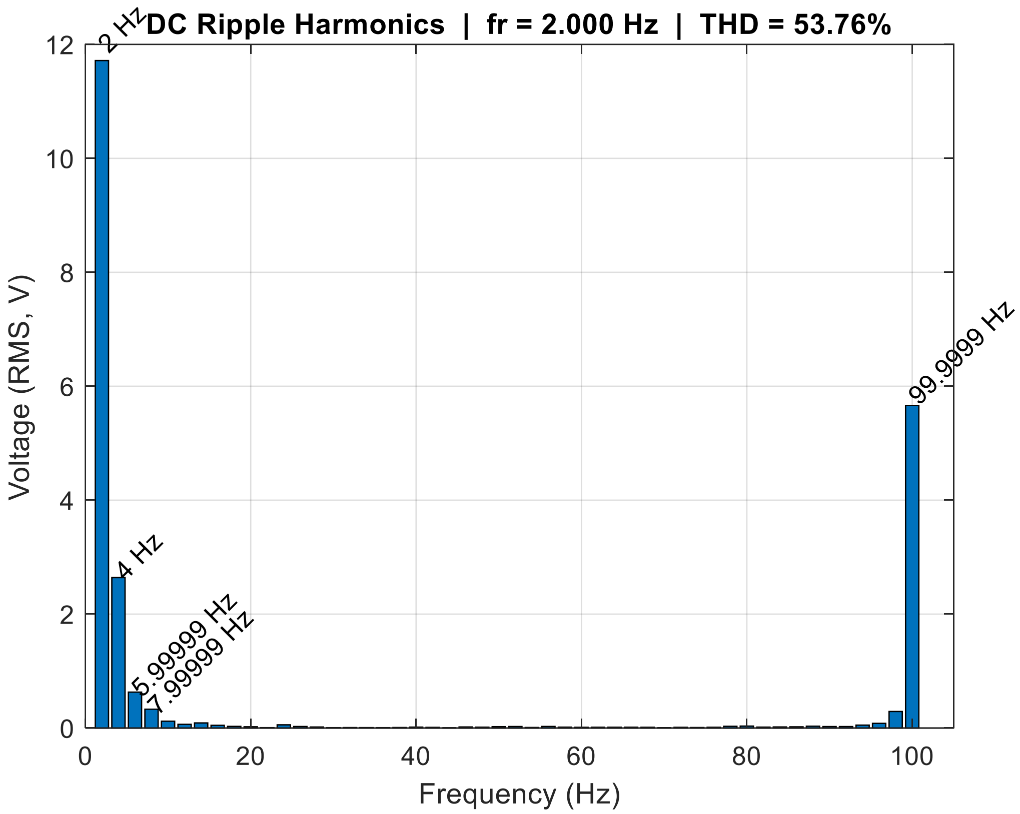

Figure 10: DC-DC boost converter output voltage THD spectrum

Harmonic Analysis of DC-DC boost converter output

The harmonic spectrum of the DC-link voltage at the output of the boost converter is shown in Figure 10. The harmonic spectrum of the DC-link voltage at the boost output (Figure 10) is dominated by a 2 Hz component (≈ 11–12 V RMS), which arises from low-frequency power oscillations on the generator side. Its multiples (4, 6, 8 Hz, …) are also present with rapidly decreasing magnitude. In addition, a distinct line appears at 100 Hz (≈ 5–6 V RMS) with very small sidebands near 99–100 Hz which originates from low-frequency interactions between the generator-side fluctuations and the switching action of the boost stage.

Although the ripple THD computed with respect to the 2 Hz fundamental is relatively high (≈ 54 %), the absolute ripple levels are tiny compared with the nominal 60 kV DC voltage: the largest components (2 Hz and ~100 Hz) are on the order of 10 V and 5 V RMS, i.e., ≪ 0.1 % of Vdc. Higher-frequency switching bands (reported separately at 16, 32, and 48 kHz) remain several orders of magnitude lower than the mean DC voltage and are not visible on this low-frequency plot.

Overall, the spectrum confirms a stable and high-quality DC link: ripple energy is concentrated at very low frequencies (2 Hz series) plus a small 100 Hz rectifier component, with amplitudes that are negligible for system operation and fully compatible with the downstream inverter requirements. Compared to similar works on multilevel boost converters [12], [15], the results here show equally low ripple percentages and comparable harmonic performance, validating the chosen architecture as both feasible and efficient for high-power (24 MW) renewable integration.

4.1.2 AC Power Quality Analysis

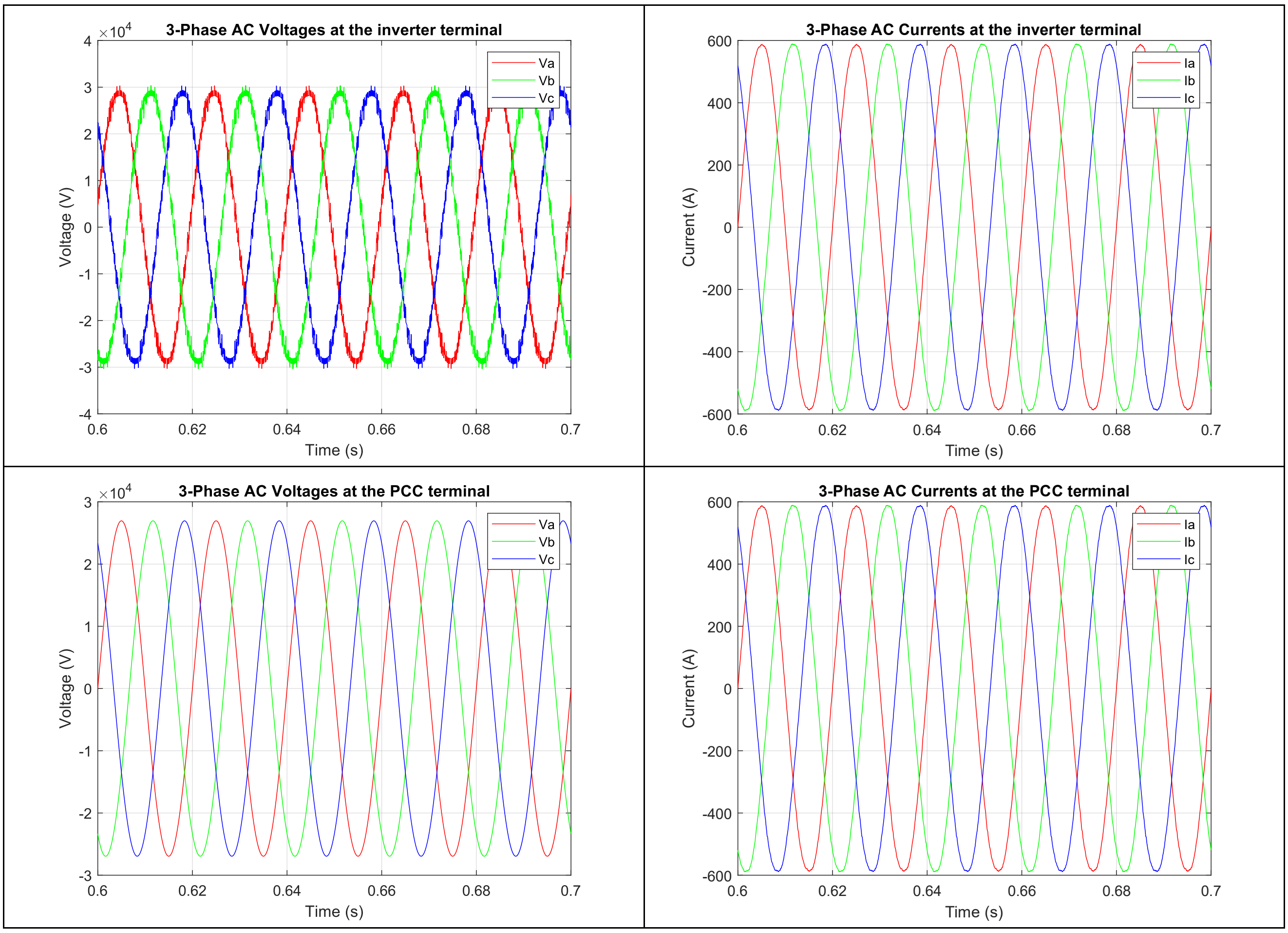

Figure 11: Inverter output voltage and current waveforms at the inverter terminal and PCC

On the AC side, the multilevel inverter produced nearly sinusoidal output voltage at the PCC but at the inverter some voltage distortion is observed as can be seen in Figure 11. At the inverter terminal the THD is 2.27 %, and the fundamental power factor remained at 0.982.

Table 3: Inverter output voltage power quality and THD analysis at the inverter terminal

Metric	Phase A	Phase B	Phase C	Average / Total	Unit
Voltage THD (classic)	2.2824	2.2582	2.2736	2.2714	%
Current THD (classic)	0.9814	0.9929	0.9796	0.9846	%
Active Power (P_true)	–	–	–	25.419	MW
Fundamental Active Power (P1)	–	–	–	25.419	MW
Reactive Power (Q1)	–	–	–	4.651	Mvar
Max Active Power (P_max)	–	–	–	27.641	MW
Min Active Power (P_min)	–	–	–	22.875	MW
RMS Active Power (P_rms)	–	–	–	25.432	MW
Power Factor (true)	–	–	–	0.982	–
Power Factor (displacement)	–	–	–	0.984	–
Voltage Unbalance Factor (VUF)	–	–	–	0.0098	%

Harmonic Analysis of Inverter Output Before RL Filter

The inverter output before the RL filter shows good power quality, with a voltage THD of approximately 2.27% and a current THD below 1%. The system delivers 25.4 MW of active power with 4.65 Mvar of reactive power, corresponding to a true power factor of 0.982. Voltage unbalance is negligible (VUF ≈ 0.01%), confirming that the inverter maintains balanced three-phase operation. After filtering, the voltage THD is expected to reduce further and can be considered close to zero.

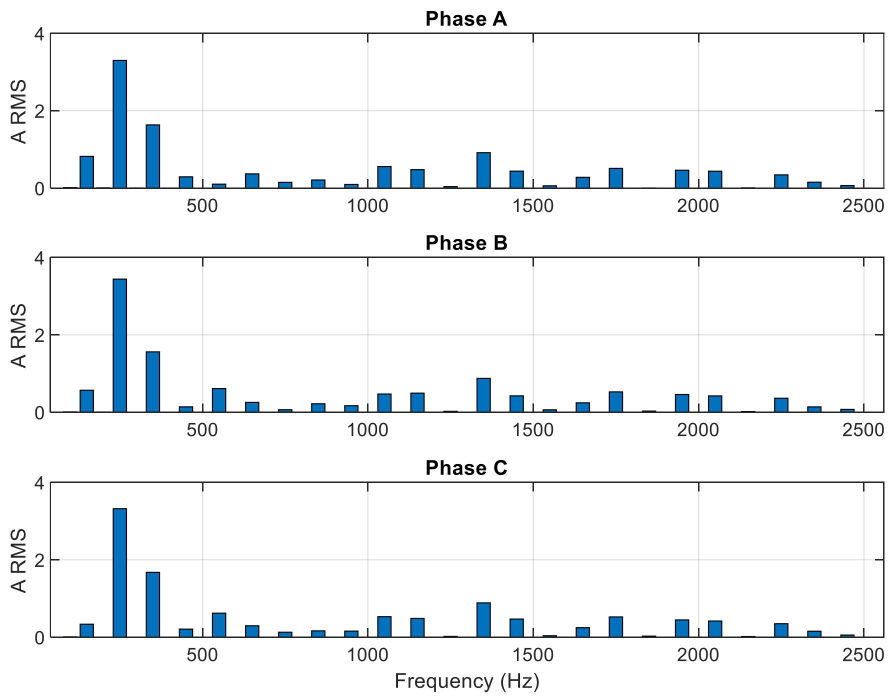

Figure 12 Harmonic current at the inverter output

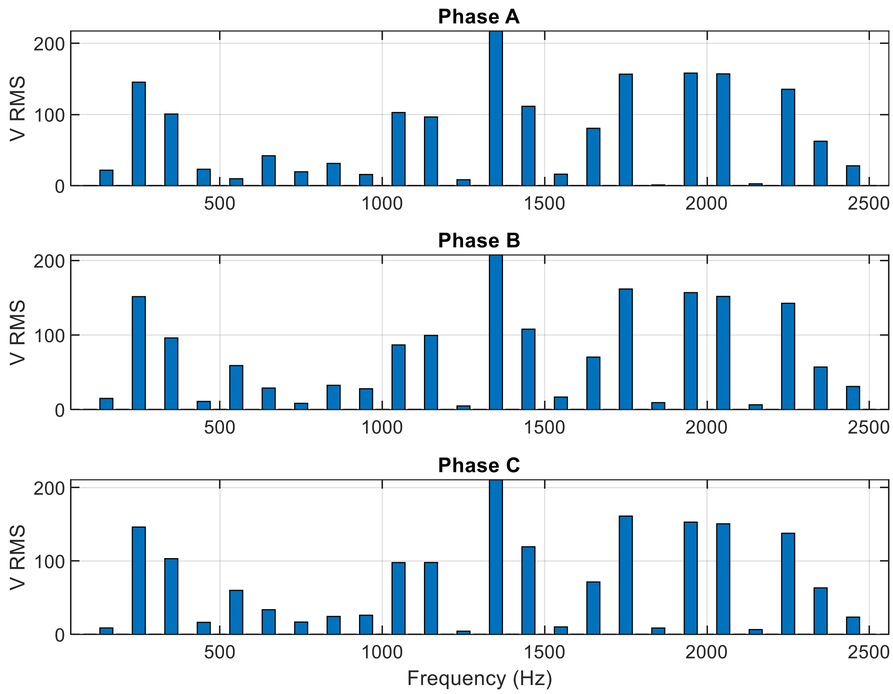

Figure 13: Harmonic Voltage at the inverter terminal

Current Harmonics

The current spectra (Figure 12) indicate that the dominant harmonics are located at the lower-order frequencies, particularly the 3rd, 5th, and 7th harmonics. The fundamental at 50 Hz is clearly dominant, with the next strongest components appearing around 250–350 Hz. The RMS magnitude of the harmonic currents beyond the 7th order is significantly smaller, with higher-order components (above 1 kHz) contributing only a minor fraction of the total distortion. This distribution confirms the low current THD (≈0.98%) reported in the power quality summary, and highlights that the inverter current waveform is already of high quality even before filtering.

Voltage Harmonics

The voltage spectra (Figure 13) reveal a higher concentration of harmonic components compared with the current spectrum. Significant peaks are observed at low-order harmonics (e.g., 3rd and 5th), but strong contributions are also present at switching-related frequencies in the range of 1–2 kHz. The magnitude of these components can reach values above 100 V RMS per harmonic, with some peaks around 200 V RMS. This is consistent with the measured voltage THD of ~2.27% in the unfiltered inverter output.

Table 4: Inverter output voltage power quality and THD analysis at the PCC

Metric	Phase A	Phase B	Phase C	Average / Total	Unit
Voltage THD (classic)	0.0000	0.0000	0.0000	0.0000	%
Current THD (classic)	0.9814	0.9929	0.9796	0.9846	%
Active Power (P_true)	–	–	–	23.997	MW

Fundamental Active Power (P1)	–	–	–	23.997	MW
Reactive Power (Q1)	–	–	–	-0.000	Mvar
Max Active Power (P_max)	–	–	–	24.411	MW
Min Active Power (P_min)	–	–	–	23.484	MW
RMS Active Power (P_rms)	–	–	–	23.998	MW
Power Factor (true)	–	–	–	1.000	–
Power Factor (displacement)	–	–	–	1.000	–
Voltage Unbalance Factor (VUF)	–	–	–	0.0002	%

With the RL filter in place, the inverter output voltage is perfectly sinusoidal, with the measured voltage THD reduced to 0%. The current THD remains unchanged at approximately 0.98%, since it is mainly determined by the harmonic content of the current waveform rather than the voltage. The active power delivered is 23.997 MW with negligible reactive power, yielding a true power factor of 1.0. The voltage unbalance factor is nearly zero (0.0002%), confirming excellent three-phase balance. These results demonstrate that the RL filter effectively removes voltage harmonics, ensuring grid-compliant power quality at the inverter output.

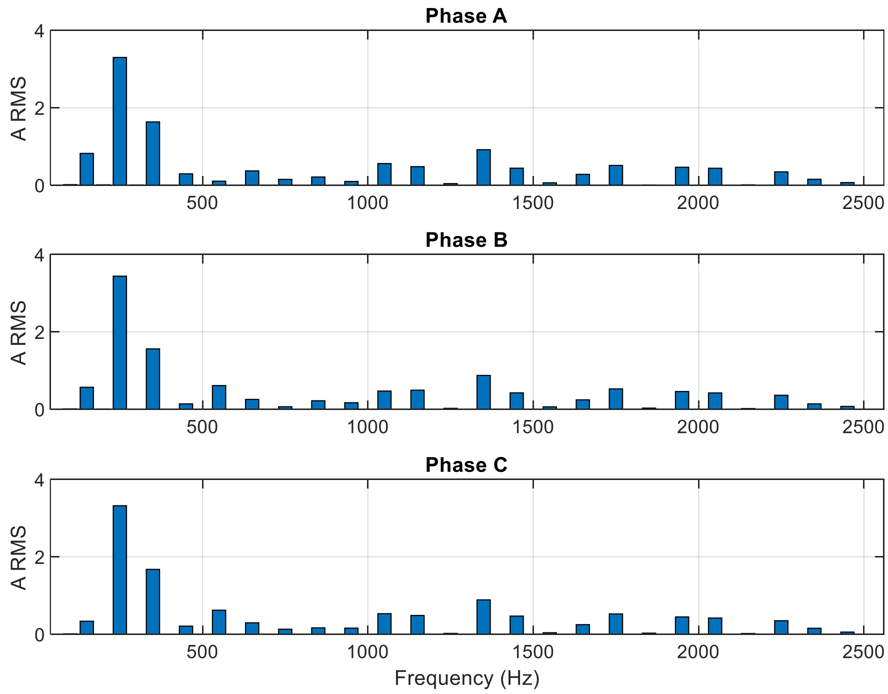

Figure 14 Harmonic current at the PCC

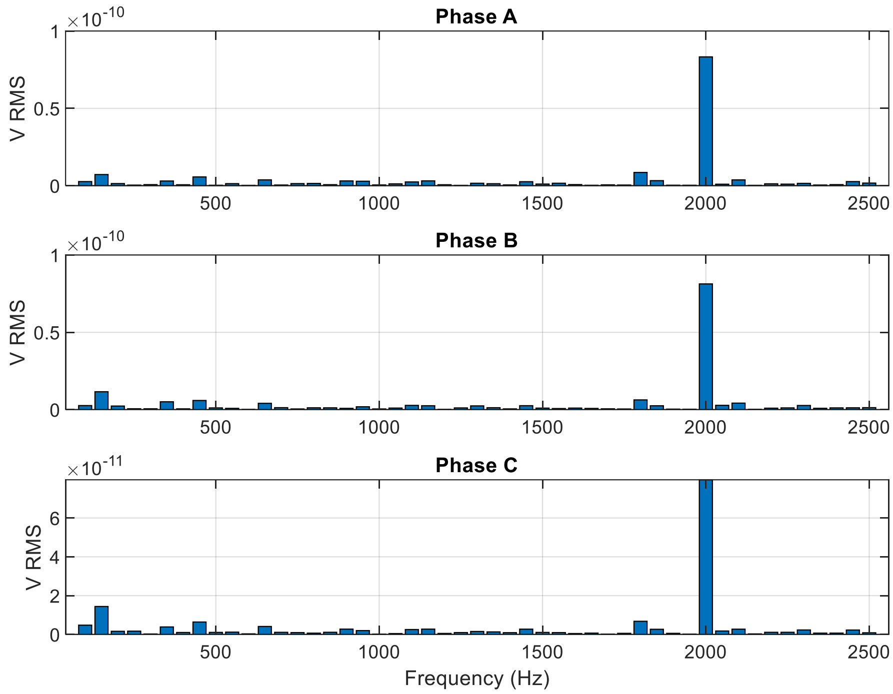

Figure 15: Harmonic Voltage at the PCC

Harmonic Analysis of Inverter Output After RL Filter (PCC)

The harmonic spectra of the three-phase currents and voltages at the point of common coupling (PCC) after the RL filter are shown in Figure 14 and Figure 15.

Current Harmonics

The current spectra indicate that low-order harmonics such as the 3rd, 5th, and 7th remain visible, with RMS magnitudes around 1–3 A. However, the amplitudes of higher-order harmonics above 1 kHz are significantly reduced compared with the unfiltered case. The fundamental component at 50 Hz is dominant, and the residual harmonic content is consistent with the measured current THD of approximately 0.98%. This shows that the RL filter does not substantially affect the harmonic profile of the current, which remains of high quality and within grid compliance.

Voltage Harmonics

The voltage spectra at the PCC demonstrate the effectiveness of the RL filter. All low-order harmonic components have been suppressed to negligible levels, and the higher-frequency switching harmonics in the 1–2 kHz range, which were prominent before filtering, are no longer visible. The remaining voltage components are several orders of magnitude smaller (on the order of 10^{-10} – 10^{-11} V RMS), effectively eliminating voltage distortion. This agrees with the total harmonic distortion (THD) results, where the post-filter voltage THD is measured as 0%.

The inverter output results confirm that the system delivers the rated 24 MW to the AC grid with excellent power quality. The measured average real power is 23.997 MW, essentially identical to the reference, while the instantaneous power oscillates within a narrow band (23.5–24.4 MW). The RMS power of 23.998 MW demonstrates steady-state stability.

The voltage quality is outstanding: the voltage THD is effectively 0 % across all three phases, which reflects the capability of the 11-level inverter to produce a waveform that is nearly sinusoidal without the need for large filters. The voltage unbalance factor (VUF) is also 0 %, confirming that the three phases are perfectly balanced in both amplitude and phase, as expected from a symmetrical MMC configuration.

The current quality is equally strong. The current THD values across phases are ~0.98 %, well below the IEEE-519 recommended limit of 5 % for harmonic distortion at this voltage level. This shows that the inverter current control strategy is effective in suppressing harmonics, and that the staircase waveform of the 11-level MMC significantly reduces switching-related distortions compared with two-level or three-level alternatives.

Regarding power factor, the inverter operated at unity PF (1.000), indicating that all delivered power is active power, with negligible reactive exchange ($Q_1 \approx 0$ MVar). This is important for compliance with modern grid codes and maximizes the utilization of the converter and transmission system.

4.1.3 Power loss and efficiency

Table 5: Power loss distribution and efficiency of Rectifier & DC-DC boost converter

Component	Value	Unit
Rectifier conduction loss	1780	W
Boost conduction loss	35200	W
Boost switching loss	31680	W
Inductor copper loss	1280	W
Capacitor ESR loss	Negligible (≈0.5)	W
Total loss	69940	W
Efficiency	99.70	%

The rectifier conduction loss amounts to approximately 1.78 kW, which is relatively small compared with the total system power rating (24 MW). This is expected, as the passive diode rectifier has only conduction losses associated with the forward voltage drop and series resistance of the diodes, and operates at grid frequency where switching losses are negligible.

The conduction loss of the IGBTs in the boost stage is approximately 35.2 kW, while the switching losses contribute another 31.7 kW. Together, the boost converter accounts for over 67 kW of losses, reflecting the high current levels (≈800 A) and high switching frequency (16 kHz) it must handle. In addition, the copper losses in the inductors amount to around 1.28 kW, while the ESR loss in the DC-link capacitors is negligible (≈0.5 W). The rectifier & DC–DC boost losses reported in Table 5 (≈ 69.9 kW, 99.70% efficiency) omit several second-order contributions, including inductor core loss, AC winding effects, temperature-dependent increases in $V_{CE(sat)}$ and $E_{on/off}$, snubber/capacitive energy, equalization resistor dissipation, and auxiliary power.

Since the inverter was represented in MATLAB/Simulink as an averaged model without explicit semiconductor switch blocks, its conduction, switching, reverse recovery, and auxiliary losses could not be captured. As a result, inverter efficiency could not be quantified, and the overall system loss and efficiency are not reported in this study.

Key Observations

- The boost converter dominates the loss profile, primarily due to the high switching frequency and large inductor current.
- Inverter losses could not be accurately quantified because of the averaged modeling approach; future studies should include device-level modeling to obtain realistic efficiency values.
- Passive component losses (inductor copper loss and capacitor ESR loss) are negligible relative to semiconductor losses.
- The rectifier + boost converter subsystem achieves an efficiency of ≈99.7%, demonstrating that this stage of the converter architecture can operate with very low losses even at high power and voltage levels.

5. Discussion

5.1 Critical review of results

While the target output power of 24 MW was achieved, the process revealed several key insights:

5.1.1 Device Stress

At 60 kV DC, device-level stresses are high. Simulation showed that if the DC bus is instead reduced to 30 kV, the current levels nearly double, requiring larger semiconductor ratings. This trade-off confirms the necessity of a high-voltage, low-current design to reduce conduction losses, semiconductor count, and filter size.

5.1.2 Comparison with Literature

The inverter output before filtering had a voltage THD of 2.27% and a current THD of 0.98%, which the RL filter reduced to 0% and 0.98%, respectively. The true power factor reached unity after filtering. By contrast, active rectifier–inverter systems in the same power range often exhibit higher unfiltered THD. For example, according to [1] active rectifier–inverter systems in large-scale VAWT applications typically achieve unfiltered current THD values between 2–4%, requiring larger filters to meet grid codes. Similarly, from [10] it is noted that PWM-based active rectifiers introduce significant high-frequency harmonics, with unfiltered voltage THD in the 3–5% range at MW scale.

On the DC side, the boost converter delivered an average voltage of 60.03 kV with only 0.044% RMS ripple. By comparison, active rectifier–inverter systems tend to exhibit larger DC-link voltage fluctuations because the active rectifier operates under variable wind and grid conditions without an intermediate boost stage. For instance, [13] show that MMC-based wind farm rectifiers exhibit DC ripple levels up to 0.5–1%, depending on operating point.

5.1.3 Loss Breakdown and Efficiency

The total loss of the rectifier + DC–DC boost converter subsystem was calculated to be approximately 69.9 kW, corresponding to an efficiency of 99.70% at the rated power of 24 MW. The dominant contribution comes from the DC–DC boost converter (~67 kW), due to the combination of high inductor current (~800 A) and high switching frequency (16 kHz). Losses in the passive diode rectifier are comparatively small (~1.8 kW), while passive component losses in inductors and capacitors are negligible relative to semiconductor losses.

When compared to values reported in literature, the results are favorable. Active rectifier–inverter systems typically show lower efficiencies, with two-level active rectifiers at MW scale achieving only 97–98% efficiency, largely limited by higher switching losses and more complex cooling requirements [8]. This highlights the efficiency advantage of a passive rectifier + multilevel boost approach, which shifts the loss burden away from the grid-frequency interface and enables simpler, lower-loss operation at very high power levels.

5.2 Limitations

The results demonstrate that the purpose and goals (Chapter 2) were achieved: a complete model of a large-scale (24 MW) wind energy conversion system was built, tested, and validated through simulation. The system showed strong performance in terms of output power delivery, DC voltage regulation, and compliance with power quality standards.

However, the study also highlighted limitations:

- Controller Design Sensitivity: The PI-based controllers were sufficient for steady-state operation, but transient responses showed oscillations and deviations. This suggests that real-world implementations would require robust control design, with hardware-in-the-loop testing before deployment.

- Grid Interaction: The inverter operated at unity power factor, but ancillary services (reactive power support, fault ride-through) were not tested, which are mandatory for modern grid codes.

6. Conclusion

This thesis has presented the modeling, analysis, and evaluation of a rectifier–boost–MMC inverter power train for a large-scale CRAFT wind turbine with a rated output of 24 MW. The study demonstrated that the combination of a passive diode rectifier, a multilevel DC–DC boost converter, and a modular multilevel inverter can deliver high efficiency, stable DC-link operation, and grid-compliant AC power at very high voltage and power levels.

The main contributions of the work can be summarized as follows:

- **Subsystem efficiency:** The combined rectifier + DC–DC boost converter achieved an efficiency of **99.70%**, corresponding to a total loss of ~69.9 kW. This very high efficiency highlights the potential of modular and multilevel topologies to operate effectively at MW-scale power levels with low losses. The overall system efficiency could not be determined, as inverter losses were not quantified within the scope of this study.

- **Loss breakdown:** The analysis showed that the DC–DC boost converter dominates the loss profile, with conduction and switching losses in the IGBTs accounting for over 95% of the rectifier + boost subsystem losses. The passive diode rectifier contributes only a small fraction (~1.8 kW), and passive component losses (inductor copper and capacitor ESR) are negligible by comparison. Inverter losses were not included in this analysis because the inverter was modeled with averaged Simulink blocks that do not capture semiconductor-level conduction or switching behavior.

- **Power quality:** The inverter output before filtering exhibited a voltage THD of ~2.27% and current THD of ~0.98%. After the RL filter, the voltage THD was reduced to 0% and the power factor reached unity. The DC-link voltage was highly stable, with ripple below 0.05% of the mean value and negligible high-frequency components.

Placed in a broader perspective, these results confirm that modular, multilevel converter topologies are highly suitable for next-generation offshore wind systems. In particular, for the CRAFT turbine concept, which targets reduced cost, counter-rotating generator design, and offshore robustness, the proposed power train provides a promising solution. It combines high efficiency, excellent power quality, and scalability to multi-megawatt levels, making it a viable candidate for future large-scale offshore deployment.

6.1 Future Work

While the project achieved its primary goals, several avenues remain open for further research and development:

1. Advanced Control Strategies:

   The PI-based current controllers exhibited small deviations in d-axis and circulating current tracking. More sophisticated methods such as model predictive control (MPC), resonant controllers (PR) for 2ω circulating components, or adaptive gain tuning could further enhance dynamic performance.
2. Loss and Efficiency Analysis:

   This thesis focused on voltage, current, and PQ performance but did not fully quantify semiconductor switching losses, conduction losses, or capacitor losses. A detailed efficiency model (including thermal performance) would provide a more complete picture of the system's economic viability.
3. Grid Support and Fault Ride-Through:

   The inverter operated at unity power factor with no reactive power control. Future work should implement reactive power support, fault ride-through (FRT) capability, and grid code compliance features to make the system suitable for real-world deployment.
4. Implement DC-DC boost converter with higher number of levels:

   Since the two-level model used in this study is not practically feasible at the required voltage and current ratings. A topology with higher number of levels would reduce the blocking voltage per device, enabling the use of commercially available IGBTs or SiC MOSFETs. Increasing the number of levels would also improve efficiency, lower switching stress, and enhance modularity. Future work should therefore focus on designing and validating such a multilevel boost converter through detailed simulations.
5. Investigate the impact of the DC-DC boost control on the machine:

   The dynamic behavior of the boost, including duty cycle modulation and current ripple, can influence generator torque pulsations and electromagnetic stress. Studying these interactions is essential to ensure stable operation and avoid excessive mechanical or electrical loading. Future work should therefore include coupled simulations of the boost converter and machine, as well as experimental validation under variable wind conditions.

In conclusion, this work demonstrates that the passive rectifier – multilevel boost – MMC inverter system is a promising and practical solution for very large offshore wind turbines. With further optimization of controls, efficiency analysis, and real-world validation, it can become a strong candidate for next-generation renewable power integration at the multi-megawatt, high-voltage scale.

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Annex

Intialization codes:

1. Variable Shaft Speed generation matlab code:

```
%% ---------- Settings ----------
% Long profile (physics time)
T_long   = 8960;          % seconds
dt       = 0.05;          % time step
t_long   = 0:dt:T_long;

% Compressed playback duration (display/animation time)
T_play   = 15;                        % seconds
time_scale = T_play / T_long;         % compress factor
t_play   = t_long * time_scale;       % compressed timestamps

% Shaft speed limits
nm_nom   = 1.2566;                    % rad/s
nm_min   = 0.8 * nm_nom;              % -20%
nm_max   = 1.2 * nm_nom;              % +20%

% Noise parameters
rng(1);                               % reproducible seed
tau_noise   = 50;                      % s, noise time constant
sigma_noise = 0.04 * nm_nom;           % noise magnitude (std)

% Mechanical inertia proxy: limit d(omega)/dt (slew-rate)
slew_time = 60;                         % s to swing ±20%
slew_max  = (0.2*nm_nom) / slew_time;   % rad/s^2 (max |dω/dt|)

%% ---------- Build noise-driven command ----------
% Generate low-pass filtered white noise
alpha = dt / max(dt + tau_noise, eps);  % filter coefficient
w = randn(size(t_long));                % white noise
noise_lp = zeros(size(t_long));
for k = 2:numel(t_long)
    noise_lp(k) = (1 - alpha)*noise_lp(k-1) + alpha * w(k);
end
nm_des = nm_nom + sigma_noise * noise_lp;

% Clip to ±20% limits
nm_des = min(max(nm_des, nm_min), nm_max);

%% ---------- Apply mechanical slew-rate limit ----------
nm = zeros(size(t_long));
nm(1) = nm_nom;
for k = 2:numel(t_long)
    step = nm_des(k) - nm(k-1);

    % Max allowed change
    max_step = slew_max * dt;

    % Rate-limit
    if step >  max_step, step =  max_step; end
    if step < -max_step, step = -max_step; end

    nm(k) = nm(k-1) + step;

    % Enforce hard limits
    if nm(k) > nm_max, nm(k) = nm_max; end
    if nm(k) < nm_min, nm(k) = nm_min; end
end

%% ---------- Compress in time ----------
timeVec = t_play; % compressed time vector
shaftspeed = nm';
shaft_speed_profile = [timeVec(:), shaftspeed(:)];

%% ---------- Plots ----------
figure('Name','Shaft Speed (physical time)');
plot(t_long, nm, 'LineWidth', 1);
xlabel('Time (s)'); ylabel('Shaft Speed \omega_m (rad/s)');
title('Natural Shaft Speed Profile (8960 s, noise-driven)');
grid on

figure('Name','Shaft Speed (compressed playback)');
plot(timeVec, nm, 'LineWidth', 1);
xlabel('Compressed Time (s)'); ylabel('Shaft Speed \omega_m (rad/s)');
title('Same Data, Time-Compressed to 15 s (no filtering/resampling)');
grid on
```

```
%% ---------- Save ----------
save('shaft_speed_profile.mat', 'timeVec', 'shaft_speed_profile');
```

2. DC-DC boost converter PLECS model initialization command:

```
dt = 500e-9;
fs = 16e3;

% boost 3L:
Lf = 5e-6;
LB = 4000e-6;
CB = 1000e-6;

% gerador:
VG = 10e3 / (sqrt(3)*sqrt(2)); % fase, pico
fG = 100;

% saída:
Vo = 60e3;
Po = 24e6;

Io = Po/Vo;
Ro = Vo/Io;

% Extract into variables for lookup tables
data1 = load('shaft_speed_profile.mat');
speed_data = data1.shaft_speed_profile;

timeVec = speed_data(:,1);
shaft_speed = speed_data(:,2);

% entrada - calc. ref corrente:
VL_rms = sqrt(3)*VG/sqrt(2);
VG_med = (3*sqrt(2)/pi)*VL_rms; % retif. 6 pulsos
IG_ref = (Po / VG_med) / 2;
```

3. 11-level inverter initialization MATLAB code:

```
%%-------------- Simulation MMC - Jessica Dohler  ------------------%

clear all
close all
clc

%% SImulation
Tstep=1e-6;
Stop_time=0.7;


%% Parameters of the grid
freq=50;
w_ref = 2*pi*freq;
Base_voltage_RMS_ph_ph=33e3; %voltage line RMS of grid
V_rms= Base_voltage_RMS_ph_ph; % line voltage
Vphase=V_rms/sqrt(3); % voltage phase
Vpeak= Vphase*sqrt(2);  % peak voltage
Vmax=V_rms*sqrt(2);

%% Parameters of the inverter
fs_inv = 2e3; %Switching frequency of the inverter (just if you want to change)
% fs_inv = 16e3; %Switching frequency of the inverter (just if you want to change)
T_carrier = 1 / fs_inv;

% Load the .mat file
load('Vout_PLECS.mat');  % This loads the variable 'data'

% Extract time and voltage vectors from rows (transpose to columns)
timeVec = data(1, :)';    % Row 1 -> column vector
VdcVec  = data(2, :)';    % Row 2 -> column vector

% Create a timeseries object (best for use in From Workspace block)
Vdc_ts = timeseries(VdcVec, timeVec);
Vdc_ts.Name = 'Vdc_ts';

% Save to a new .mat file for Simulink
save('Vdc_timeseries.mat', 'Vdc_ts');
Vdc=Vdc_ts;


% Load the .mat file
```

```
load('Iout_PLECS.mat');  % This loads the variable 'data'

% Extract time and voltage vectors from rows (transpose to columns)
timeVec1 = data(1, :)';    % Row 1 -> column vector
IdcVec  = data(2, :)';    % Row 2 -> column vector

% Create a timeseries object (best for use in From Workspace block)
Idc_ts = timeseries(IdcVec, timeVec1);
Idc_ts.Name = 'Idc_ts';

% Save to a new .mat file for Simulink
save('Idc_timeseries.mat', 'Idc_ts');
Idc=Idc_ts;

Smmc=50e6;

M=(2*Vphase)./Vdc; %modulation ratio MMC

%Levels of the inverter
n_level = 11;
n_modules = 5;

%% DC Capaitance calculation
e=.0500;
H=0.063661977236758;
cap_modules=0.0015;
cap_modules_TOT=2.94e-04;
init_voltage_modules=12000;
resistance_mod=1e-3;
snub_res_module=1e6;


%% Arm calculation
Larm=0.0431;
X= 13.5336;
Rarm=4.0601;

%% RL filter calculation
L=0.028; %indutor de acoplamento à rede
rL=2.69;


%% -----------  Constants for Decoupling block and current PI controls
% AC Current Control

rLac_eq= 4.7200;
Lac_eq = 0.0495;


%Gains
% kpi_inv = 16.5167;
% kii_inv = 1.5733e+03;

kpi_inv = 93.3;
kii_inv = 8.90e+03;


%% -----------  Constants for Decoupling block and current PI controls
% AC Circulating Current


qsi_1=0.7;
omega_n1=2*pi*30;

kpi_inv_cir = 33.8717;
kii_inv_cir =  1.7032e+04;


%% ---------  Constants for PLL block

omega_n2=2*pi*100;
qsi_2=0.7;
Kp_pll= (2*omega_n2*qsi_2)/Vpeak;
tal_pll= (Kp_pll*Vpeak)/(omega_n2)^2;
Ki_pll= (Kp_pll/tal_pll);


%% ----- Inverter control
% ---------------------- Ramp Reference ----------------------


Final_out_iq_ref=0;
Tramping_iq_ref=0.2;
Init_out_iq_ref=0;
```

```
Final_out_id_cir_ref=10;
Tramping_id_cir_ref=0.35;
Init_out_id_cir_ref=0;

Final_out_iq_cir_ref=0;
Tramping_iq_cir_ref=0.05;
Init_out_iq_cir_ref=0;

%% ----- Power control setpoint  (replace Vdc outer-loop params) -----
P_rated       = 24e6;           % 24 MW target at steady state
Init_out_Pref = 24e6;              % start at 0 W
Final_out_Pref= P_rated;        % ramp to rated
Tramping_Pref = 0.25;           % 0.25 s ramp (same idea as before)

% If you use a Step or Ramp source:
% Step at t = Tramping_Pref from Init_out_Pref to Final_out_Pref
% or use a rate limiter for a smooth ramp.

%% ----------------------  Vdc Control ----------------------



Kpv_inv= 4.1567e-07;
Kiv_inv=  1.3760e-05;


Ts     = 1/fs_inv;    % s
fc     = 150;         % Hz  (choose 100–200 Hz)
alpha  = exp(-2*pi*fc*Ts);
```

4. Inverter output power quality and THD analysis function MATLAB code:

```
function pq = analyze_pq_ac_phase(matfile, fundHz, Hmax, varargin)
% ANALYZE_PQ_AC_PHASE  AC PQ analysis from *PHASE* inputs only.
%   pq = analyze_pq_ac_phase('inverter_output_AC.mat', 50, 50, ...
%        'tSkip',0.2, 'Nc',20, 'autoFund',true, ...
%        'stripFund','none', 'plot',true, 'savePrefix','');
%
% Accepted MAT formats (phase-domain only):
%   - numeric Nx7: [t Va Vb Vc Ia Ib Ic]
%   - fields t,Va,Vb,Vc,Ia,Ib,Ic
%   - struct S.data as Nx7 above
%
% Outputs:
%   - THD classic and THD excl-1st (optionally stripping fundamental)
%   - True power, P1/Q1, PF(true)/PF(disp), VUF (from phase phasors)
%   - Per-phase spectra (projection-based), tables, and optional plots

% ---------- options ----------
p = inputParser;
p.addParameter('tSkip',0, @(x)isnumeric(x)&&isscalar(x)&&x>=0);
p.addParameter('Nc',20, @(x)isnumeric(x)&&isscalar(x)&&x>=3);
p.addParameter('autoFund', true, @(x)islogical(x)&&isscalar(x));
p.addParameter('stripFund','none', @(s)ischar(s)||isstring(s)); % 'none'|'both'|'voltage'|'current'
p.addParameter('plot',true, @(x)islogical(x)&&isscalar(x));
p.addParameter('savePrefix','', @(s)ischar(s)||isstring(s));
p.parse(varargin{:});
opt = p.Results;

% ---------- load (phases only) ----------
S = load(matfile);
[t, Va,Vb,Vc, Ia,Ib,Ic] = extract_phases_only(S); % <-- phase-only

% ---------- fundamental ----------
if nargin<2 || isempty(fundHz) || fundHz<0.2 || fundHz>400
    if opt.autoFund
        fundHz = estimate_fundamental(t, (Va+Vb+Vc)/3, 0.2, 200);
        fprintf('Auto-detected fundamental: %.6f Hz\n', fundHz);
    else
        error('Provide fundHz or set ''autoFund'', true.');
    end
end
if nargin<3 || isempty(Hmax), Hmax=50; end

% ---------- skip transient ----------
keep = t>=opt.tSkip; t=t(keep);
Va=Va(keep); Vb=Vb(keep); Vc=Vc(keep);
Ia=Ia(keep); Ib=Ib(keep); Ic=Ic(keep);

% ---------- window last Nc cycles ----------
T0 = 1/fundHz;
NcAvail = floor((t(end)-t(1))/T0);
Nc = max(3, min(opt.Nc, NcAvail));
```

```matlab
if Nc < opt.Nc
    fprintf('Note: using %d cycles (limited by data after tSkip).\n', Nc);
end
t1 = t(end) - Nc*T0; use = (t>=t1);
t=t(use); Va=Va(use); Vb=Vb(use); Vc=Vc(use);
Ia=Ia(use); Ib=Ib(use); Ic=Ic(use);

% ---------- prep for THD (optionally remove 50 Hz for residual THD only) ----------
Va_forTHD=Va; Vb_forTHD=Vb; Vc_forTHD=Vc;
Ia_forTHD=Ia; Ib_forTHD=Ib; Ic_forTHD=Ic;
if ~strcmpi(opt.stripFund,'none')
    rmV = any(strcmpi(opt.stripFund, {'both','voltage'}));
    rmI = any(strcmpi(opt.stripFund, {'both','current'}));
    if rmV
        [Va_forTHD, ~] = remove_fund_projection(t, Va, fundHz);
        [Vb_forTHD, ~] = remove_fund_projection(t, Vb, fundHz);
        [Vc_forTHD, ~] = remove_fund_projection(t, Vc, fundHz);
    end
    if rmI
        [Ia_forTHD, ~] = remove_fund_projection(t, Ia, fundHz);
        [Ib_forTHD, ~] = remove_fund_projection(t, Ib, fundHz);
        [Ic_forTHD, ~] = remove_fund_projection(t, Ic, fundHz);
    end
end

% ---------- spectra (projection at k*f0) ----------
Fs = 1/mean(diff(t));
specV_A = single_spectrum_proj(Va, Fs, fundHz, Hmax);
specV_B = single_spectrum_proj(Vb, Fs, fundHz, Hmax);
specV_C = single_spectrum_proj(Vc, Fs, fundHz, Hmax);
specI_A = single_spectrum_proj(Ia, Fs, fundHz, Hmax);
specI_B = single_spectrum_proj(Ib, Fs, fundHz, Hmax);
specI_C = single_spectrum_proj(Ic, Fs, fundHz, Hmax);

specV_A_res = single_spectrum_proj(Va_forTHD, Fs, fundHz, Hmax);
specV_B_res = single_spectrum_proj(Vb_forTHD, Fs, fundHz, Hmax);
specV_C_res = single_spectrum_proj(Vc_forTHD, Fs, fundHz, Hmax);
specI_A_res = single_spectrum_proj(Ia_forTHD, Fs, fundHz, Hmax);
specI_B_res = single_spectrum_proj(Ib_forTHD, Fs, fundHz, Hmax);
specI_C_res = single_spectrum_proj(Ic_forTHD, Fs, fundHz, Hmax);

% ---------- THD classic and excl-1st ----------
THD_V_classic = [thd_from_spec(specV_A), thd_from_spec(specV_B), thd_from_spec(specV_C)];
THD_I_classic = [thd_from_spec(specI_A), thd_from_spec(specI_B), thd_from_spec(specI_C)];

V1 = [max(specV_A.harmRMS(1),eps), max(specV_B.harmRMS(1),eps), max(specV_C.harmRMS(1),eps)];
I1 = [max(specI_A.harmRMS(1),eps), max(specI_B.harmRMS(1),eps), max(specI_C.harmRMS(1),eps)];

THD_V_excl1 = [ ...
  sqrt(sum(specV_A_res.harmRMS(2:end).^2))/V1(1), ...
  sqrt(sum(specV_B_res.harmRMS(2:end).^2))/V1(2), ...
  sqrt(sum(specV_C_res.harmRMS(2:end).^2))/V1(3) ];
THD_I_excl1 = [ ...
  sqrt(sum(specI_A_res.harmRMS(2:end).^2))/I1(1), ...
  sqrt(sum(specI_B_res.harmRMS(2:end).^2))/I1(2), ...
  sqrt(sum(specI_C_res.harmRMS(2:end).^2))/I1(3) ];

% ---------- phasors and sequences (from phase signals) ----------
Va1p = proj_phasor_rms(Va, t, fundHz);
Vb1p = proj_phasor_rms(Vb, t, fundHz);
Vc1p = proj_phasor_rms(Vc, t, fundHz);
Ia1  = proj_phasor_rms(Ia, t, fundHz);
Ib1  = proj_phasor_rms(Ib, t, fundHz);
Ic1  = proj_phasor_rms(Ic, t, fundHz);

a = exp(1j*2*pi/3);
Vpos = (Va1p + a*Vb1p + a^2*Vc1p)/3;
Vneg = (Va1p + a^2*Vb1p + a*Vc1p)/3;
Ipos = (Ia1  + a*Ib1   + a^2*Ic1 )/3;
Ineg = (Ia1  + a^2*Ib1 + a*Ic1  )/3;
VUF  = abs(Vneg)/max(abs(Vpos), eps);

% ---------- powers ----------
p_inst = Va.*Ia + Vb.*Ib + Vc.*Ic;  P_true = mean(p_inst);
P_max  = max(p_inst); P_min = min(p_inst); P_rms = rms(p_inst);

S1_ph = [Va1p;Vb1p;Vc1p] .* conj([Ia1;Ib1;Ic1]);
S1 = sum(S1_ph); P1 = real(S1); Q1 = imag(S1);

% Robust apparent power (works with unbalance + harmonics)
Vrms = [rms(Va) rms(Vb) rms(Vc)];
Irms = [rms(Ia) rms(Ib) rms(Ic)];
S_total_rms = sqrt( sum(Vrms.^2) * sum(Irms.^2) );

PF_true = P_true / max(S_total_rms, eps);  % real ÷ apparent, consistent
```

```
PF_disp = cos(angle(S1));                  % fundamental-only PF

% ---------- tables & plots ----------
tblV_A = make_harmonic_table(specV_A, 'Voltage_PhaseA');
tblV_B = make_harmonic_table(specV_B, 'Voltage_PhaseB');
tblV_C = make_harmonic_table(specV_C, 'Voltage_PhaseC');
tblI_A = make_harmonic_table(specI_A, 'Current_PhaseA');
tblI_B = make_harmonic_table(specI_B, 'Current_PhaseB');
tblI_C = make_harmonic_table(specI_C, 'Current_PhaseC');

if ~isempty(opt.savePrefix)
    writetable(tblV_A, sprintf('%s_Vharm_A.csv', opt.savePrefix));
    writetable(tblV_B, sprintf('%s_Vharm_B.csv', opt.savePrefix));
    writetable(tblV_C, sprintf('%s_Vharm_C.csv', opt.savePrefix));
    writetable(tblI_A, sprintf('%s_Iharm_A.csv', opt.savePrefix));
    writetable(tblI_B, sprintf('%s_Iharm_B.csv', opt.savePrefix));
    writetable(tblI_C, sprintf('%s_Iharm_C.csv', opt.savePrefix));
end
if opt.plot
    plot_harmonics(struct('phaseA',specV_A,'phaseB',specV_B,'phaseC',specV_C), ...
        'Voltage Harmonics (Phase RMS)','V (RMS)');
    plot_harmonics(struct('phaseA',specI_A,'phaseB',specI_B,'phaseC',specI_C), ...
        'Current Harmonics (Phase RMS)','A (RMS)');
end

% ---------- pack ----------
pq.meta.file = matfile; pq.meta.fundHz = fundHz; pq.meta.Hmax = Hmax;
pq.meta.Ncycles = Nc; pq.meta.tSkip = opt.tSkip;
pq.meta.stripFund = opt.stripFund;

pq.thd.voltage.classic_perPhase = THD_V_classic;
pq.thd.current.classic_perPhase = THD_I_classic;
pq.thd.voltage.classic_avg = mean(THD_V_classic);
pq.thd.current.classic_avg = mean(THD_I_classic);

pq.thd.voltage.excl1_perPhase = THD_V_excl1;
pq.thd.current.excl1_perPhase = THD_I_excl1;
pq.thd.voltage.excl1_avg = mean(THD_V_excl1);
pq.thd.current.excl1_avg = mean(THD_I_excl1);

pq.fund.Vpos = Vpos; pq.fund.Vneg = Vneg; pq.fund.Ipos = Ipos; pq.fund.Ineg = Ineg;
pq.balance.VUF = VUF;

pq.fund.Va1 = Va1p; pq.fund.Vb1 = Vb1p; pq.fund.Vc1 = Vc1p;
pq.fund.Ia1 = Ia1;  pq.fund.Ib1 = Ib1;  pq.fund.Ic1 = Ic1;

pq.powers.P_true_W = P_true; pq.fund.P1_W = P1; pq.fund.Q1_var = Q1;
pq.pf.true = PF_true; pq.pf.displacement = PF_disp;

pq.spectra.voltage.A = specV_A; pq.spectra.voltage.B = specV_B; pq.spectra.voltage.C = specV_C;
pq.spectra.current.A = specI_A; pq.spectra.current.B = specI_B; pq.spectra.current.C = specI_C;

pq.tables.VA = tblV_A; pq.tables.VB = tblV_B; pq.tables.VC = tblV_C;
pq.tables.IA = tblI_A; pq.tables.IB = tblI_B; pq.tables.IC = tblI_C;

% ---------- print ----------
fprintf('\n=== AC PQ Summary (%s) ===\n', matfile);
fprintf('f0: %.6f Hz | Window: %d cycles | tSkip: %.3f s\n', fundHz, Nc, opt.tSkip);
fprintf('V THD classic (%%): [%.4f  %.4f  %.4f] | Avg=%.4f%%\n', ...
    100*THD_V_classic, 100*mean(THD_V_classic));
fprintf('I THD classic (%%): [%.4f  %.4f  %.4f] | Avg=%.4f%%\n', ...
    100*THD_I_classic, 100*mean(THD_I_classic));
if ~strcmpi(opt.stripFund,'none')
  fprintf('V THD excl-1st (%%): [%.4f  %.4f  %.4f] | Avg=%.4f%%  (fund removed)\n', ...
      100*THD_V_excl1, 100*mean(THD_V_excl1));
  fprintf('I THD excl-1st (%%): [%.4f  %.4f  %.4f] | Avg=%.4f%%  (fund removed)\n', ...
      100*THD_I_excl1, 100*mean(THD_I_excl1));
end
fprintf('P_true: %.3f MW | P1: %.3f MW | Q1: %.3f Mvar\n', ...
    P_true/1e6, P1/1e6, Q1/1e6);
fprintf('P_true: %.3f MW | P_max: %.3f MW | P_min: %.3f MW | P_rms: %.3f MW\n', ...
        P_true/1e6, P_max/1e6, P_min/1e6, P_rms/1e6);
fprintf('PF(true)=%.3f | PF(disp)=%.3f | VUF=%.4f%%\n', PF_true, PF_disp, 100*VUF);
end

% ================== helpers ==================

function [t, Va,Vb,Vc, Ia,Ib,Ic] = extract_phases_only(S)
% Accept only phase-domain signals. Error otherwise.
if all(isfield(S,{'t','Va','Vb','Vc','Ia','Ib','Ic'}))
    t=S.t(:); Va=S.Va(:); Vb=S.Vb(:); Vc=S.Vc(:); Ia=S.Ia(:); Ib=S.Ib(:); Ic=S.Ic(:); return;
end
if isfield(S,'data') && isnumeric(S.data)
    A = S.data; if size(A,1)<size(A,2), A=A.'; end
    if size(A,2)==7
```

```
        t=A(:,1); Va=A(:,2); Vb=A(:,3); Vc=A(:,4); Ia=A(:,5); Ib=A(:,6); Ic=A(:,7);
        t=t(:); Va=Va(:); Vb=Vb(:); Vc=Vc(:); Ia=Ia(:); Ib=Ib(:); Ic=Ic(:); return;
    else
        error('S.data must be Nx7 [t Va Vb Vc Ia Ib Ic] for phase-domain.');
    end
end
% try single numeric field
fn = fieldnames(S);
if numel(fn)==1 && isnumeric(S.(fn{1}))
    A = S.(fn{1}); if size(A,1)<size(A,2), A=A.'; end
    if size(A,2)==7
        t=A(:,1); Va=A(:,2); Vb=A(:,3); Vc=A(:,4); Ia=A(:,5); Ib=A(:,6); Ic=A(:,7);
        t=t(:); Va=Va(:); Vb=Vb(:); Vc=Vc(:); Ia=Ia(:); Ib=Ib(:); Ic=Ic(:); return;
    else
        error('Numeric array must be Nx7 [t Va Vb Vc Ia Ib Ic] for phase-domain.');
    end
end
error('Could not detect phase-domain AC data. Provide [t Va Vb Vc Ia Ib Ic].');
end

function f0 = estimate_fundamental(t, x, fmin, fmax)
x = x(:)-mean(x);
N=numel(x); Ts=mean(diff(t)); Fs=1/Ts;
x=x(round(N/3):end); N=numel(x);
w=hann(N); X=fft(x.*w); f=(0:N-1)*Fs/N;
X=X(1:floor(N/2)+1); f=f(1:floor(N/2)+1);
band=(f>=fmin)&(f<=fmax); [~,k]=max(abs(X(band))); idx=find(band);
f0=f(idx(k));
end

function out = single_spectrum_proj(x, Fs, f0, Hmax)
x = x(:) - mean(x);
N = numel(x); t = (0:N-1).' / Fs;
w = hann(N); xw = x .* w; Wm = mean(w);
harms = (1:Hmax)*f0; harms = harms(harms < Fs/2);
H = numel(harms); Xh = zeros(H,1);
for k=1:H
    wk = 2*pi*harms(k);
    c  = mean( xw .* exp(-1j*wk*(t - t(1))) ) / Wm;   % complex RMS/√2
    Xh(k) = sqrt(2) * c;                              % complex RMS phasor
end
out.hz      = harms(:);
out.harmRMS = abs(Xh(:));  % per-harmonic RMS magnitudes
end

function THD = thd_from_spec(sp)
if isempty(sp.harmRMS), THD = NaN; return; end
H1 = max(sp.harmRMS(1), eps);
THD = sqrt(sum(sp.harmRMS(2:end).^2)) / H1;
end

function [x_noF, xF] = remove_fund_projection(t, x, f0)
t = t(:); x = x(:);
w0 = 2*pi*f0; N = numel(t);
tw = t - t(1); win = hann(N);
xw  = x .* win;
c   = mean( xw .* exp(-1j*w0*tw) ) / mean(win);  % complex RMS/√2
xF  = sqrt(2) * real( c .* exp(1j*w0*tw) );
x_noF = x - xF;
end

function X1 = proj_phasor_rms(x, t, f0)
x = x(:); t = t(:);
w = 2*pi*f0;
c = mean( (x - mean(x)) .* exp(-1j*w*(t - t(1))) ); % ~ Vrms/√2 * e^{jϕ}
X1 = sqrt(2) * c;                                   % Vrms ∠
end

function T = make_harmonic_table(specPhase, label)
ord=(1:numel(specPhase.harmRMS)).';
T=table(ord, specPhase.hz(:), specPhase.harmRMS(:), ...
    'VariableNames', {'HarmonicOrder','Frequency_Hz','RMS'});
T.Properties.Description = sprintf('%s | THD = %.4f %%', label, ...
    100*sqrt(sum(specPhase.harmRMS(2:end).^2))/max(specPhase.harmRMS(1),eps));
end

function plot_harmonics(spec, titleStr, ylab)
harms=spec.phaseA.hz(:);
A=[spec.phaseA.harmRMS, spec.phaseB.harmRMS, spec.phaseC.harmRMS];
figure('Name',titleStr);
tiledlayout(3,1,'Padding','compact','TileSpacing','compact');
nexttile; bar(harms, A(:,1)); grid on; ylabel(ylab); title(sprintf('%s - Phase A', titleStr));
nexttile; bar(harms, A(:,2)); grid on; ylabel(ylab); title('Phase B');
nexttile; bar(harms, A(:,3)); grid on; ylabel(ylab); xlabel('Frequency (Hz)'); title('Phase C');
end
```

5. DC-DC boost converter output power quality and THD analysis function MATLAB code:

```
function dc = analyze_dc_link(matfile, varargin)
% ANALYZE_DC_LINK  DC bus power-quality and ripple THD analyzer.
%   dc = analyze_dc_link('DC_boost_output.mat', ...
%        'tSkip',0.5, 'Nc',20, 'Hmax',50, ...
%        'autoRipple',true, 'gridFundHz',[], 'rippleMult','auto', ...
%        'fr_hint',[], 'fsw',[16e3 2*16e3 3*16e3], 'plot',true);
%
% INPUT MAT formats accepted:
%   - Nx2 [t Vdc]
%   - Nx3 [t Vdc Idc]
%   - struct with fields t,Vdc,(Idc) or S.data with 2 or 3 cols
%
% Outputs printed and returned in struct 'dc':
%   dc.t, dc.vdc, dc.idc (if present)
%   dc.mean.Vdc, dc.ripple.Vrms, dc.Vpp
%   dc.ripple.fr (fundamental), dc.ripple.THD, dc.ripple.V1_rms
%   dc.switchingBands (if fsw provided): RMS around fsw, 2fsw, 3fsw
%   dc.idc.mean, dc.idc.rippleRMS (if Idc available)
%   dc.power.Pavg, dc.power.Pripple_rms (if Idc available)

% ---------- options ----------
p = inputParser;
p.addParameter('tSkip',0, @(x)isnumeric(x)&&isscalar(x)&&x>=0);
p.addParameter('Nc',20, @(x)isnumeric(x)&&isscalar(x)&&x>=3);
p.addParameter('Hmax',50, @(x)isnumeric(x)&&isscalar(x)&&x>=3);

% New options
p.addParameter('autoRipple', false, @(x)islogical(x)||ischar(x)||isstring(x));  % true/false or
'detect'|'2x'|'6x'
p.addParameter('gridFundHz', [], @(x)isempty(x)||(isnumeric(x)&&isscalar(x)&&x>0));
p.addParameter('rippleMult', 'auto', @(s)ischar(s)||isstring(s));               % 'auto'|'2x'|'6x'

% Backward-compatible hint
p.addParameter('fr_hint',[], @(x)isempty(x)||(isnumeric(x)&&isscalar(x)&&x>0));

p.addParameter('fsw',[], @(x)isnumeric(x));     % vector of switching freqs to report band RMS
p.addParameter('plot',true, @(x)islogical(x)&&isscalar(x));
p.parse(varargin{:});
opt = p.Results;

% ---------- load ----------
S = load(matfile);
[t, vdc, idc] = extract_dc(S);

% ---------- skip transient ----------
keep = t >= opt.tSkip;
t = t(keep); vdc = vdc(keep);
if ~isempty(idc), idc = idc(keep); end

% ---------- choose ripple fundamental fr ----------
fr = [];
% Highest priority: explicit fr_hint
if ~isempty(opt.fr_hint)
    fr = opt.fr_hint;
else
    % Next: autoRipple selection
    if islogical(opt.autoRipple) && opt.autoRipple
        % detect from DC waveform (largest non-DC spectral line)
        fr = estimate_ripple_fundamental(t, vdc - mean(vdc), 1, 0.8*(1/(2*mean(diff(t)))));
    elseif ischar(opt.autoRipple) || isstring(opt.autoRipple)
        mode = lower(string(opt.autoRipple));
        switch mode
            case "detect"
                fr = estimate_ripple_fundamental(t, vdc - mean(vdc), 1, 0.8*(1/(2*mean(diff(t)))));
            case {"2x","6x"}
                % need a gridFundHz (if missing, fall back to detect)
                if ~isempty(opt.gridFundHz)
                    mult = double(mode=="6x")*6 + double(mode=="2x")*2;
                    fr = mult * opt.gridFundHz;
                else
                    fr = estimate_ripple_fundamental(t, vdc - mean(vdc), 1, 0.8*(1/(2*mean(diff(t)))));
                end
            otherwise
                % unknown string -> fall back to detect
                fr = estimate_ripple_fundamental(t, vdc - mean(vdc), 1, 0.8*(1/(2*mean(diff(t)))));
        end
    else
        % autoRipple disabled: optionally derive from gridFundHz + rippleMult
        if ~isempty(opt.gridFundHz)
            if strcmpi(opt.rippleMult,'6x'), fr = 6*opt.gridFundHz;
            elseif strcmpi(opt.rippleMult,'2x'), fr = 2*opt.gridFundHz;
            else, fr = estimate_ripple_fundamental(t, vdc - mean(vdc), 1, 0.8*(1/(2*mean(diff(t)))));
```

```
            end
        else
            % Final fallback: detect
            fr = estimate_ripple_fundamental(t, vdc - mean(vdc), 1, 0.8*(1/(2*mean(diff(t)))));
        end
    end
end

% ---------- window last Nc cycles of ripple ----------
T0 = 1/fr;
NcAvail = floor((t(end)-t(1))/T0);
Nc = max(3, min(opt.Nc, NcAvail));
t1 = t(end) - Nc*T0;
use = t >= t1;
t = t(use); vdc = vdc(use); if ~isempty(idc), idc = idc(use); end

% ---------- metrics ----------
Vdc_mean = mean(vdc);
Vr = vdc - Vdc_mean;
Vr_rms = rms(Vr);
Vpp = max(vdc) - min(vdc);

% ripple THD via projection at k*fr
rip = dc_ripple_metrics(t, vdc, opt.Hmax, fr);

% switching band RMS (optional)
sw = [];
if ~isempty(opt.fsw)
    Fs = 1/mean(diff(t));
    for k=1:numel(opt.fsw)
        sw(k) = switching_band_metrics(Vr, Fs, opt.fsw(k)); %#ok<AGROW>
    end
end

% current / power if available
if isempty(idc)
    Idc_mean = NaN; Ir_rms = NaN; Pavg = NaN; Pripple_rms = NaN;
else
    Idc_mean = mean(idc);
    Ir_rms = rms(idc - Idc_mean);
    p_inst = vdc .* idc;
    Pavg = mean(p_inst);
    Pripple_rms = rms(p_inst - Pavg);
end

% ---------- pack ----------
% ---------- pack ----------
dc.meta.file = matfile;
dc.meta.Nc = Nc; dc.meta.fr = rip.fr; dc.meta.tSkip = opt.tSkip;
dc.meta.autoRipple = opt.autoRipple;
dc.meta.gridFundHz = opt.gridFundHz;
dc.meta.rippleMult = opt.rippleMult;

% Store signals
dc.signals.t   = t;
dc.signals.vdc = vdc;
dc.signals.idc = idc;

% Store results
dc.mean.Vdc        = Vdc_mean;
dc.ripple.Vrms     = Vr_rms;
dc.Vpp             = Vpp;
dc.ripple.fr       = rip.fr;
dc.ripple.THD      = rip.THD;
dc.ripple.V1_rms   = rip.V1_rms;
dc.ripple.hz       = rip.hz;
dc.ripple.harmRMS = rip.harmRMS;

if ~isempty(opt.fsw)
    dc.switchingBands = sw;
else
    dc.switchingBands = [];
end

dc.idc.mean        = Idc_mean;
dc.idc.rippleRMS   = Ir_rms;
dc.power.Pavg      = Pavg;
dc.power.Pripple_rms = Pripple_rms;

% ---------- print ----------
fprintf('=== DC-Link PQ Summary (%s) ===\n', matfile);
fprintf('Window: %.3f-%.3f s (last %d cycles @ fr=%.3f Hz)\n', t(1), t(end), Nc, rip.fr);
fprintf('Vdc_mean = %.1f V | Vripple_rms = %.3f V (%.3f %%) | Vpp = %.1f V\n', ...
    Vdc_mean, Vr_rms, 100*Vr_rms/max(Vdc_mean,eps), Vpp);
fprintf('Ripple THD (harmonics of %.3f Hz): %.2f %%\n', rip.fr, 100*rip.THD);
```

```matlab
if ~isempty(opt.fsw)
    for k=1:numel(opt.fsw)
        fprintf('Switching band RMS @ %.0f Hz: %.3f V\n', opt.fsw(k), sw(k));
    end
end

if ~isempty(idc)
    fprintf('Idc_mean = %.3f A | Iripple_rms = %.3f A\n', Idc_mean, Ir_rms);
    fprintf('Pavg = %.3f MW | Pripple_rms = %.2f kW (%.3f %%)\n', ...
        Pavg/1e6, Pripple_rms/1e3, 100*Pripple_rms/max(Pavg,eps));
end
end


% ================ helpers ================

function [t, vdc, idc] = extract_dc(S)
idc = [];
if all(isfield(S, {'t','Vdc'}))
    t=S.t(:); vdc=S.Vdc(:);
    if isfield(S,'Idc'), idc=S.Idc(:); end
    return
end
if isfield(S,'data') && isnumeric(S.data)
    A = S.data;
elseif isstruct(S)
    fn = fieldnames(S);
    if numel(fn)==1 && isnumeric(S.(fn{1})), A = S.(fn{1});
    else, error('Unsupported MAT structure for DC link.');
    end
else
    A = S;
end
if size(A,1) < size(A,2), A = A.'; end
if size(A,2)==2
    t=A(:,1); vdc=A(:,2);
elseif size(A,2)>=3
    t=A(:,1); vdc=A(:,2); idc=A(:,3);
else
    error('Expect Nx2 [t Vdc] or Nx3 [t Vdc Idc].');
end
t=t(:); vdc=vdc(:); if ~isempty(idc), idc=idc(:); end
end

function fr = estimate_ripple_fundamental(t, x, fmin, fmax)
x = x(:)-mean(x); N=numel(x); Ts=mean(diff(t)); Fs=1/Ts;
w=hann(N); X=fft(x.*w); f=(0:N-1)*Fs/N;
X=X(1:floor(N/2)+1); f=f(1:floor(N/2)+1);
band=(f>=fmin)&(f<=fmax); [~,k]=max(abs(X(band))); idx=find(band);
fr = f(idx(k));
end

function rip = dc_ripple_metrics(t, vdc, Hmax, fr_hint)
v = vdc(:); t = t(:);
Ts = mean(diff(t)); Fs = 1/Ts;
vr = v - mean(v);
if isempty(fr_hint)
    fr = estimate_ripple_fundamental(t, vr, 1, 0.8*Fs/2);
else
    fr = fr_hint;
end
fNyq = Fs/2; harms = (1:Hmax)*fr; harms = harms(harms < fNyq); H=numel(harms);
N=numel(vr); w=hann(N); tw=(t - t(1)); vrw=vr.*w; Wm=mean(w);
Hrms = zeros(H,1);
for k=1:H
    wk=2*pi*harms(k);
    c = mean( vrw .* exp(-1j*wk*tw) ) / Wm;
    Hrms(k) = abs(sqrt(2)*c);
end
V1 = max(Hrms(1), eps);
THD = sqrt(sum(Hrms(2:end).^2))/V1;
rip.fr=fr; rip.hz=harms(:); rip.harmRMS=Hrms(:); rip.THD=THD; rip.V1_rms=V1;
end

function r = switching_band_metrics(x, Fs, f0)
% Narrow RMS around f0 (±0.5% BW), zero-phase IIR
bw = max(1.0, 0.005*f0); f1=max(0.1,f0-bw); f2=min(Fs/2*0.99,f0+bw);
d = designfilt('bandpassiir','FilterOrder',4,'HalfPowerFrequency1',f1,...
    'HalfPowerFrequency2',f2,'DesignMethod','butter','SampleRate',Fs);
xr = filtfilt(d, x(:));
r = rms(xr);
end
```

6. Loss calculation MATLAB code

```matlab
%% Rated values
Pout = 24e6;        % Output power [W]
Vout_dc = 60e3;     % Boost output voltage [V]
Vin_dc  = 30e3;     % Boost input voltage [V]
Iout_dc = Pout / Vout_dc;             % Output current [A]
D = 1 - Vin_dc/Vout_dc;               % Duty cycle
IL = Iout_dc / (1 - D);               % Boost inductor current [A]

%% Rectifier diode parameters
VT0 = 1.845;              % Threshold voltage [V]
rT  = 0.951e-3;           % Differential resistance [Ohm]
Idc = Iout_dc;            % DC output current [A]
Iavg_diode = Idc/3;       % Each diode average current
Irms_diode = Idc/sqrt(3);% Each diode RMS current
P_diode_cond = VT0*Iavg_diode + rT*Irms_diode^2; % Per diode
P_rect = 6 * P_diode_cond; % Total rectifier loss

%% Boost IGBT parameters (assumed 11-level topology)
Vcesat = 2.0;             % IGBT saturation voltage [V]
Eon = 20e-3;              % Turn-on energy [J]
Eoff = 25e-3;             % Turn-off energy [J]
fs_boost = 16e3;          % Switching frequency [Hz]
n_series = 1;             % Series IGBTs per SM
n_par = 2;                % Parallel IGBTs per SM
Nlev_boost = 11;          % Number of boost levels
Npaths = 2;               % Number of conduction paths
Nins = Nlev_boost;        % Inserted submodules
Isw_dev = IL/n_par;       % Current per device [A]

% Boost conduction loss
Ncond_boost = Npaths * Nins * n_series * n_par;
P_cond_boost = Ncond_boost * Vcesat * Isw_dev;

% Boost switching loss
Nsw_boost = Npaths * Nins * n_series * n_par;
Esw_dev = Eon + Eoff; % [J]
P_sw_boost = Nsw_boost * fs_boost * Esw_dev;

%% Inductor parameters
Rdc_L = 1e-3;             % Inductor winding resistance [Ohm]
P_inductor = IL^2 * Rdc_L; % Per inductor
Nind = 2;                 % Number of inductors
P_ind_tot = Nind * P_inductor;

%% Capacitor parameters
Resr = 2e-3;              % Equivalent series resistance [Ohm]
Vrms_cap = 22.9;          % Example ripple voltage [V]
fr = 112;                 % Ripple frequency [Hz]
Ceq = 1000e-6;            % Capacitance [F]
Irms_cap = 2*pi*fr*Ceq*Vrms_cap;
P_cap = Irms_cap^2 * Resr;


%% Total losses
P_loss_tot = P_rect + P_cond_boost + P_sw_boost + P_ind_tot + P_cap ;
eta = Pout / (Pout + P_loss_tot);

%% Generate breakdown table
LossNames = { ...
    'Rectifier conduction loss', ...
    'Boost conduction loss', ...
    'Boost switching loss', ...
    'Inductor copper loss', ...
    'Capacitor ESR loss', ...
    'Total loss', ...
    'Efficiency'};

LossValues = [ ...
    P_rect, ...
    P_cond_boost, ...
    P_sw_boost, ...
    P_ind_tot, ...
    P_cap, ...
    P_loss_tot, ...
    eta*100]; % Efficiency in %
Units = { ...
    'W', 'W', 'W', 'W', 'W', 'W', '%'};
T = table(LossNames', LossValues', Units', 'VariableNames', {'LossComponent','Value','Unit'});

%% Display table
disp(T);
```