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# Electro-Acoustic and Electronic Applications Utilizing Thin Film Aluminium Nitride

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#### **Abstract**

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In recent years there has been a huge increase in the growth of communication systems such as mobile phones, wireless local area networks (WLAN), satellite navigation and various other forms of wireless data communication that have made analogue frequency control a key issue. The increase in frequency spectrum crowding and the increase of frequency into microwave region, along with the need for minimisation and capacity improvement, has shown the need for the development of high performance, miniature, on-chip filters operating in the low to medium GHz frequency range. This has hastened the need for alternatives to ceramic resonators due to their limits in device size and performance, which in turn, has led to development of the thin film electro-acoustics industry with surface acoustic wave (SAW) and bulk acoustic wave (BAW) filters now fabricated in their millions. Further, this new technology opens the way for integrating the traditionally incompatible integrated circuit (IC) and electro-acoustic (EA) technologies, bringing about substantial economic and performance benefits.

In this thesis the compatibility of aluminium nitride (AlN) to IC fabrication is explored as a means for furthering integration issues. Various issues have been explored where either tailoring thin film bulk acoustic resonator (FBAR) design, such as development of an improved solidly mounted resonator (SMR) technology, and use of IC technology, such as chemical mechanical polishing (CMP) or nickel silicide (NiSi), has made improvements beneficial for resonator fabrication or enabled IC integration. The former has resulted in major improvements to Quality factor, power handling and encapsulation respectively. The later has provided alternative methods to reduce electro- or acoustomigration, reduced device size, for plate waves, supplied novel low acoustic impedance material for high power applications and alternative electrodes for use in high temperature sensors.

Another method to enhance integration by using the piezoelectric material, AlN, in the IC side has also been explored. Here methods for analysing AlN film contamination and stoichiometry have been used for analysis of AlN as a high-k dielectric material. This has even brought benefits in knowledge of film composition for use as a passivation material with SiC substrates, investigated in high power high frequency applications. Lastly AlN has been used as a buried insulator material for new silicon-on-insulator substrates (SOI) for increased heat conduction. These new substrates have been analysed with further development for improved performance indicated.

**Keywords:** AlN, FBAR, FPAR, CMP, SOI, Nickel Silicide, Wafer Bonding

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*To Rebecca and Eliot*



# List of Papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

- I D. M. Martin, V. Yantchev and I. Katardjiev, “**Buried electrode electroacoustic technology for the fabrication of thin film based resonant components**”, J. Micromech. Microeng., **16**, 1869–74, 2006.
- II J. Enlund, D. Martin, V. Yantchev and I. Katardjiev, “**Solidly mounted thin film electro-acoustic resonator utilizing a conductive Bragg reflector**”, Sensors and Actuators A. **141**, 598-602, 2008.
- III J. Enlund, D. M. Martin, V. Yantchev and I. Katardjiev, “**Q-degradation and crosstalk in BAW sensor arrays operating in conductive liquid media**”, submitted to IEEE 2009 sensors, 2009.
- IV D. M. Martin, U. Smith, V. Yantchev, J. Olsson and I. Katardjiev, “**Thick NiSi electrodes for AlN electro-acoustic applications**”, Electrochemical and Solid-State Letters, **12** (5), H182-4, 2009.
- V D. M. Martin, J. Enlund, U. Smith, V. Yantchev, J. Olsson and I. Katardjiev, “**Thick silicides synthesised with smooth surface for integrated TFBAR applications**”, submitted to J. Micromech. Microeng., 2009.
- VI D. M. Martin, J. Enlund, O. Kappertz and J. Jensen “**Comparing XPS and ToF-ERDA measurement of high-k dielectric materials**”, J. Phys.: Conf. Ser. **100** 012036, 2008.
- VII M. Wolborski, D. M. Martin, M. Bakowski, A. Hallén and I. Katardjiev, “**Improved Properties of AlON/4H-SiC Interface for Passivation Studies**” Materials Science Forum, **600-603**, 763-6, 2009.
- VIII D. M. Martin, Ö. Vallin, I. Katardjiev and J. Olsson, “**Hydrophilic Wafer Bond Fabrication and Thermal Characterisation of new SOI Incorporating Buried Aluminium Nitride Insulator**”, manuscript, 2009.

# Description of my contribution

- I All of fabrication, analysis and writing with significant input from co-authors.
- II Took part in fabrication and involved in analysis and discussion.
- III Took part in fabrication and involved in analysis and discussion.
- IV All of fabrication, analysis and writing with significant input from co-authors.
- V All of fabrication, analysis and writing with shared modelling and significant input from co-authors.
- VI All of fabrication, analysis and writing with significant input from co-authors.
- VII Shared fabrication and film characterisation, involved in discussion and writing.
- VIII All of fabrication, analysis and writing with significant input from co-authors.

## Related Publications

- I D. M. Martin, Ö. Vallin, I. Katardjiev and J. Olsson, “Buried Aluminium Nitride Insulator for SOI Substrates”, 2007 EURO-SOI, 67-8, 2007.
- II D. M. Martin, Ö. Vallin, L. Vestling, I. Katardjiev and J. Olsson, “Improved Thermal Characteristics in SOI using a Buried Aluminium Nitride Insulator”, 2008 EUROSIOI, 97-8, 2008.
- III D. M. Martin, Ö. Vallin, I. Katardjiev and J. Olsson, “Buried Aluminum Nitride Insulator for Improving Thermal Conduction in SOI”, IEEE 2008 Int. SOI Conf. Proc., 105-6, 2008.
- IV Ö. Vallin, D. Martin, U. Smith, and J. Olsson, “Oxide free wafer bonding of silicon-on-silicon carbide substrates”, 2008 EUROSIOI, 95-6, 2008.
- V J. Olsson, Ö. Vallin, D. Martin, L. Vestling, U. Smith, and H. Norström, “Silicon-on-SiC hybrid substrate with improved high frequency and thermal performance”, 2008 EUROSIOI, 51-2, 2008.
- VI J. Olsson, Ö. Vallin, D. Martin, L. Vestling, U. Smith, and H. Norström, “Silicon-on-SiC hybrid substrate with low RF-losses and improved thermal performance”, 2008 GHz Symposium, 79, 2008.
- VII Ö. Vallin, D. M. Martin, J. Lu, L.-G. Li, U. Smith, H. Norström, and J. Olsson, “Thermal Characterization of Silicon-on-SiC Substrates”, IEEE 2008 Int. SOI Conf. Proc., 69-70, 2008.
- VIII D. M. Martin, J. Enlund, V. Yantchev, J. Olsson and I. Katardjiev, “Optimisation of a smooth multilayer Nickel Silicide surface for ALN growth”, 2008 J. Phys.: Conf. Ser., **100** 042014, 2008.
- IX D. M. Martin, J. Enlund, V. Yantchev, U. Smith, J. Olsson and I. Katardjiev, “Thick silicides synthesised with smooth surface for integrated TFBAR applications”, 2008 European Frequency and Time Forum, E1b03 – 110, 2008.
- X J. Enlund, I. Katardjiev and D. M. Martin, “Fabrication and Evaluation of an “Electrodeless” Solidly Mounted Thin Film Electroacoustic Resonator”, Proc. 2005 IEEE Ultrason. Symp., **3**, 1837-9, 2005.
- XI P. L  v  que, D. Martin, B. G. Svensson and A. Hall  n, “Defect Evolution in Proton-Irradiated 4H SiC Investigated by Deep Level Transient Spectroscopy”, Materials Science Forum, **433-436**, 415-8, 2003.

- XII D. M. Martin, H. Kortegaard Nielsen, P. L  v  que, and A. Hall  n, G. Alfieri and B. G. Svensson, “Bistable defect in mega-electron-volt proton implanted 4H silicon carbide”, Appl. Phys. Lett., **84** (10), 1704-6, 2004.
- XIII H. Kortegaard Nielsen, D. M. Martin, P. L  v  que, A. Hall  n, B. G. Svensson, “Annealing study of a bistable defect in proton-implanted n-type 4H-SiC”, Physica B, **340–342**, 743–7, 2003.
- XIV H. Kortegaard Nielsen, A. Hall  n, D. M. Martin, B. G. Svensson, “M-center in low-dose proton implanted 4H-SiC; bistability and change in emission rate”, Materials Science Forum, **483-485**, 497-500, 2005.
- XV T. Kubart, D. Depla, D. M. Martin, T. Nyberg and S. Berg, “High rate reactive magnetron sputter deposition of titanium oxide”, Appl. Phys. Lett., **92**, 221501-1-3 , 2008.
- XVI J. Jensen, R. Sanz, D. M. Martin, A. Surpi, T. Kubart, M. V  zquez, M. Hernandez-Velez, “Implantation of anatase thin film with 100 keV <sup>56</sup>Fe ions: damage formation and magnetic behaviour”, Accepted for publication in Nuclear Instruments and Methods in Physics Research Section B, 2009.

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# Abbreviations

AFM	Atomic Force Microscopy
BAW	Bulk Acoustic Wave
CMOS	Complementary Metal-Oxide Semiconductor
CMP	Chemical Mechanical Polishing
EA	Electro-Acoustic
FBAR	Thin Film Bulk Acoustic Resonator
FPAR	Thin Film Plate Acoustic Resonator
IC	Integrated Circuit
IDT	Inter-Digital Transducer
LFE	Lateral Field Excited
MOS	Metal-Oxide Semiconductor
SAW	Surface Acoustic Wave
SEM	Scanning Electron Microscopy
SMR	Solidly Mounted Resonator
SOI	Silicon On Insulator
SIMOX	Separation by IMplanted OXygen
TEM	Transmission Electron Microscopy
TEA	Thin Film Electro-acoustics
ToF-ERDA	Time of Flight-Elastic Recoil Detection Analysis
WLAN	Wireless Local Area Networks
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction



# 1 Introduction

It could be claimed that the origins of the electro-acoustic industry and devices started with a conjecture by Coulomb (1736-1806) that electricity might be produced by pressure. The origins could alternatively be found in the discovery of piezoelectricity by the Curie brothers (1880). Since then it was put to use in the detection of submarines (1914-1918) by Langevin, oscillator stabilization using quartz based crystal resonators (1921) and on through to Mason's invention of GT cut quartz (1940) [1]. Electro-acoustic devices have now been used for over 60 years in a number of applications such as delay lines, oscillators, resonators, sensors, actuators, dispersive delay lines, chemical and biochemical sensors, acoustic microscopy, specialized military equipment and the telecommunications industry.

The history of integrated circuits has the foundation of the field effect transistor (1926) with J. E. Lilienfeld, invention of a bipolar transistor (1947) at Bell laboratories and Kilby's integrated circuit in 1958. Since then there have been several advances in silicon and silicon dioxide technology enabling the fabrication of ever decreasing device size, faster operating speeds and device density. All of this following Moores law (1965) that the number of transistors on a chip will double every two years.

However, it is with the rapid increase in wireless and mobile communications that has led the research into thin film based electro-acoustic (TEA) resonators based on piezoelectric thin films. One of the materials of choice for this industry is piezoelectric aluminium nitride, which is fully compatible with IC fabrication. In a modern cleanroom facility both TEA and IC technology use many similar fabrication techniques. It therefore should be possible to transfer other as yet unused technologies from IC to provide solutions or alternative answers for the electro-acoustic industry. Allied to this is the technological limits of silicon and its oxide are now being reached makes research into alternative materials such as dielectrics of paramount importance. Thus it can be seen that both technologies have much to donate to each other and any further common uses of methodology increases the ability for their integration.

Therefore in this thesis, research has been based on area where technology can be transferred, such as using chemical mechanical polishing to solve cracking issues in acoustic devices and use of nickel silicide as an alternative electrode decreasing migration effects and replacing Al for high power applications. Improvements have been studied in resonator design for increas-

ing power handling abilities with the fabrication of an all metal Bragg reflector providing an efficient heat path through the metal mirror.

Alternatively material aspects and the transfer of AlN technology has been studied as an alternative high-k dielectric, a surface passivation layer for SiC based devices and as an alternative insulator layer to reduce self heating in SOI.

The research presented in this thesis has been conducted within the framework of the SSF (Swedish Foundation for Strategic Research) ICTEA project to to accomplish process and functional integration of the traditionally incompatible IC and electroacoustic (EA) technologies and also through the MS2E program in microelectronics.

## 2 AlN Material Properties and Applications

In this chapter some of the relevant properties and uses of AlN will be discussed. It will begin with basic electronic properties leading to its application as a piezoelectric material and the details of piezoelectricity. A short discussion on AlN's various uses in IC technology highlights some areas AlN could prove useful and enable integration with TEA technology (papers VI-VIII). There is a brief description of the deposition methods available and the method used here before a final description of the resonators fabricated and the excitation used (papers I-III and V).

### 2.1 Properties of AlN

Due to its unique properties, both electrically and acoustically, aluminium nitride (AlN) is an interesting material with many potential uses. As can be seen in table 1 it has a high resistivity making it a possible insulator material used for device passivation or combined with its dielectric constant it becomes a useful gate dielectric. The high bandgap energy also has uses in optical devices emitting the blue wavelength and potential uses in packaging due to its chemical stability, hardness and high thermal conductivity [2].

Table. 1 Wurtzite AlN properties [2-3].

Property		Value
Bandgap Energy	$E_g$ [eV]	6.2
Dielectric constant	$\epsilon_r$	8.2-8.9
Critical Field	$E_{cr}$ [MV/cm]	6-15
Resistivity	$\rho$ [ $\Omega$ cm]	$10^{13}$
Melting Point	$T_m$ [ $^{\circ}$ C]	2200
Thermal Conductivity	$\kappa$ [W/cmK]	2
Lattice const.	$a$ [ $\text{\AA}$ ]	3.112
	$c$ [ $\text{\AA}$ ]	4.982
Lattice		Hexagonal

It is however the change from quartz based resonators to thin film based where the unique properties of AlN have become a major advantage. The rapid advance of mobile and wireless data communications has placed exact-

ing requirements on components operating in the microwave region. Single crystal solutions in the gigahertz frequency range are becoming too bulky and costly and are incompatible to integrated circuit (IC) fabrication. Based on each material's unique properties, defining its acoustic velocity, the increase in frequency requires device dimensions to be reduced further and further. This in turn pushes up the fabrication costs of single crystal substrates higher. This makes the thin film electroacoustic (TEA) technology even more attractive. For TEA technology there has been substantial progress in recent years and it is now an established technology with millions of components manufactured annually. The electroacoustic technology is based on the energy transformation between acoustic to electric energy and back again. In TEA technology this transformation takes place in thin piezoelectric films such as AlN, ZnO and Lead Zirconate Titanate (PZT) of which only AlN is truly IC compatible.

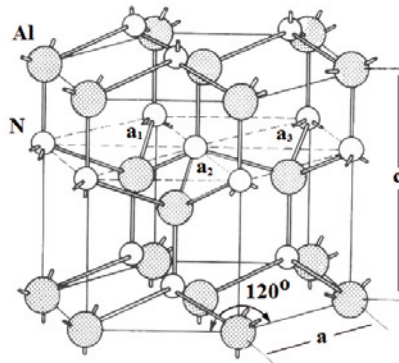


Figure 1. The wurtzite hexagonal phase of AlN with the growth shown in the c-axis orientation as used in this work.

## 2.2 Piezoelectricity

Another very important quality of the AlN is its piezoelectricity. The latter is represented by both the possibility for elastic deformation to proportionally induce electrical polarization as well as the possibility of applied electric field generating mechanical stress in a proportional manner. It is noted that strong piezoelectric effect is found in the wurtzite hexagonal phase of AlN seen in figure 1. In this lattice configuration the AlN is spontaneously polarized along its c-axis and the major piezoelectric effect is observed along this polarization axis. Simple understanding of the piezoelectricity can be reached through the model of the ionic CdS crystal. In a simplified consid-

eration the CdS can be considered as chain of negative (S) and positive (Cd) ions connected by springs (representing the elastic forces) (see figure 2).

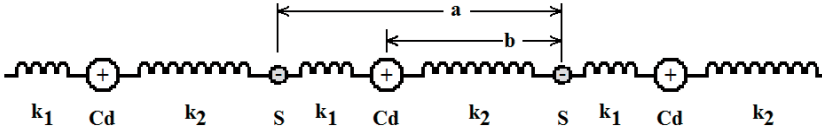


Figure 2. Schematic of a cadmium sulphide (CdS) ion crystal.

An important feature of this material is that the closest neighbours to a given ion are non symmetrically placed with respect to it. The latter is associated by the presence of spontaneous electric polarisation along the chain. If one period of the chain of atoms is considered the total dipole moment is

$$P = \frac{q}{2}(a - 2b) \neq 0 \quad (1)$$

where  $q$  is the charge of one electron,  $a$  the atomic spacing between S atoms and  $b$  the spacing between a Cd and S atom.

If external stress is applied to the chain, the deformation will cause change of the dipole moment, which in turn will determine a corresponding change in the polarization. Therefore the material equation for the electrical displacement along the polarization should be upgraded to:

$$D_z = \epsilon E_z + e S_{zz} \quad (2)$$

where  $D$  is the displacement,  $E$  the electric field,  $S$  the strain,  $\epsilon$  the dielectric constant and  $e$  the elastic constant. In a very similar manner, when external electric field is applied, the positive and negative ions in the chain will move in opposite directions and the overall deformation within a chain period will be nonzero due to the different rigidity of the springs. The latter is associated with mechanical stress generated by external electric field. Thus the material equation for the mechanical stresses should be upgraded to:

$$T_{zz} = c S_{zz} - e E_z \quad (3)$$

where  $c$  is the stiffness constant and  $T$  the stress. Equations (2) and (3) describe the piezoelectric effect in 1D form. Most generally, piezoelectricity is inherently related to the lack of centre of inversion (i.e non symmetrical order of the atoms).

This effect is therefore used to generate acoustic waves in the material and convert between electrical and acoustic energy. The ability of a material to perform this operation is governed by its elastic constants and mechanical stress and strain tensors which are themselves influenced by the symmetry of the unit cell. Therefore piezoelectric materials, which are anisotropic materials without a centre of symmetry, have the ability to couple electric field and atomic displacements with elastic stress and strain. Some of the acoustic properties of AlN are listed in table 2. The phase velocities for AlN are 5750 m/s for surface acoustic waves (SAW) [4] and 11350 m/s for bulk acoustic waves (BAW) [5].

Table 2. Acoustic properties of AlN used [6-7].

Material	AlN
$k_t^2$ (%)	6.0
$Z_f$ ( $\times 10^6$ ) [Nsm <sup>-3</sup> ]	35.9
$v_f$ ( $\times 10^3$ ) [m/s]	11.01
$\rho$ [kg/m <sup>3</sup> ]	3260
Temp. Coefficient [ppm/ <sup>o</sup> C]	-25

## 2.3 AlN for IC Applications

As previously mentioned AlN has a good dielectric constant making it one of a few interesting materials, others include Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, as a gate dielectric. The renewed interest in gate dielectric replacement is due to the ever decreasing device dimensions which now bring the natural oxide of Si, SiO<sub>2</sub>, down to its physical limits in thickness and thus current leakage. Typically SiO<sub>2</sub> has a dielectric constant of 3.9 compared to a measured AlN constant by Engelmark et. al. of 10 [8].

For semiconductor devices another important area is the passivation layer which is responsible for eliminating electrical shorts dissipating any charge build up and protecting against any chemical contamination. It has even been reported that passivation can help reduce electromigration [9]. Device reliability depends on the passivation material and thus the critical field ( $E_{cr}$ ) of the dielectric is an important parameter for these materials. Increased temperatures or damage by radiation effects can cause material degradation and thus decrease  $E_{cr}$  and increase leakage currents. Further device instability can be caused by injection or trapping of carriers into the dielectric. A large bandgap is also needed in the dielectric so that a large offset between either the valence or conduction bands, in a MOS structure, thus restricting tunneling between semiconductor and insulator. For Si based devices SiO<sub>2</sub> has a number of advantages but for III-V semiconductors, like SiC, improvement in reliability is needed. There are a number of advantages in using AlN such

as its superior crystallographic match to SiC, similar thermal expansion, high dielectric constant and an advantages deposition at room temperature [10]. Deposition of amorphous AlN would even have fewer columnar boundaries thus preventing further leakage through this mechanism. Due to the good crystallographic match and similar thermal conduction using an AlN passivation layer would bring an advantage of high temperature operation with less mechanical stress and higher resistance to cracking.

Table 3 Comparison of typical SOI material properties [2, 11-14].

Material	Bandgap [eV]	$\epsilon_r$	Critical Field $E_{cr}$ [MV/cm]	Thermal Conductivity [W/cmK]
c-Si	1.12	11.9	0.3	1.5
polysilicon				1.3-0.4
$\alpha$ -Si				0.018
SiO <sub>2</sub>	9	3.9	10	0.014
Al <sub>2</sub> O <sub>3</sub>	8.8	8	5	0.02-0.5
AlN	6.2	8.5/8.9	6-15	2

Finally AlN can be used as the replacement of the insulating box layer in silicon on insulator substrates, SOI. The current material, once again SiO<sub>2</sub> the natural oxide, suffers from poor thermal conduction. Thus device performance is degraded for power devices made on SOI substrates due to the self heating effects [15]. Even with the increased difficulties in fabrication, more complex and higher cost, the need for improved temperature performance makes AlN a very interesting choice as insulator in SOI. A comparison of material properties can be seen in table 3. The superior thermal conductivity can readily be seen for AlN in comparison to SiO<sub>2</sub> or even Al<sub>2</sub>O<sub>3</sub> [16], another common choice as replacement insulator, in fact it has a similar thermal conductivity to Si the substrate material.

## 2.4 Deposition of AlN

Table 4. Deposition Parameters for C-axis orientated AlN.

Target	Al (99.999%)
Substrate to target distance	55 mm
Base pressure	<5.10 <sup>-8</sup> mTorr
Process pressure	2 mTorr
DC power	1200 W
Ar gas flow rate	20 sccm (99.999%)
N <sub>2</sub> gas flow rate	40 sccm (99.999%)
Deposition rate	≈1 nm/s

Although there are several ways to deposit AlN such as chemical vapour deposition (CVD) [17] and molecular beam epitaxy (MBE) [18], the AlN fabricated in this thesis have been deposited using physical vapour deposition (PVD). The films have all been deposited using reactive sputtering at room temperature, which has been detailed elsewhere [10], and the details for thick crystalline AlN are shown in table 4. A typical 2  $\mu\text{m}$  film for electro-acoustic devices deposited onto Mo electrodes can be seen in figure 3a. The film quality is demonstrated by the good columnar structure and the good interface with Mo electrode is seen in figure 3b. The films deposited for passivation studies are made at a pressure of 10 mTorr and are 200 nm thick.

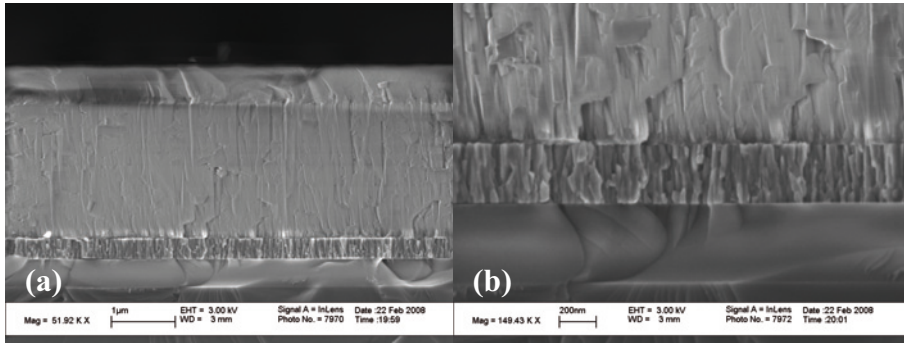


Figure 3. Cross-sectional SEM micrographs of (a) 2  $\mu\text{m}$  AlN film deposited at 2 mTorr and (b) close up of interface.

## 2.5 Types of Resonator Devices

The two main resonator device types in current usage are SAW and BAW, with the acoustic wave travelling along the surface of the piezoelectric along a waveguide or through the piezoelectric film thickness, respectively. In this thesis the thickness excited thin film bulk acoustic resonator is used (TFBAR).

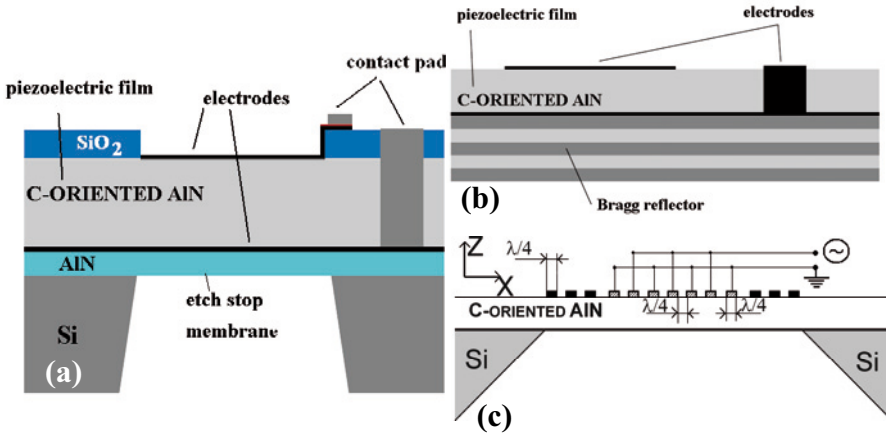


Figure 4. FBAR device schematic with (a) membrane type, (b) SMR type and (c) FPAR device schematic.

Two types of BAW resonator are the membrane type which is free standing and a solidly mounted resonator (SMR), shown in figure 4a and b, respectively. In both BAW resonators a piezoelectric material is sandwiched between two electrodes, in the former case an air gap is engineered either side through back etching of the substrate. This enables a high reflectance of the sound wave with air and gaining high Q values which is a measure of device quality. It is defined as the ratio between stored energy and dissipated energy for one cycle. In the topology here an extra etch stop layer is shown for protection of the electrodes during the Si substrate back etch. In the SMR type the membrane is acoustically isolated from but solidly mounted onto a substrate with a Bragg reflector [19] consisting of alternating pairs of, quarter wavelength thick, high and low acoustic impedance material. In figure 5b the transmission (c) and reflected (b) parts of the wave can be seen. The alternating pairs of high and low acoustic impedance material need to reflect back over 99.99% of the acoustic energy so that good quality factors can be achieved. This is still a decrease in Q from the membrane type of resonator but has the benefit of stability.

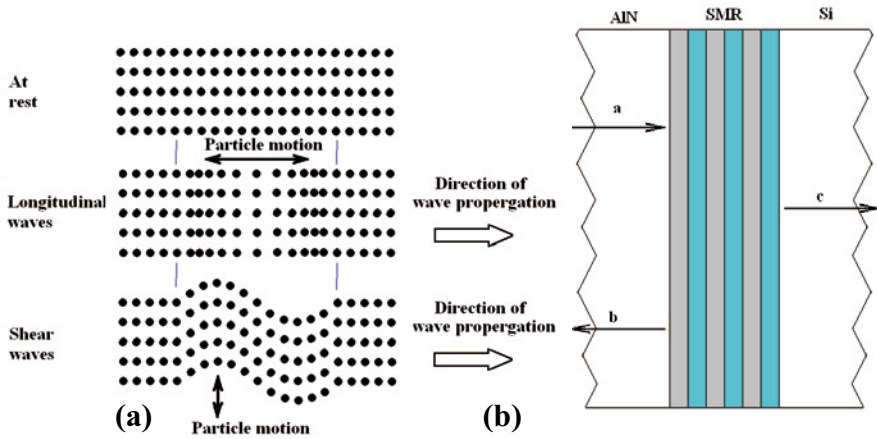


Figure 5. Schematic representation of: (a) wave motion and (b) transmission and reflection through a SMR stack.

For the thickness excited waves sound travels in either the longitudinal or shear mode, as seen in figure 5a. As discussed earlier distortions of the piezoelectric material, by an applied electric field, are acted upon by internal elastic forces restoring the system to equilibrium. Similar to a spring the elastic constant keeps restoring opposite to the distortion which combined with particle inertia brings about an oscillation. As seen in figure 5 the longitudinal wave has the wave propagation and particle oscillation in the same direction whilst shear modes have the distortion and hence particle motion perpendicular to wave propagation. An actual resonator fabricated using a membrane cavity is shown in figure 6a.

Another type of wave that can propagate in thin solid membranes is called the plate or Lamb wave and is used in thin film plate acoustic resonators (FPAR). FPAR's consist of an interdigital transducer (IDT) and a distributed Bragg type of reflector. The reflectors are formed by a quarter wavelength Al strips periodically placed on the top of the membrane surface, as shown in figure 4c. Here the IDT's can be seen in the centre lightly shaded and the reflector strips either side shaded black. A fabricated device is seen in figure 6b.

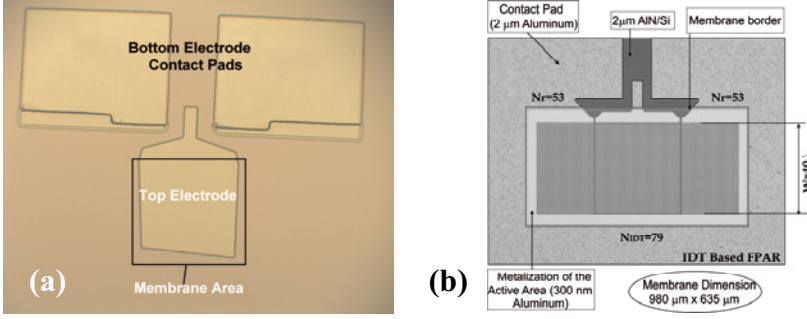


Figure 6. Actual fabricated devices: (a) FBAR membrane with  $300 \times 300 \mu\text{m}^2$  area and (b) FPAR.

Plate waves are lateral waves that propagate in plates of finite thickness. The number of waves, at a given frequency, that can be supported depends on the ratio of the film thickness ( $d$ ) and wavelength ( $\lambda$ ),  $d/\lambda$ . The waves are either symmetrical or asymmetrical which defines the symmetry with respect to the median plane of the plate and therefore the deformation, as seen in figure 7 [20].

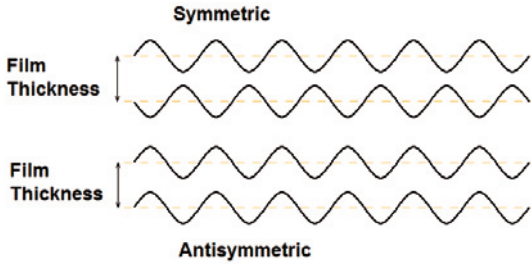


Figure 7. Representation of the symmetric and antisymmetric modes of Lamb waves.

For thin plate waves, as used in paper I with a ratio of  $0.167\lambda$ , only the lowest order symmetric  $S_0$  and asymmetric  $A_0$  modes are observed, at frequencies less than the fundamental bulk resonance. In AlN the  $S_0$  mode has a velocity greater than 9800 m/s and the  $A_0$  mode has a greatly reduced velocity of 1840 m/s [21]. The high velocity exhibited by the  $S_0$  mode makes it an attractive proposition for microwave components.



## 3 Characterisation Techniques

There are many different methods for characterising materials that can be used to investigate its texture, composition and surface. In this thesis some of the main investigative techniques are detailed here.

### 3.1 X-Ray Diffraction

One of the characterisation techniques used in this thesis is x-ray diffraction (XRD) [22]. This method is used here principally to determine the degree of crystallinity or preferred orientation of the deposited AlN films using rocking curve measurements and  $\theta$ - $2\theta$  scans, respectively. It also has been used to discover the phase of silicides by analysis of  $\theta$ - $2\theta$  peaks present and even to discover whether any form of re-crystallisation has taken place in Si, both using  $\theta$ - $2\theta$ . Using the grazing incidence set up helps to determine the initial stages of crystallisation and by control of the grazing angle, therefore penetration depth into the film, whether any re-crystallisation is at the interface or surface. This method also has the advantage of being a non destructive technique.

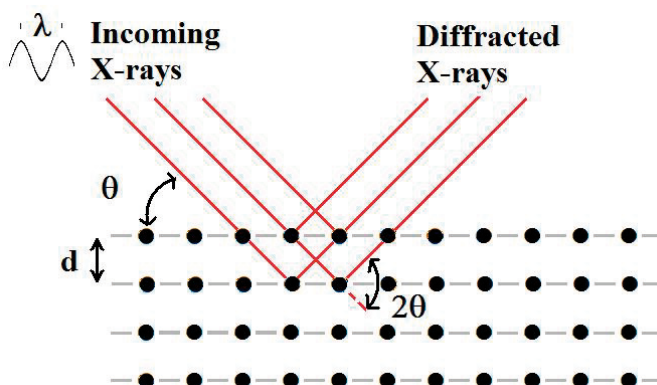


Figure 8. Schematic representation of diffraction in an atomic lattice.

The technique is based on information on the probed material structure provided by constructive and destructive interference of an incoming X-ray

beam reflected of the materials structure. This can be seen in figure 8 where each atom in the periodic structure scatters the incoming wave as described by Braggs law

$$n\lambda = 2d \sin \theta \quad (4)$$

where  $n$  is an integer,  $\lambda$  the wavelength of x-rays ( $1.54\text{\AA}$  from the Cu  $K\alpha$  source used here),  $d$  the distance between atomic planes and  $\theta$  the angle between the crystalline surface and incident beam. Therefore constructive interference is achieved when distance travelled through the sample,  $2d\sin\theta$ , is equal to the wavelength multiplied by an integer and for all other angles results in destructive interference. As well as crystal structure mentioned previously the XRD technique can also be used to ascertain other material parameters such as grain size, lattice dimensions and stress induced in the film during growth.

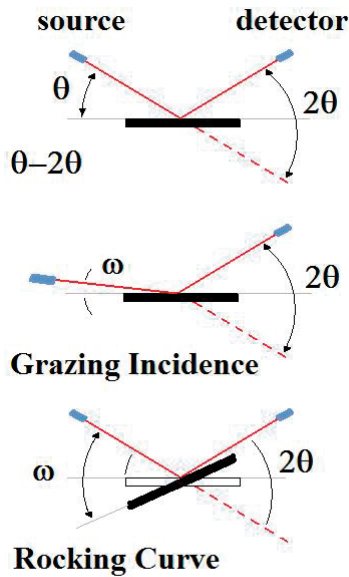


Figure 9. The positional movement of X-ray geometries for various XRD scans.

There are three main XRD scans used during this work,  $\theta$ - $2\theta$ , grazing incidence (GI) and  $\omega$  scans, which can be seen in figure 9. The first is  $\theta$ - $2\theta$  which has been used to establish preferred orientation of the materials. Establishing which planes are present in a film also gives information on the films phase, an example of which is seen in figure 10, where the change in phase between  $\text{Ni}_2\text{Si}$  and  $\text{NiSi}$  is seen for different annealing temperatures. Here the source and detector are coupled so that  $\theta$  and  $2\theta$  are varied in tan-

dem for an interval of interest with constructive interference, hence signal, at angles which fulfil the Bragg condition.

The second type of scan is grazing incidence which results in a scan similar to the  $\theta$ - $2\theta$ . However, here as the incident and reflected waves are no longer coupled and strong crystalline planes will not generate a signal in the spectrum. Thus any influence from either single a crystalline substrate or strong orientations in the deposited film will be masked and only signals generated from weak crystal planes will be seen in the diffractogram. Generally the incident angle penetrates a few  $\mu\text{m}$  into the sample but the low angle of incidence here probes only a few hundred nm of the sample surface, using angles between  $0.5$  to  $5^\circ$ . This method also probes a larger surface area however the signals are still weak due to only reflections from weak crystalline planes being picked up and thus tend to be noisy. In this method the incident angle is held constant whilst  $2\theta$  is swept through the desired range.

The final method shown in figure 9 is the rocking curve ( $\omega$  curve) measurement. In this instance both the  $\theta$  and  $2\theta$  angles are locked to a specified plane, generally in this thesis that of AlN (002), and the sample is rocked about the axis of incidence. The full width at half maximum (FWHM) of the resultant peak indicates the orientation quality of the film.

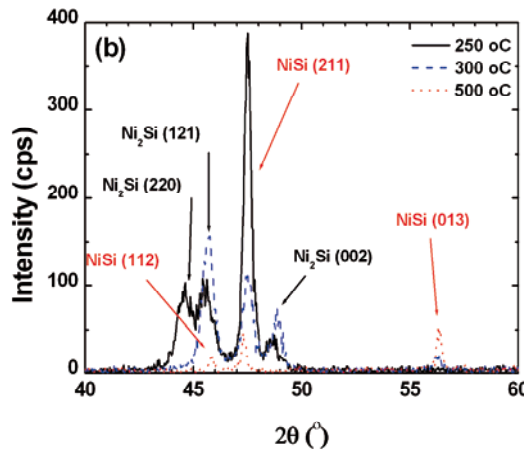


Figure 10. Diffractograms from three nickel silicide films for RTA temperatures showing the transition between the first two silicide phases,  $\text{Ni}_2\text{Si}$  and  $\text{NiSi}$ , as well as at the optimised temperature.

## 3.2 Atomic Force Microscopy

The basic principle of atomic force microscopy (AFM) is a sharp tip, around 10 nm, is scanned over a sample surface and deflected by any surface irregularities, contact AFM. The tip is held on the end of a spring loaded cantilever and deflections in the tip are translated into a signal by a laser reflection from the tip into a detector. Another method called either tapping or non-contact mode scans very close to a sample surface and uses atomic forces. Here the atoms of the tip and sample are separated and when spaced wide apart the atoms attract, due to van der Waals force, and when brought too close together they repel, due to electrostatic repulsive forces. The deflection in the tip is again detected via a laser and translated into an image of the sample surface as seen in figure 11. There are several interesting uses for this method such as the root mean square (rms) of the surface roughness, interesting facets seen in sample surface, such as the pits seen in figure 11, and even steps in surface created by masking and implantation or etching.

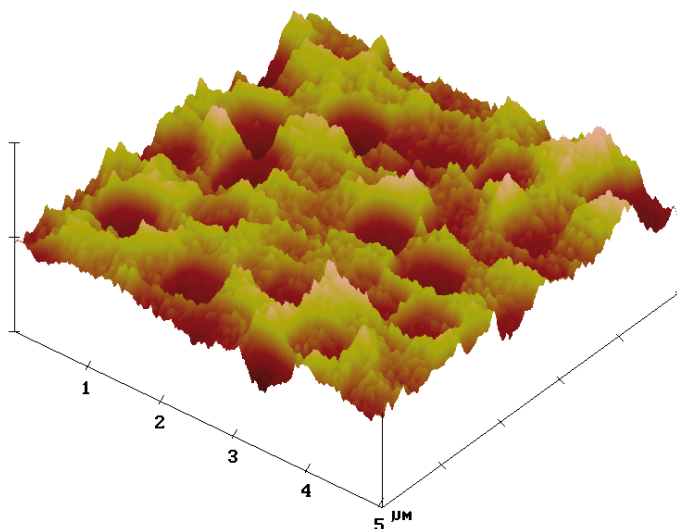


Figure 11. AFM micrograph of Simgui SIMOX device layer surface,  $Z = 10$  nm/division, the rms here is 1.3 nm.

The rms value is a measure of the surface roughness which may have a detrimental effect on the texture of AlN, and smooth surfaces of less than 1 nm rms are needed for strong bonds in the case of wafer bonding. The roughness of the surface shown is believed to be due to the fabrication technique of SIMOX (separation by implantation of oxygen) silicon on insulator (SOI)

substrates. It is interesting to note that this wafer was bonded successfully to a very smooth surface where the rough pits were seen as being beneficial.

### 3.3 X-ray Photoelectron Spectroscopy

A surface analytical technique based on the photoelectric effect is X-ray photoelectron spectroscopy (XPS) and is used to study the chemical composition of around 30Å deep into a sample surface [23]. It is also referred to as electron spectroscopy for chemical analysis (ESCA). As can be seen in figure 12a an incident x-ray beam strikes the sample at an angle and a photoelectron is ejected, figure 12b. The emitted electrons are collected in a hemispherical energy analyser and the detected energies relate to the chemical composition of the sample, figure 12a. This is seen in equation 5 where the energy required to remove an electron is subtracted from the initial energy of the incident photon. The energy required to remove the electron is made of the binding energy to its orbital and the work function to leave the surface, thus limiting the sample depth.

$$E_{Kinetic} = h\nu - E_i - \Phi \quad (5)$$

where  $E_{kinetic}$  is the kinetic energy of the ejected photoelectron,  $h\nu$  the energy of incident photon,  $E_i$  the binding energy of electron orbital and  $\phi$  the surface work function.

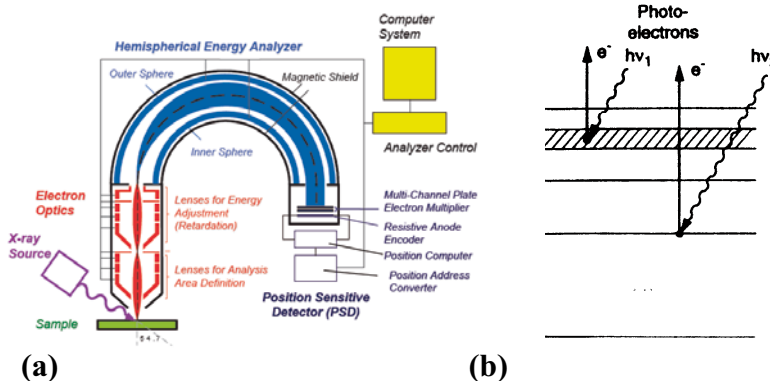


Figure 12. Schematic of (a) a XPS system [24] and (b) the principle of XPS [25].

Not only can the atomic composition of a sample can be determined but also the chemical bonding of atoms. This is due to chemical shifts in the binding energy between different atomic bonds, for example Al bonded to oxygen

results in a positive shift of the binding energy. The sample depth that is probed can also be a problem for one of two reasons. Firstly any variation within the 30 Å depth will not be resolvable and will be analysed as one region and secondly this will not investigate the bulk composition of a film. In the near surface region greater resolution can be achieved by varying the incident beam so that at low angles of incidence only the surface is analysed. However this can still be difficult to interpret as the higher incident angles also include signal from the surface region. For investigation of bulk composition most XPS equipment includes an ion gun for sputtering of the sample material between XPS spectrum scans. Several cycles of the sputtering can be performed with scans performed in between so that a sputter profile of the sample concentration can be extracted. The profile however is still a sputter time depth profile and not thickness and the results can be affected by preferential sputtering of lighter atoms. Additionally there are energy dependencies to each spectrometer which may need to be accounted for by reference samples with a known composition and calculation of a set of sensitivity factors for individual XPS equipment and sample composition. Care also needs to be taken with charging effects shifting peaks to higher binding energies or if a flood gun is used for neutralisation then over neutralisation can shift to lower binding energies. Further analysis of these areas can be seen in ref 26 and 27.

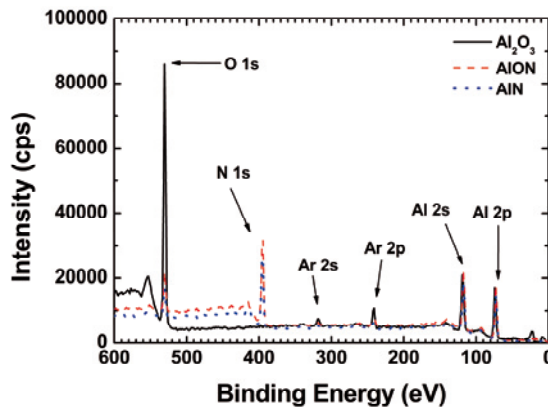


Figure 13. XPS depth profiling spectra of binding energy region between 600 and 0 eV for three different sample compositions,  $\text{Al}_2\text{O}_3$ , AlON with 10 % oxygen and AlN with 8% oxygen.

In the general case XPS has been used to determine whether any contamination, such as oxygen, has been incorporated into an AlN film during deposition or subsequent fabrication steps. Any contamination incorporated into

the AlN piezoelectric will decrease the quality of the film texture and its electromechanical coupling. The detection limit of XPS is 0.5 % which is enough for oxygen contamination to detrimentally affect AlN films. Care must be taken with analysis of oxygen as the initial surface will have high levels of oxygen content and directly after sputtering with an ion gun the surface will re-oxidise so any elemental scan of oxygen should be conducted first to obtain an accurate stoichiometry profile. After sample loading into the XPS system a sufficient period must be allowed to elapse for the extraction of any contaminating oxygen obtained during the loading process. Paper VI has a detailed analysis of XPS examination of oxygen contaminated AlN films and conversion to a depth scale in nm. An example of film analysis for passivation studies of amorphous ALN films, paper VII, is seen in figure 13. Here a scan of the spectrum between 600 eV and 0 eV is shown, a concentration profile was obtained through elemental scans completed prior to the full spectrum therefore the oxygen signal here is likely to be slightly increased. However it is clearly seen that the  $\text{Al}_2\text{O}_3$  consists only of Al and O with no contamination, the Ar incorporation is due to the ion gun species used for sputtering. For the other two samples the elements Al, O and N can be resolved.

### 3.4 Time of Flight – Elastic Recoil Detection Analysis

An alternative method used for elemental composition studies of thin films is time of flight – elastic recoil detection analysis (ToF-ERDA) [28]. The standard operating conditions used for film analysis here was a 40 MeV  $^{127}\text{I}^{9+}$  ion beam, which enabled the detection of light elements such as hydrogen. The incoming ion beam and outgoing recoils impinged/exited at  $67.5^\circ$  ( $\theta_1$  and  $\theta_2$  respectively) to the sample surface normal, respectively, giving a recoil angle of  $45^\circ$  ( $\phi$ ), see figure 15. A detailed description of the experimental set-up has been given elsewhere [29-30]. In this method the incident heavy ion knocks the target atom which elastically recoils and is then detected. The time-of-flight (ToF) and the energy signals for each recoil are recorded and the recoil energy of each element then converted to elemental depth profiles. The process starts with a conversion of the time versus energy spectra, see figure 16, into mass versus energy channel and then concentration versus energy channel using the CONTES code (conversion of time–energy spectra) [31]. Mass and energy calibration was established by measurements of reference samples and following the procedure reported by El Bouanani et al. [32]. Conversion of the recoil energy spectra to elemental depth profiles was based on SRIM2006 code [33]. The detection efficiencies for the different recoil species were established from standards by scaling to the electronic stopping power for the recoil isotopes according to Zhang et al. [30].

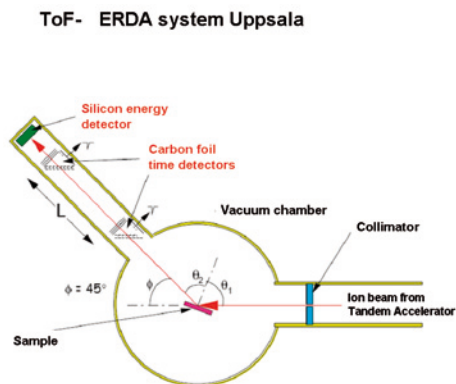


Figure 15. Schematic of the ToF-ERDA system at Uppsala University.

The advantages of the method is the simultaneous measurement of all elemental profiles, detectability of light elements on heavy substrates and most importantly the ability to detect trace elements. An example of identifying both a trace element and a light element is the detection of hydrogen seen in figure 16. The concentration of hydrogen here is below 1 %.

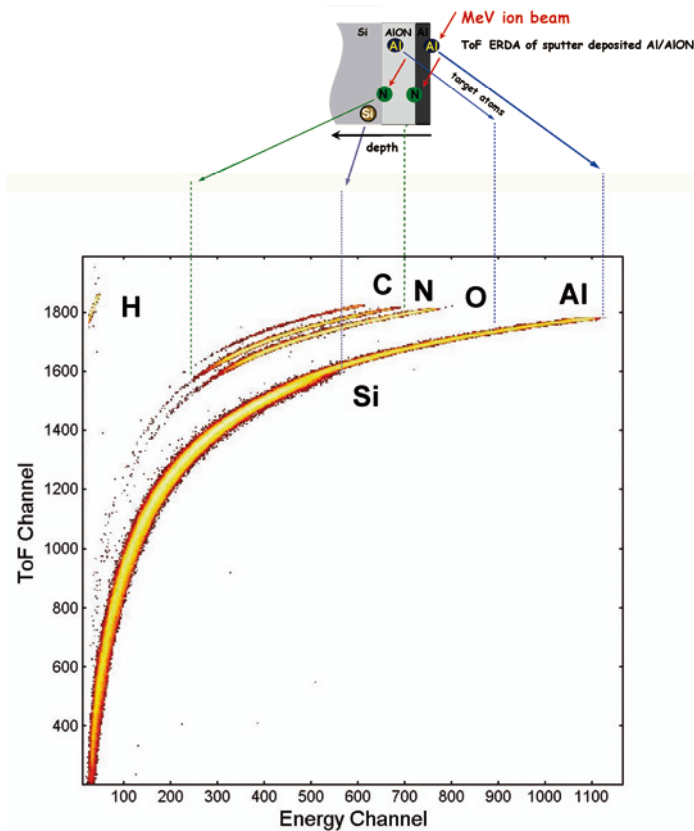


Figure 16. Scatter-plot (time v's energy) for AlON sample, from paper VI. Hydrogen and carbon contamination are clearly seen.

It can be readily seen from figure 16 that the detected elements from the surface are easily discernable from those detected in the bulk.



## 4 IC Fabrication Technology

In this chapter some description is given for the IC technology that is used to solve issues in resonator fabrication (papers I and IV-V). The last two sections outline an area where AlN could be used for fabricating an alternative substrate for reduction in self heating effects of high power devices and the wafer bonding method used to create these substrates (paper VIII).

### 4.1 Chemical Mechanical Polishing

Chemical mechanical polishing (CMP) has grown rapidly and been used in the semiconductor industry since its invention in 1984 [34], particularly after the development of copper metallization in very large scale integration (VLSI). The advantages of planarization technology are the elimination of step coverage between interconnect levels in VLSI technology [35] via dielectric planarization or recessed metal planarization [36-37]. Tungsten CMP is a well-researched and established process in this industry [37-38].

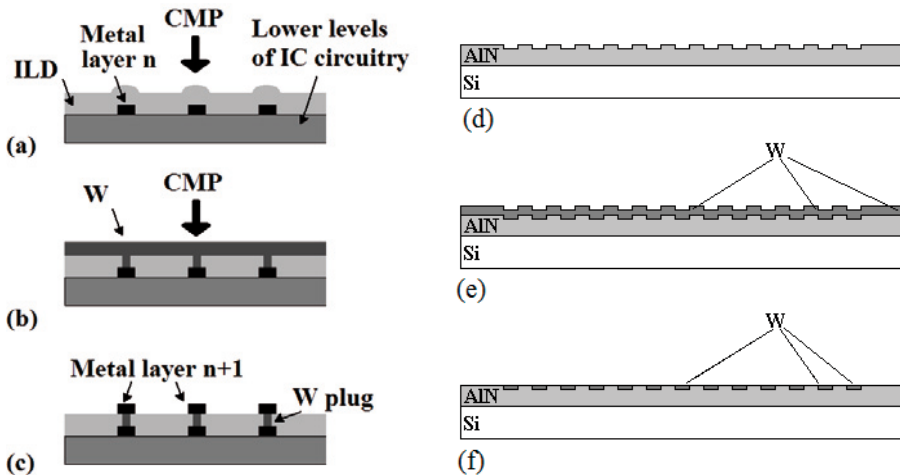


Figure 17. Process flow for: (a-c) Al wiring between interconnect levels using tungsten plugs creating buried electrodes and (d-f) buried W electrodes.

The general process flow for creating interconnect levels in IC processing is shown in figure 17. A metal layer is defined on top of the lower IC circuitry to be connected and then covered with an interlayer dielectric (ILD). This surface is then planarized using CMP, figure 17a. Masking and etching is used to create openings for W plugs which are subsequently filled, figure 17b, and then polished once more down to the dielectric surface. The result is seen in figure 17c where the next metal layer can be defined on top of the plug creating an interconnect between the IC levels. A similar process has been developed in this work to create buried electrodes as seen in figure 17d-e. Here the interdigital transducer (IDT) openings are first created in the AlN piezoelectric, 300 nm deep trenches in a 2  $\mu\text{m}$  thick AlN film. The W or Mo is then deposited filling the trenches and covering the AlN surface, figure 17e. The CMP is then performed on this surface resulting in IDT's buried in the piezoelectric surface, figure 17f.

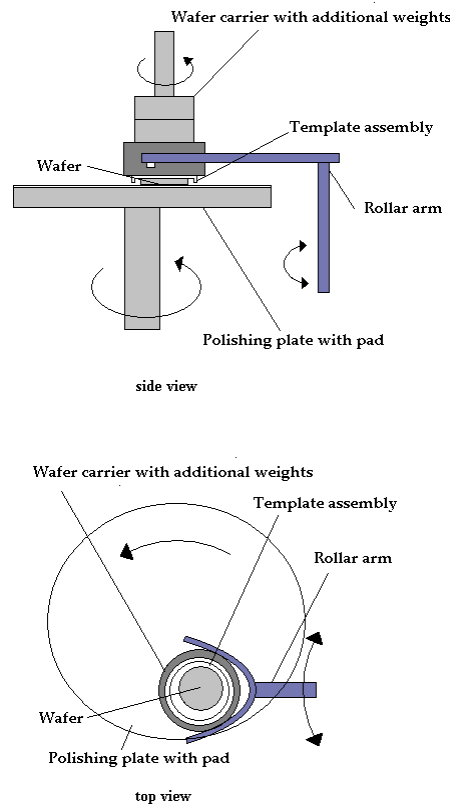


Figure 18. Schematic of CMP equipment.

The CMP is achieved using a bench top PM4 precision lapping and polishing machine, from Logitech Ltd. The general features of the equipment can be seen in figure 18. A polishing pad is mounted on a 30 cm diameter polishing plate. The wafer is mounted on a template assembly which holds the wafer by capillary effect and this in turn is mounted via adhesive on the back to the carrier assembly. The template assembly consists of a polymer material upon which the wafer rests and the template holds the wafer in place. The wafer carrier is placed, with wafer facing down towards polishing pad, inside the supports of the roller arm on the polishing pad. When the polishing plate rotates the wafer carrier adopts the same rotation as the plate. The roller arm can sweep the wafer carrier across the plate for more uniform pad wear. Pressure is applied by adding weights to the wafer carrier and the polishing slurry is supplied directly to the polishing pad which is in contact with the wafer surface. The removal of material, namely W or Mo, is a combination of mechanical abrasion and chemical etching. After polishing the wafer is cleansed/buffered on the same pad whilst being rinsed with DI water. The wafer is then transferred in DI water to an ultrasonic acetone bath where any residual particles are washed away.

## 4.2 Silicides

Silicides are a metallisation common to IC fabrication and a major building block in very-large-scale integration (VLSI) is the MOS field effect transistor. Here, silicides have been used for self-aligned metallization in contacts to source, drain and on polysilicon gates. In the early 1960's PtSi was first used to improve the rectifying characteristics of diodes [39]. There are a number of silicides used in IC process, the most common being  $\text{TiSi}_2$ ,  $\text{CoSi}_2$  and  $\text{NiSi}$ . Presently,  $\text{NiSi}$  is considered the most versatile silicide for all six electrode areas in complementary MOS (CMOS) technology [39]. It has several advantages, such as a low resistivity of  $10 \mu\Omega \text{ cm}$  even on very narrow polysilicon lines, minimum silicon consumption and a low formation temperature of 300 to 400°C. Fabrication of  $\text{NiSi}$  also has the advantage of a large temperature formation window. The low-resistivity  $\text{NiSi}$  phase is stable up to 700°C and formation can be accomplished in a single step. It is a chemically and oxidation stable material and is immune to electromigration [39].

In this work the  $\text{NiSi}$  technology is transferred and used as an electrode material for use in acoustic applications. The relatively low acoustic impedance of  $\text{NiSi}$  make it especially interesting in view of replacement of the lossy low impedance Al electrodes in high power applications. Reliability of Al is degraded by spiking in the Si substrate [40] as well as electromigration [40] and acoustomigration, which leads to hillocks and voids in the Al film [41].

However certain requirements not previously met had to be investigated and solutions found. These problems centred on the thickness required for electrodes in acoustic applications being in excess of a few hundred nm whilst in IC applications the average requirement is in the order of 10 nm. For use in FBAR resonators the Si from the substrate may not be available and smooth surfaces would be needed for subsequent depositions of piezoelectric material.

In IC components a metal layer is deposited onto Si then transformed into the required silicide phase by rapid thermal annealing (RTA) where the metal and silicide diffuse together into the required phase determined by the temperature and time. Due to the thickness and roughness constraints for acoustic applications a unique synthesis has been developed and is based on a multilayer approach [42-43]. The fabrication of thick NiSi electrodes consisted of alternately sputter depositing Ni and Si layers without breaking vacuum. Each material was deposited with a specific sub-layer thickness to a total as deposited thickness over 400 nm, as seen in figure 19. The thickness ratio of deposited Si to Ni required to produce stoichiometric NiSi was 2:1. The required silicide thickness can be calculated using the fact that 1 nm Ni produces a NiSi thickness of 2.22 nm, while consuming 1.84 nm Si in the process [44-45]. The deposited multilayer stack is annealed at 500°C for 30 seconds with rapid thermal processing (RTP) to form a thick stoichiometric NiSi layer.

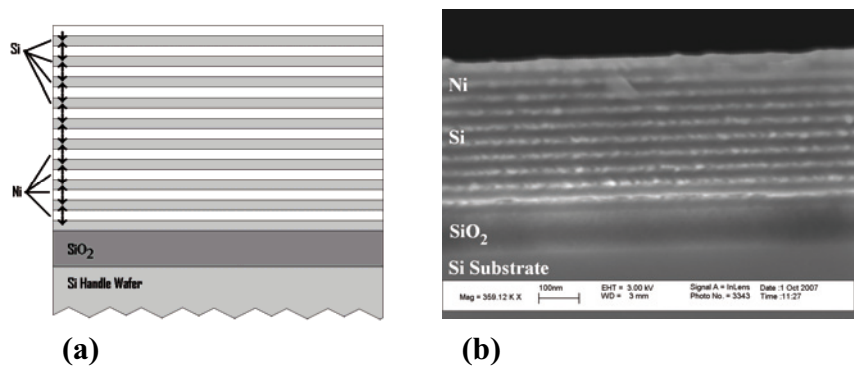


Figure 19. (a) Schematic and (b) SEM micrograph of 10 pairs of alternately as-deposited Ni and Si layers, light and dark respectively. The flow of the dominant diffusing species is indicated by the arrows.

### 4.3 Silicon On Insulator

Almost all CMOS fabrication is made on bulk silicon wafers thanks to the abundance of electronic grade substrates and the quality of the natural oxide. However the interactions of devices, namely drain source or gate regions, with the substrate and the parasitic effects this produces are becoming problematic. There are some tricks used such as epitaxial wafers or deep trench isolation but these bring more complex fabrication issues thus increasing costs and lowering manufacturing yield. Tie this in to the continuous reduction in device size, requirements for faster devices, low power consumption demands and increase in device density alternative solutions become necessary.

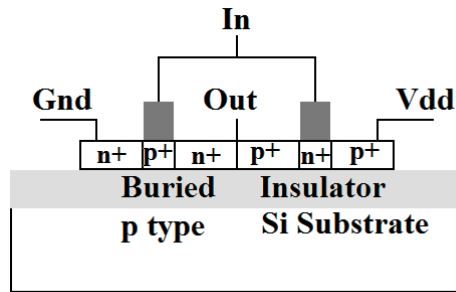


Figure 20. Schematic diagram of a CMOS inverter fabricated on SOI.

One alternative is to fabricate devices on SOI which then provides a full dielectric isolation of device and prevents most parasitic effects [46]. This can clearly be seen in figure 20, where the dielectric layer shields the device from most parasitic effects which would otherwise short through the substrate or create parasitic capacitances and it can be seen that device isolation becomes simpler. The reduction in leakage currents also enables operation at higher temperatures than bulk devices [47]. Other advantages of devices fabricated on SOI are faster switching speeds, lower power consumption and decreased chip heating compared to bulk Si devices.

The SOI substrates consist of a thin silicon device layer on top of a  $\text{SiO}_2$  insulating layer fabricated on thick silicon substrates. There are three fabrication methods currently in production. One method is the separation by implanted oxygen (SIMOX) using high doses of oxygen implanted with high energy into bulk silicon and then thermally annealing [48]. The next is created using the bonding of one silicon wafer to another silicon wafer, which is also covered with an oxide layer, then bond strength annealing and finally

thinning the backside of one wafer to the device layer thickness. This type is referred to as bond and etch back SOI (BESOI) [48]. More recently a method called smart cut has started fabrication. Here a hydrogen layer is implanted into an oxidised wafer and then bonded to another oxidised wafer. A low thermal treatment fractures the wafers apart where the hydrogen layer is buried, followed by a high temperature annealing and finally polishing of the device layer Si [49]. The later type of substrate now dominates the market and is available in large wafer sizes.

There are however, some disadvantages with these substrates, mentioned briefly in chapter 2, and these centre around the low thermal conductivity of  $\text{SiO}_2$ . It has a thermal conductivity of  $0.014 \text{ W/cmK}$  which is 100 times less than Si. Therefore during operation the device is unable to conduct the heat away from the active area adequately, causing the device temperature to rise and limiting device performance. This effect is called self heating and the effects on even simple MOS structures can be observed in figure 21 [50]. For the SOI substrate, open squares, at higher drain voltages the saturated current is seen to decrease. This behaviour is directly related to the self heating effects of the buried silicon oxide in the SOI substrate. It can also be seen that this effect is less apparent for epi substrates.

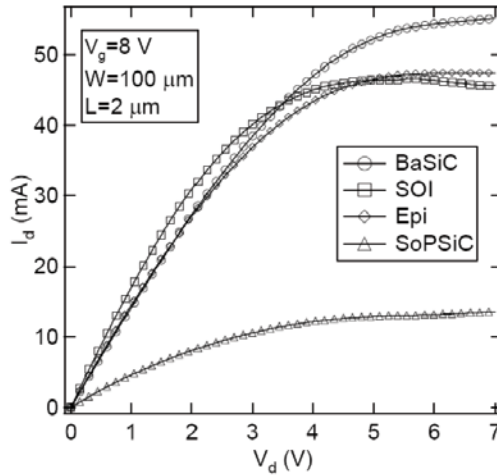


Figure 21.  $I_d$ - $V_d$  at high voltages.  $I_{d,sat}$  (SOI) drops due to self heating effects.

Self heating of buried silicon dioxide can also be seen in figure 22 where 2D simulations of thermal resistors created in the device layer of Si on two types of SOI. Thermal resistors consist of a conducting Si finger, formed on the insulator surface, which has a high current pushed through it whilst measuring the voltage drop over resistor. The measured resistance is then compared to a calibration where device was externally heated and current voltage char-

acteristics measured. From this the rise in temperature due to high current flow can be calculated.

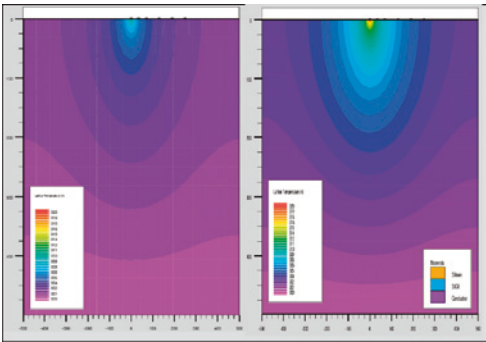


Figure 22. 2D simulations of temperature distribution for a 20°C temperature increase on (a) SOI with SiO<sub>2</sub> and (b) SOI with AlN. Scale from red to purple is 320 to 300 K respectively.

This process is modelled in a simulation and in the figure to the left, where a traditional SiO<sub>2</sub> insulator is used, the temperature rise is held very close to the thermal resistor.

The latest idea is to fabricate alternative SOI using insulating layers which are more thermally conductive. One alternative is AlN which combines the advantages of a thermal conductivity of 2 W/cm which is close to Si, and is compatible to IC facilities.

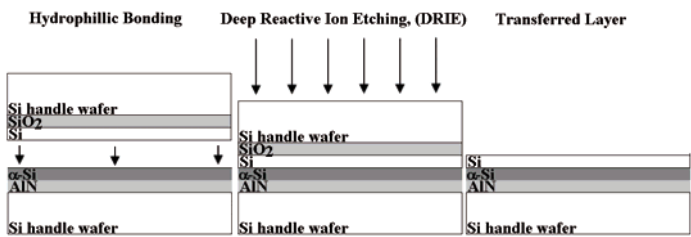


Figure 23. Process schematic for transfer of device layer.

In this thesis, see paper VIII, silicon on aluminium nitride SOI is created as shown by the process flow in figure 23. The buried AlN is prepared by sputter deposition onto a silicon handle wafer and then deposited with an amor-

phous Si layer without breaking vacuum. The surface is then hydrophillically prepared along with a commercial SIMOX substrate. The two surfaces are brought into contact together where spontaneous bonding occurs, assist by the smooth amorphous Si layer. Deep reactive ion etching is then used on the backside of the SOI substrate until the buried oxide is exposed. The oxide layer is etched in hydrofluoric acid leaving the transferred Si device layer on top of a buried AlN insulator.

Modelling of this SOI structure can be seen in figure 22, right hand image. Here the improved thermal conductivity is demonstrated by the increased flow of temperature away from the device and further into the substrate.

## 4.4 Wafer Bonding

Another process technique used in IC fabrication is wafer bonding which can be performed with or without an intermediate layer. The interlayers that are used can be either conducting or insulating and this type of bonding can be used for the bonding of non-flat surfaces. For bonding without interlayers anodic bonding can be used, however it requires the substrates to be clamped between two metal electrodes with high voltages of up to 1 kV. One of the substrates used is a glass containing sodium ions which are displaced by the electric field at temperatures of 400°C away from the bond interface. This glass surface is highly reactive with the other Si surface creating a strong chemical bond. Direct wafer bonding is the method used in this thesis and is used for the fabrication of advanced substrates such as silicon on glass, silicon on sapphire and strained silicon on insulator. Other advantages of this method is different materials can be bonded, the stacking of many processed layers is helped, encapsulation and even for creating microfluidic channels. Direct bonding is also used in MEMS fabrication where the oxide layer can be used as the sacrificial layer releasing the membranes. Surface preparation can be achieved chemically, by plasma activation or even by CMP. The disadvantage with this method is that flat clean and smooth surfaces are needed but the result is a spontaneous bond that does not require any external forces. When the two prepared surfaces are brought together a weak bond is formed by van der Waals forces, capillary forces or electrostatic forces [51]. The weak bond is then strengthened by thermal annealing, generally at 1000°C. Direct bonding uses surfaces that are made either hydrophilic which usually require oxide surfaces or hydrophobic which are generally silicon.

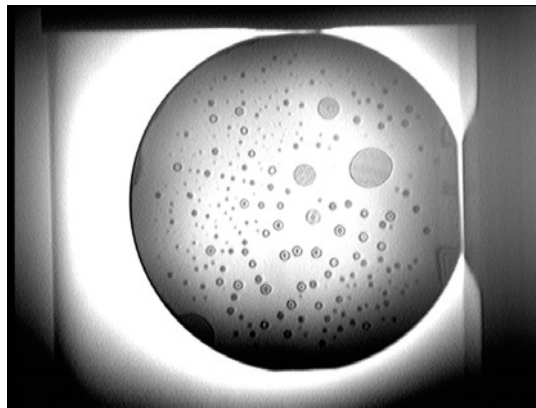


Figure 24. Infrared transmission photograph of hydrophobic bonding of two Si surfaces after bond strength annealing at 1000°C.

Hydrophobic surfaces have no affinity for water and can be chemically prepared using hydrofluoric acid chemical pre-treatment which etches the natural  $\text{SiO}_2$ . This leaves a hydrogen or fluorine terminated surface which needs to be bond immediately after treatment before the surface becomes contaminated by hydrocarbons which form interface bubbles upon annealing [52-53]. Voids formed after annealing hydrophobic prepared surfaces can be seen in figure 24. The bonding here is initially through HF molecules between the Si surfaces which then desorbs during annealing leaving a Si-Si bond.

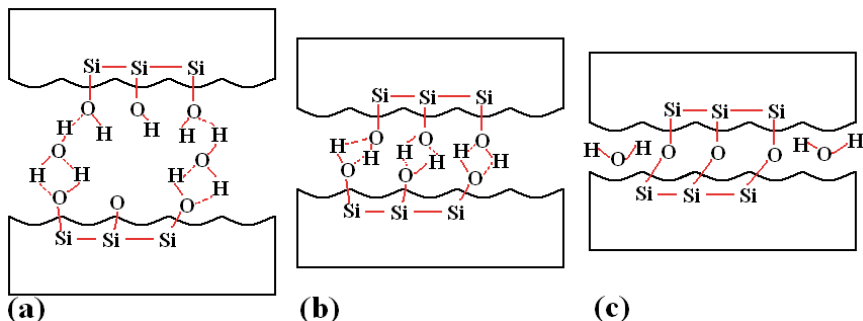


Figure 25. Hydrophilic bonding process schematic: (a) initial water bonding, (b) bonding through van der Waals and finally (c) Si-O-Si bonding.

As mentioned previously, there can be issues relating to hydrogen contamination and interface bubble formation. In this work hydrophobic bonding has been used which has a strong affinity for water which is enhanced by surface pre-treatment of  $\text{HNO}_3$  increasing the Si-OH groups. The bonding process can be seen in figure 25. Initial contact is formed through water molecules (a), during annealing the water molecules diffuse away from the interface, dissolve into the surrounding surfaces or form new hydroxyl bonds (b). Eventually excess hydrogen and water is forms water molecules leaving Si-O-Si bonds which forms a thin oxide layer, (c). When one surface is covered in oxide the water molecules and any excess hydrogen can be absorbed into this layer, otherwise voids can be created by the trapped gases. This can be avoided via channels leaving escape routes for trapped gases created via one roughened surface [54] or channels etched into one surface [55]. This is discussed in paper VIII. A high resolution transmission electron microscope (HRTEM) image of the thin oxide layer formed between two Si surfaces can be seen in figure 26. Here it is believed that the oxide emanates from the hydrophilic treatment prior to bonding [56]. If one of the bonding wafers is covered in oxide prior to bonding, to absorb the trapped gases, then it has been demonstrated that it is possible to diffuse out a silicon dioxide layer situated between two silicon layers [57-58].

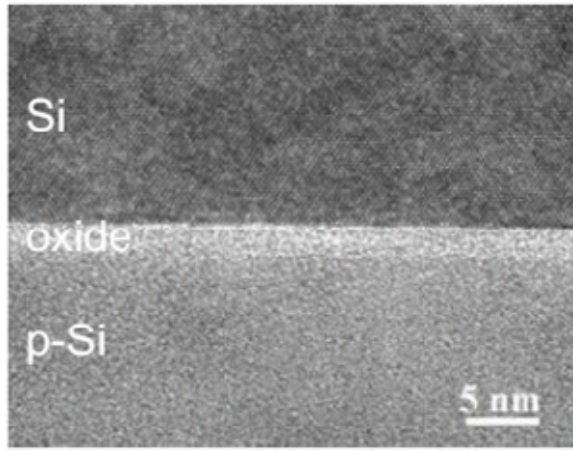


Figure. 26. HRTEM micrograph of hydrophobic wafer bonding of two Si surfaces, the interface oxide layer can be seen clearly.

Further discussion of bond strength can be seen in paper VIII and other bond analysis methods are discussed in ref [59]. Spontaneous direct hydrophobic bonding is successfully performed for AlN covered wafers using a sputter deposited Si interlayer with very little observable voids seen in IR imaging, see figure 27.

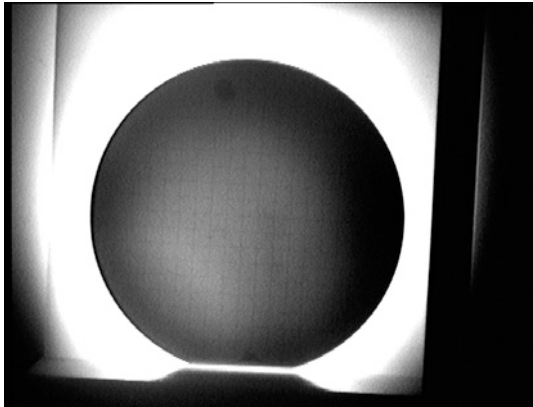


Figure. 27. Infrared transmission photograph of a smart cut SOI, with a gridded structure etched into the device layer, and Si on AlN deposited Si wafer after spontaneous bonding and annealing at 500°C for one hour.



## 5 Summary of Papers

### Paper I

In this paper a process technique from IC processing has been transferred over to fabrication of electrodes for electro-acoustic devices. In BAW devices a major limitation stems from AlN structural defects, namely cracks, formed at the edges of the patterned bottom electrode, thus limiting both device performance and reliability.

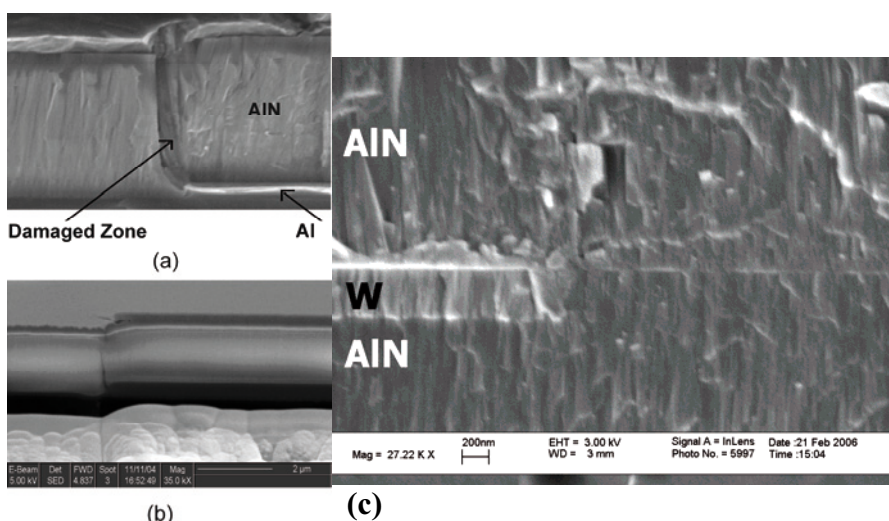


Figure 28. Cross-sectional SEM micrograph of 2  $\mu\text{m}$  thick AlN film: (a) structure of the damaged zone, (b) membrane undulation and (c) crack free growth of AlN on buried W electrodes.

These deficiencies are illustrated in figure 28 which represents two cross-sectional SEM micrographs of the area around an electrode edge. Specifically, figure 28(a) shows a close up of the defect structure around the step, while figure 28(b) shows the undulating structure of the AlN membrane resulting from the patterned bottom electrode. Here CMP is used to eliminate these technological imperfections. An additional fabrication step is introduced to bury electrodes into a sacrificial layer, and polish with CMP, resulting in a planarized surface for the subsequent AlN deposition. In figure

28(c) an SEM micrograph of an AlN film grown onto polished W electrodes, which are buried into an AlN sacrificial layer, is shown. The formation of the highly damaged zones (cracks) is no longer observed. The texture of the AlN film grown onto polished tungsten also shows a significant improvement over that grown onto untreated tungsten shown by a decrease in the FWHM of the (002) rocking curve to  $2.9^\circ$  from  $3.6^\circ$ , respectively.

Further to this a one-step lithography process for burying molybdenum (Mo) and tungsten (W) electrodes into an aluminium nitride (AlN) surface using the CMP step was developed for use in electroacoustic devices. It should be noted that Mo and W are well known to have high acoustic quality, relatively low resistivity, low electro-migration and the possibility for operation at higher temperatures. Thin film plate wave electroacoustic resonant devices (FPAR) have been designed and fabricated by means of the technology developed. Burying the reflector electrodes is also expected to have substantially improved resistance to acoustomigration effects at high powers. Results showed that FPAR utilizing buried electrodes resulted in improved reflectivity.

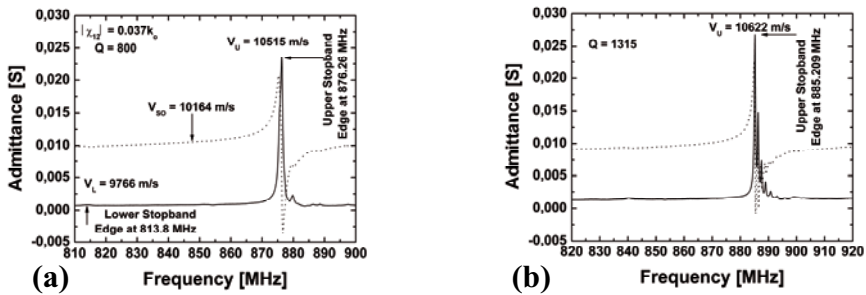


Figure 29. Close to resonance characteristics of a synchronous  $12\ \mu\text{m}$  wavelength FPAR using (a) tungsten electrodes and (b) molybdenum electrodes with fewer reflector strips. The dashed line represents susceptance and the solid line represents conductance.

Reflection parameters determined as  $|\chi_{12}| = 0.037k_0$  represented over 60% increase in reflection compared to devices with strips deposited on the surface [60]. In figure 29a the close to resonance characteristics of the device are shown. Such an improvement leads to a possibility of 60% size reduction of the reflectors keeping the entire reflection unity. The high sheet resistivity of the thin W film obtained led to slight degradation of the device quality factor (as compared with Al electrodes) which in this case approached values of up to 800. To alleviate this deficiency the W metallization was subsequently replaced by Mo as illustrated in figure 29b. Here the number of strips in the reflectors is reduced from 53 to 30. The device Q of 1315 demonstrated in this case shows the vast potential of this technology when

minimization of the plate wave components is pursued. It should be pointed out that further minimization of the parasitic electrode resistance will lead to higher quality factors. If this resistance is artificially eliminated from the measured data, intrinsic quality factors well in excess of 2000 are achieved. It should be noted that because of the strong reflections in the IDT structure, the wave excitation is an extremely narrowband function around the upper stopband edge and the wave excitation around the lower stopband edge is almost negligible. Thus, the position of the latter cannot be identified and the estimation of the reflection per strip achieved cannot be directly derived. However it can be seen that good response is still obtained even with this reduction in number of reflector strips. Thus both metallizations exhibit a substantially increased reflection efficiency resulting in a reduction of the device size.

## Paper II

This paper represents an improvement in resonator design leading the way to an increase in potential benefit towards technological integration. Membrane based resonators have been extensively studied in the last 20 years and currently demonstrate a device quality factor ( $Q$ ) approaching 2000 at around 2 GHz [61]. The drawbacks of the membrane approach are related to the relatively limited power handling capabilities [62] and the reduced sustainability to stresses in the thin films. An alternative FBAR resonator design uses an acoustic mirror, Bragg reflector, for device isolation. Currently, the limitations of the SMR technology are associated with the relatively lower quality factors achieved. Limitations in device  $Q$  at series resonance is attributed to the degrading influence of the parasitic series resistance and is expected to be more pronounced at higher frequencies of operation as the electrodes become thinner. In this work, the emphasis of device optimization is on the minimization of the parasitic resistance.

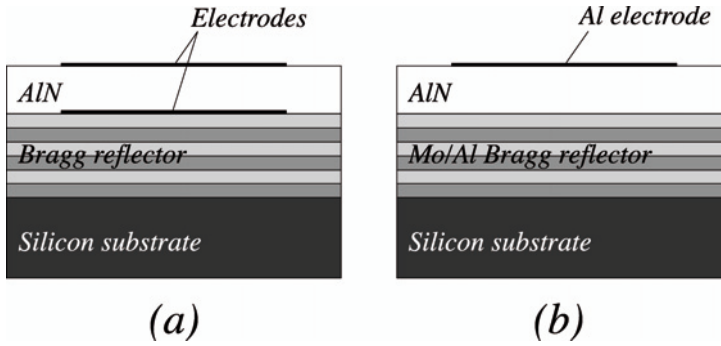


Figure 30. Resonator cross-sections: (a) conventional SMR with two thin electrodes, (b) design with an all metal Bragg reflector.

The combined electrode-Bragg reflector design proposed here can be combined with other optimization techniques which are discussed and thus a trade off between acoustic and resistive losses can be achieved. The adaptation in design is apparent in figure 30b where the top electrode is incorporated into an all metal Bragg reflector.

In Table 5 the measured and the extracted parameters for both types of resonators are shown. The combined electrode-Bragg reflector SMR exhibits a 4.5 times lower ohmic resistance than that of the conventional SMR and similar motional resistance. The former is due to the combined effects of eliminating the bottom electrode resistance and doubling the thickness of the top electrode. At series resonance the “electrodeless” and the conventional SMRs demonstrate unloaded  $Q_U$  of 464 and 382, respectively. The slightly

lower  $Q_U$  of the “conventional” SMR could be related to specific technological deficiencies. What is more important is to characterize the quality factor degradation due to the electrical parasitics. For this reason the relative quality drop,  $\delta Q = (Q_U - Q_{L,S})/Q_U$ , can be used. The combined electrode-Bragg reflector SMR exhibits quality degradation of 2.6%, which is 10 times lower in comparison with the 26% degradation for the conventional SMR. This clearly demonstrates how important the reduction of the parasitic series resistance is.

Table 5. Summary of the measured and the extracted parameters of the fabricated devices.

Parameter	“Metal Reflector”	Thin electrode
$f_S$ [GHz]	1.97	1.89
$f_P$ [GHz]	1.99	1.93
$Q_{L,S}$	452	295
$Q_{L,P}$	295	211
$Q_U$	464	382
$k_{t,U}^2$ [%]	4.1	4.2
$R_m$ [ $\Omega$ ]	1.64	1.74
$C_0$ [pF]	3.90a	3.58
$R_S$ [ $\Omega$ ]	0.24	1.1
$\eta$	51.6	31.5
$\delta$ [%]	2.6	26

<sup>a</sup> The value represents only the static capacitance of the active area. The parasitic contribution formed by the contact pad and the non-patterned Bragg reflector is taken out.

The design includes an efficient heat path through the mirror and if an SMR was composed of two metal Bragg reflectors placed either side of the piezoelectric film it is thought to result in a device with substantially improved power handling capabilities. This arises from both the reduced power dissipation, due to reduced electrode resistance, and the substantially increased heat conductivity of the Bragg reflectors. As the resonator is acoustically isolated at the frequencies of interest from its surroundings any type of low cost packaging could be used. Another advantage of the proposed design becomes apparent at high frequencies where the relative thickness of the electrodes increases in order to keep the electrode resistance sufficiently low. In such cases it has been shown [63] that at a frequency of 8 GHz this relative increase of the electrode thickness results in a 40% loss of the coupling coefficient. The design developed in this could solve this issue. Combining the electrode into the Bragg reflector creates a robust solution to many issues in SMR technology making it a more functional technology compared to membrane type resonators and increasing the ability of integration of electro-acoustic and IC technologies.

## Paper III

In this paper an adaptive design of the resonator is compared to investigate crosstalk in liquid media. The ability for sensors to be created using TEA technology also increases the compatibility for sensors to be integrated with IC technology in smaller transportable devices. Once more the SMR design is utilised but in this application with liquid media a tilted AlN film is required to operate in the thickness shear mode. The liquid was placed into contact with the top electrode, M2, which consisted of 100 nm Au/Pt. The micro-fluidic system was defined in PDMS. The device design can be seen in figure 31.

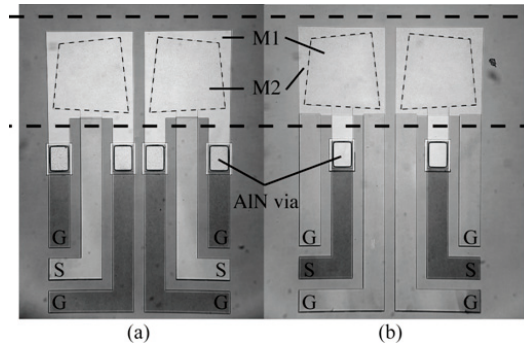


Figure 31. Photomontage of the two configurations of sensor arrays prior to PDMS placement. The extent of the fluidic channel is indicated by the horizontal dashed lines. The apodized areas indicate the active area of the resonators. The distance between the resonators is 50  $\mu\text{m}$ .

In figure 31a the signal is connected to the top electrode (M2) and is thus in contact with the conductive liquid (S-1), whilst in figure 31b the signal line is connected to the bottom electrode (M1) configuration S-2.

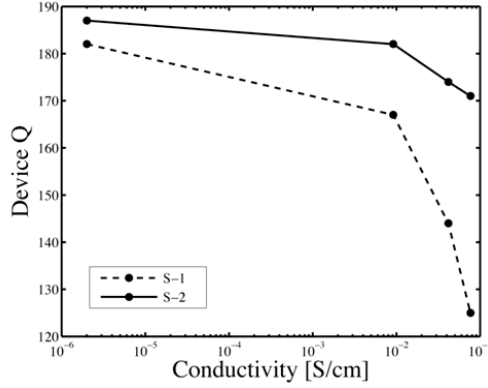


Figure 32. Device Q in the two sensor arrays as a function of liquid conductivity. The Q degradation is more pronounced for the S-1 array (dashed line), than for the S-2 array (solid line).

The resonators in the arrays had an operating parallel frequency  $f_p$  around 1.3 GHz with a Q value in de-ionized water of 180. Figure 32 shows the drop in Q value as a function of liquid conductivity. For S-1, the drop was about 31% for the highest conductivity, while for S-2 the maximum drop was only 9%. It is also seen that when the conducting liquid is in contact with the signal line the cross talk increases due to the additional fringe capacitance and ohmic leakage paths through the liquid. With the alternative configuration presented the top electrode and liquid define the ground plane, shielding the electric field from the free ions. With the signal now applied to the smaller bottom electrode, the effective capacitance remains unaltered and the cross talk is minimized.

## Paper IV

This paper investigates further promotion of TEA and IC technology by replacement of the electrode material. Currently, Al and Mo metallizations are in use. Both metals have such limitations that research into an alternative metallization compatible with AlN is essential. Here it is proposed to use NiSi, an existing IC metallization, for resonator electrodes thus increasing the compatibility of TEA and IC technology. Electro-acoustic applications require silicide thickness in the order of hundreds of nanometres. The existing technologies present thick silicides with increased surface roughness, resulting in poor AlN growth as well as increased acoustic losses, both of which are unfavourable for FBAR applications. The increased roughness can be seen in figure 33 where the zero and one pairs demonstrate surface roughness values in excess of 5 and 9 nm respectively. The zero and one pairs consist of a silicided thick layer of Ni deposited on bulk silicon and sputter deposited silicon layer, respectively.

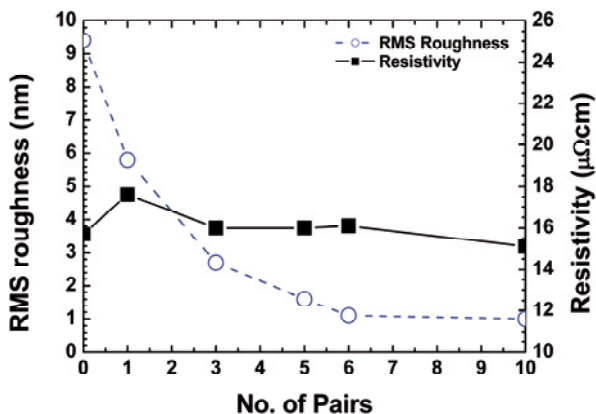


Figure 33. Surface roughness rms values and corresponding NiSi resistance for different multilayer stacks, with open circles using left scale and closed squares using right scale, respectively.

Instead a fabrication process, described more fully in the paper, involving thinner multilayers was investigated. Here it was discovered that thinner layers, therefore more pairs to achieve the same thickness, resulted in a positive influence on the surface roughness of the film. The decrease in surface roughness is probably related to the distance travelled by the Ni diffusing species during silicidation [43]. Smooth roughness values approaching 1 nm rms, beneficial to AlN film growth, are seen for the more finely layered structures having 5, 6, and 10 pairs, respectively. The measured resistivity of

the resulting NiSi films tends toward  $15 \mu\Omega \text{ cm}$ , achieved by the ten pair stack, in agreement with published values [39].

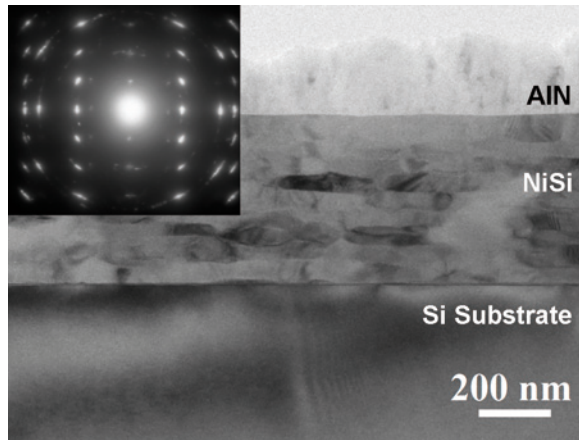


Figure 34. TEM micrograph of a 10 pair NiSi film with deposited AlN. Insert is a local area diffraction pattern of the AlN film.

Cross sections of the films were studied using SEM and TEM. A micrograph of a ten pair NiSi film after silicidation shows over 300 nm thick in figure 34. No consumption of Si, from the substrate can be seen from the silicidation process. Surprisingly, the layered structure is still present. However, the original ten pairs seem to have merged into only eight layers and a thicker top layer. This can be explained through the dominant diffusion species, Ni, which diffuses into the adjacent Si layers during the silicidation. The Ni and Si atoms interact and independently form NiSi crystallites, consuming all the Ni in the process. The independently formed layers of NiSi crystallites meet at the centre of each initial Si layer. In the case of the thicker top layer, the Ni here, in contrast to the inner Ni layers, is only in direct contact with a single Si layer. This Ni is not shared between two Si layers and therefore has enough Ni remaining free to diffuse all the way through to the next Ni layer forming a uniform NiSi layer twice as thick as the underlying NiSi layers. A fuller explanation of this effect and the reordering of the crystal structure as observed with XRD is given in the paper.

The result of AlN grown on a ten pair stack is seen in figure 34, where the TEM analysis shows a void-free nucleation of the AlN film and the high film quality is also illustrated by the well-defined (002) AlN reflections in the high-resolution TEM insert of figure 34.

## Paper V

As suggested in the previous paper the use of NiSi electrodes will bring several benefits to FBAR technology such as reduced susceptibility to either electro- or acoustomigration effects which degrade device performance. It also is a potential replacement material for the common used low acoustic impedance material Al with the benefit of enabling high voltage, high power or high temperature sensor applications. It has even been highlighted that even Mo has limitations stress [64] and oxidation [62]. For integration issues in IC Mo requires unfavourable post-annealing steps up to 900°C for front end CMOS processing of CMOS transistors [65] whilst NiSi is considered the most versatile silicide for this purpose [39]. In this paper NiSi electrodes were fabricated on simple membrane type resonators and compared to simultaneously fabricated resonators consisting only of Mo electrodes. To obtain good devices investigations into AlN deposition on rough NiSi surfaces was performed using a Ti seed layer. Here the thickness of the Ti seed layer was investigated with the results shown in figure 35.

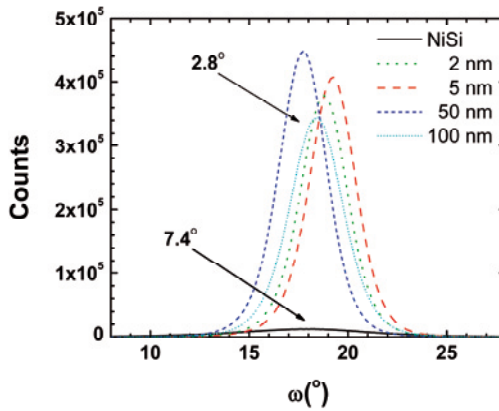


Figure 35. FWHM of the (002) rocking curve, for AlN deposited onto a Ti seed layer on NiSi with a surface roughness of 2 nm.

The seed layer thickness was varied to investigate the effect of the surface roughness carried forward from the underlying NiSi film. Thin seed layers, with a thickness in the range of the surface roughness, would follow the contours of the surface whilst thick seed layers, deposited with a thickness of over one magnitude greater than the surface roughness, would smooth out the resultant deposited surface. If the main influence is from the roughness of the surface then the texture of AlN grown onto Ti will be improved for the thick Ti films. To the best of the authors' knowledge this effect has not been

investigated previously. Results indicate that even on a substrate which has a poor surface for AlN growth, we can improve the quality of the AlN film greatly by the use of a Ti seed layer. It is also clear that the thickness of the Ti film has no significant influence on the quality of the AlN film, not even when the Ti film is thick enough to smooth out the surface roughness of the underlying NiSi layer. The dominating influence here is therefore the relatively good crystallographic match of the Ti surface structure to AlN, both of which have a hexagonal crystallographic structure.

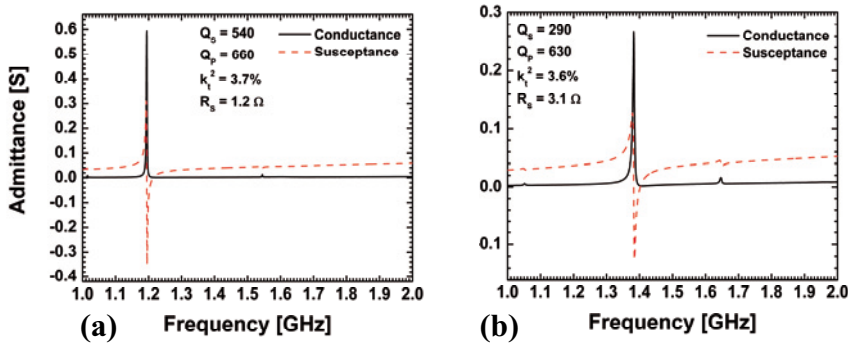


Figure 36. FBAR response of resonator based on (a) Mo top electrodes and (b) NiSi top electrodes. The dashed line represents susceptance and the solid line the conductance.

The results of the resonator comparison can be seen in figure 36. Both types of devices exhibit one and the same AlN quality since all FBARs had a bottom electrode of molybdenum. Loaded parallel  $Q$ 's approaching 700 were obtained for both types of device. The NiSi top electrode FBAR has a series  $Q_s$  of around 300, which is less than the  $Q_s$  of 540 for the Mo electrode which can be attributed the difference in series resistance,  $3.1 \Omega$  to  $1.2 \Omega$  respectively. The loaded device couplings,  $k^2t$  were found to be 3.7% for Mo top electrodes and 3.6% for NiSi top electrodes. The reduction in effective coupling is attributed to the parasitic parallel capacitance formed between the connecting signal line and the non-patterned bottom electrode [66] and further reduction in coupling also arises from the quality of the piezoelectric film [22]. Hence the observed electromechanical coupling is quite reasonable.

Further investigations were conducted on the acoustic quality of NiSi. Simulations were conducted demonstrating NiSi as a replacement for Al as the low acoustic material in an all metal Bragg reflector.

## Paper VI

In this paper film deposition methods for depositing AlN are adapted to fabricate alternative material for future integrated capacitor structures. The flow of the precursor gases, in the reactive dc magnetron sputtering used, determines the film composition, although the relationship between flow and stoichiometry is highly nonlinear. Due to this complex processing behaviour, careful analysis of the stoichiometry of the deposited films is required. Furthermore the functionality of the films also depends both on the stoichiometry and the impurity levels, making an exact chemical analysis even more important. Composition of AlON films is analyzed with elemental depth profiles are obtained by X-ray photoelectron spectroscopy (XPS) in combination with sputter sectioning and time-of-flight elastic recoil detection analysis (ToF-ERDA).

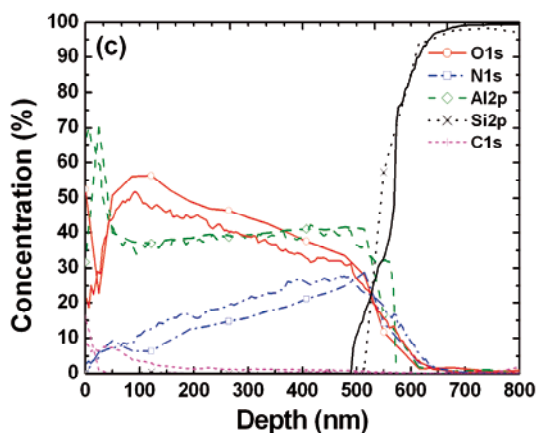


Figure 37. Elemental depth profiles obtained by ToF-ERDA no symbols and XPS sputter profiling open symbols. Combined conversion to a nm depth scale of AlON.

Both kinds of measurements revealed variation in film composition throughout the whole film thickness, figure 37. There are advantages and disadvantages for both film analysis methods revealed during the comparison. Measurements from ToF-ERDA can distinguish trace elements and contamination unseen through XPS sputter profiling, such as H and Ar. There can also be effects seen through preferential sputtering which change the composition seen through XPS. This effect was not seen in this work. The advantage for XPS is the ability to distinguish between differing binding states, therefore more information on the chemical make up of the samples, and it is generally more available. Conversion of depth profiles, for both ToF-ERDA and XPS, into a nm depth scale using film thickness obtained with SEM micro-

graphs of film cross section is performed improving the agreement between the methodologies further. Although both methods were able to independently verify each other and each was shown to be able to investigate film composition alone it was seen that a combination of both techniques during the initial studies of new materials would be a powerful tool for film analysis. ToF-ERDA is especially useful in providing the composition of an unknown sample, which subsequently can be used with XPS to obtain sensitivity factors specific to elements in the sample and equipment specific influences.

# Paper VII

Passivation layers of reactively sputtered AlON are deposited with varying composition and studied. The aim is to investigate its potential for use as a dielectric for silicon carbide (SiC) surface passivation.

Table 6. Summary of Depositions

Set No.	Deposition	Thickness [nm]	Stoichiometry		Surface pretreatment	Diodes incl.	Breakdown	Breakdown
			XPS <sup>1</sup> Al:N:O [%]	RBS <sup>1</sup> Al:N:O [%]			field before/ after anneal p <sup>2</sup> [MV/cm]	field before/ after anneal n <sup>3</sup> [MV/cm]
1	Al <sub>4.4</sub> N <sub>4.6</sub> O <sub>1</sub>	197	44:46:10	40:50:10	UV	Yes	-5.7/-6.8	7.3/7.3
2	Al <sub>4.5</sub> N <sub>4.7</sub> O <sub>0.8</sub>	98.5	45:47:8	45:47:8	UV	No	-6.0/-6.0	6.9/6.9
3	Al <sub>4.5</sub> N <sub>4.7</sub> O <sub>0.8</sub>	98.5	45:47:8	45:47:8	RCA1	No	-5.9/-6.8	6.2/-6.0
4	Al <sub>4.5</sub> N <sub>4.7</sub> O <sub>0.8</sub>	197	45:47:8	45:47:8	UV	Yes	-5.5/6.8	6.4/6.4

<sup>1</sup> at the SiC interface, <sup>2</sup> on a p-type semiconductor in accumulation, <sup>3</sup> on a n-type semiconductor in accumulation

The passivation structure was formed by a thin SiO<sub>2</sub> buffer layer which provides a good interface quality and large band offsets, while the thick high-k top dielectric layer suppresses the electrical field outside of SiC device. Film roughness varied from 1.5 to 2.3 nm for Sets 1 and 4 (200 nm) and from 1 to 2.1 nm for Sets 2 and 3 (100 nm). Films with a low oxygen content demonstrated a preferential (002) texture as determined by XRD. The AlN [002] peak intensity of the film with 10% oxygen content is 5 times lower compared to the film with the 8% oxygen content, indicating poorer crystallinity. The extracted average dielectric constant was 8.4 and 8.9 for the films with 8% and 10% oxygen content, respectively.

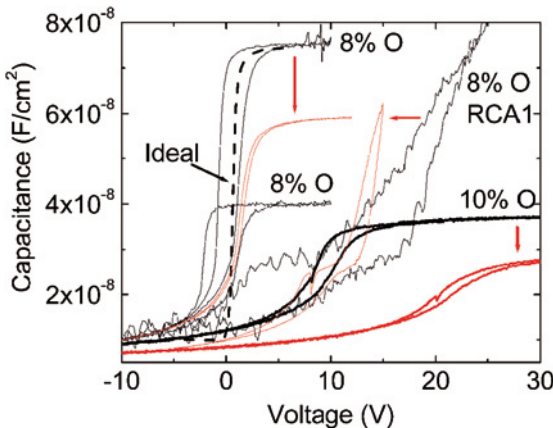


Figure 38. CV characteristics (100 Hz) of the AlON films deposited on 4H-SiC surface without SiO<sub>2</sub> buffer layer.

Analysis of the electrical quality of the film found a large net negative interface charge for samples with 10% oxygen content and for samples with 8% oxygen content and subjected to RCA1 surface cleaning, prior to deposition. In both cases the large negative charge is believed to originate from excess of oxygen at the SiC interface. For samples with 8% oxygen and UV treatment the hysteresis corresponds to  $N_{\text{int}}$  of about  $8 \times 10^{11} \text{ cm}^{-2}$  for both thicknesses (Set 2 and 4). Since oxygen is the most probable source of ionic species in the reactive sputtering process the hysteresis should be dependent on the oxygen content as well as on the thickness of the AlON film. The comparable value of the hysteresis for the samples with different AlON thicknesses, but the same oxygen content, indicates that the charge responsible for hysteresis is not caused by charge migration in the bulk insulator but is due to polarization phenomena.

Thermal treatment, 400°C in a forming gas, reduced the relative dielectric constant to 6.6 and 6.8 for the AlON films with 8% and 10% of oxygen, respectively. The CV hysteresis measured is also reduced for all samples, see figure 38, the arrow indicates results after annealing. It was also observed that annealing reduces leakage current by up to two orders of magnitude, however, the general leakage current characteristics are very similar to those before annealing.

It was also observed that passivated SiC diodes measured at the reverse bias of 100 V (not shown) have a leakage current reduced by a factor of 3 and 2 for the 8 % and 10% oxygen films (Set 4 and 1), respectively, compared to non-passivated devices. The reduction of the leakage current is most probably caused by the negative charge that originates from the AlON/SiC interface states and polarization in the AlON layer, leading to an extension of the depletion region.

It is therefore seen that AlON is a promising material for SiC device passivation with a reduction in the leakage current of SiC diodes.

## Paper VIII

The final paper investigates the bonding of buried AlN layers to high quality silicon for the fabrication of alternative SOI substrates. Alternative insulation layers are needed in SOI as the continuous scaling of device size and poor thermal conductivity of SiO<sub>2</sub> brings about increased self-heating in SOI MOSFETs which is responsible for degradation in mobility, threshold voltage, sub threshold swing and leakage current [67]

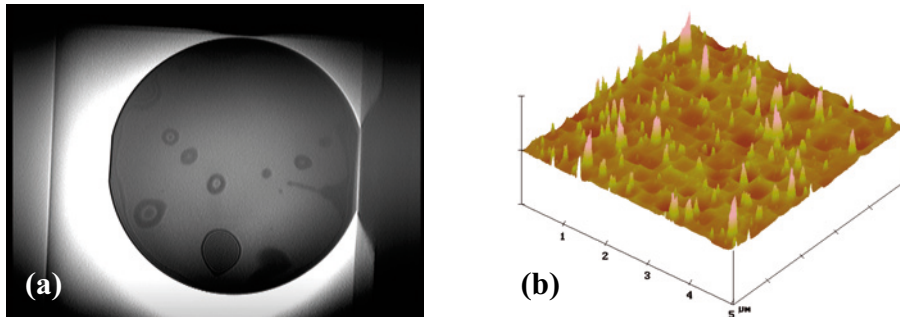


Figure 39. (a) Infrared transmission photograph of after spontaneous bonding and annealing at 500°C for 1 hour and (b) AFM micrograph of transferred Si device layer,  $Z = 100$  nm/division with an rms of 5.6 nm.

The first problem to resolved in the paper is to transfer a silicon device layer onto a reactively sputter deposited AlN film. The solution used is to hydrophilically bond a commercial SOI substrate with the fabricated substrate. Due to the need for chemical treatment of the surface for cleaning and promotion of a hydrophilic surface it was found that the AlN surface needed protecting. This was resolved through sputter depositing an amorphous Si ( $\alpha$ -Si) film directly after deposition of the AlN in the same deposition system without breaking vacuum. An added benefit of this procedure was the improvement in prepared surface roughness from 0.7 nm for as deposited AlN to 0.3 nm with a covering of amorphous Si. A weak bond is formed after spontaneous hydrophilic bonding of the wafers so an annealing step is performed at 500°C in a N<sub>2</sub> ambient for 1 hour. The annealing step strengthens the bond considerably to a point test wafer fractured perpendicular to the bond surfaces during the crack test. It was estimated that the bond strength was in the region of 1.2 J/m<sup>2</sup> which was an improvement on values reported elsewhere [68-69]. An infrared transmission image of the annealed bond can be seen in figure 39a, where large bonded areas are seen with few voids. The commercial SIMOX wafer used was seen to have a rough surface of 1.3 nm with 5 nm deep pits in the surface. The smooth surface of the AlN prepared wafer is believed to compensate for this roughness and the SIMOX rough-

ness itself is believed to act as an escape channel for trapped gases during the bonding and subsequent annealing promoting void free areas.

Final transfer of the SOI device layer is achieved by etching of the SOI handle wafer with the Bosch process and a HF dip to remove the buried  $\text{SiO}_2$  layer. The transferred Si device layer is shown in figure 39b. The pits from the device layer are still evident but now 8 nm deep and the surface roughness is 5.6 nm, although increase in roughness could be due to the new surface originally belonging to the backside of the SIMOX device layer Si.

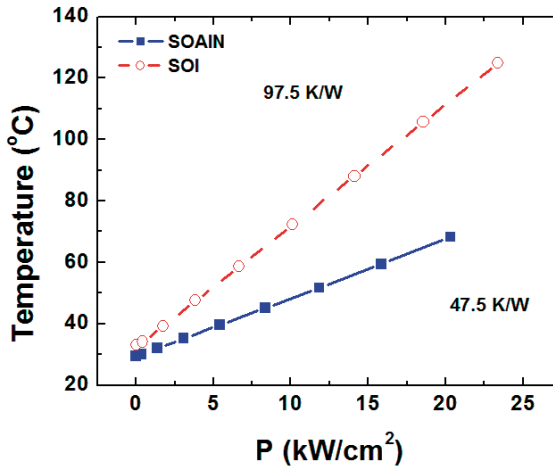


Figure 40. Measured temperature as a function of applied power density for SoAlN and SOI substrates.

Thermal devices were then fabricated in the new SoAlN substrate using standard CMOS processing. Devices were fabricated in a standard commercial SOI simultaneously. The results are shown in figure 40. The thermal resistance of 97 K/W for the commercial SOI substrate is in good agreement with those reported by Whipple et al. [15]. The new SoAlN substrate has an improved performance with reduced self heating effects and an effective thermal resistance half that of oxide, 47.5 K/W. The thermal conductivity of AlN is around 2 W/cmK, whilst  $\text{SiO}_2$  is 0.014 W/cmK, indicating that even better performance should be expected. On analysis it became clear that other thermal barriers are contributing to the temperature raise measured for the devices fabricated on the SoAlN wafer. These barriers are identified as the  $\alpha$ -Si layer used to protect the AlN surface, which has a similar thermal conductivity to  $\text{SiO}_2$ , the thin bonding oxide and the interfaces between each layer in the structure. Solutions to reduce the effect of these barriers are identified such as thinning or removal of the  $\alpha$ -Si or thermal recrystallisation of  $\alpha$ -Si.

It has been shown that new SOI structures are possible to be fabricated and with development can utilise the improved thermal conductivity of AlN. Added to this advantage reactively sputtered AlN films are already used in a number of acoustic applications such as resonators and sensors [70-71]. Therefore another benefit of using AlN is also enabling integration of IC and electro-acoustic technology.

## 6 Future Trends and Further Development

In general terms there is a significant lag time between invention and fabrication in the high tech industry. For both the fields of TEA and IC, the established leaders in these industries will look for advantages in their fields. This usually occurs through small improvements in current technology, design or fabrication techniques. Therefore it could seem unlikely that full integration of these technologies will happen in the near future. This becomes more difficult to analyse when the benefits and difficulties have yet to be fully counted. It seems clear that using just one substrate and fabricating both resonators and CMOS on the same chip should save in time, material costs, personnel, and packaging. The use of one chip solutions could even possibly enable a simple upgrading capability without the need for replacing the whole mobile unit. However, this has yet to be proved. Both parts can be hermetically sealed and flip chip packaged together at reasonable cost with all the facilities already available and in use. For a change into complete integration there may be need for one of the industries to upgrade facilities, there could be compatibility issues, require new knowledge of the others technology and require a whole process flow of design to take advantage of all this would bring. This also leads to the question of which industry would lead the integration, even in a partnership.

However it could be argued that integration reduces the foundries needed for fabrication, combines similar techniques and even uses the similar engineers and design methods.

There are also other indicators for change such as Intels recent change over from  $\text{SiO}_2$  to  $\text{HfO}_2$  many years after the first research by academic institutions into high-k dielectrics for transistor gates. The silicon industry also researches MEMS resonators based on micromachining of silicon as opposed to piezoelectric. Both these factors signify that integration is considered as a technology of the future, more recent developments of bio-sensors based on FBAR's creates alternative markets that could even lead the way into this era. The need for lower power consumption and sustainable resources are also contributing factors in drive for research and change in how costs are calculated for any change in fabrication.

In this thesis three main ideas have been investigated which could all help the integration process. Firstly two papers have investigated improvements or alternative use of solidly mounted resonators which is a much more robust design and suited towards an integrated approach. It is shown that an all

metal Bragg reflector can be used as the electrode thus reducing the series resistance, improving Quality factor, removing the electrode from the resonance cavity and creating an efficient heat path through the Bragg mirror. Secondly the use of IC technology such as CMP and NiSi in resonator fabrication also increases common process areas for the technologies as well as having individual benefits for TEA. These benefits include a reduction in migration effects, increased reflection in IDT's, therefore reducing device size and solving cracking at electrode edge via use of CMP or providing alternative low acoustic electrodes which are more chemically stable, even at high temperatures, for use in high temperature sensors in the case of NiSi electrodes. Alternatively AlN can be utilised in several IC areas as a high-k material with the advantage of low interface charges and survivability for high temperature Si gate processing or as a passivation layer for devices made in SiC where the high critical fields reach the limits of SiO<sub>2</sub>. Within this area AlN is a very interesting material once more for replacement of SiO<sub>2</sub> but this time for its high thermal conductivity. In this case the proposal is to use an AlN buried insulation layer for alternative SOI substrates to reduce self heating effects. The concept has been proved and can be taken further through improvements in processing and use of thicker AlN films. There is even a possibility to use AlN piezoelectricity to put strain on a silicon device layer thus changing carrier mobility. There are several users of SOI in the chip industry, such as AMD, IBM and it is used in Xbox 360, PlayStation 3 and Wii games modules, although bulk Si is still has the biggest market share with Intel. Once more though with the newly created Foundry Company, once of AMD, with facilities in Dresden using SOI this is still a technology of the future. Therefore a substrate which includes the piezoelectric material has an added advantage for processing resonators together with IC components.

Overall the research performed here has benefits for FBAR or IC alone but also has the advantage of enabling any integration between the two technologies. Whether this will be the case remains to be seen, however with a large amount of research still being conducted in this area [72-76] it seems that the will is already there.

## 7 Sammanfattning på svenska

Det är under den senaste tioårsperioden som piezoelektriska tunnfilmsmaterial har börjat ersätta enkristallina piezoelektriska bulkmaterial i elektroakustiska högfrekvenskomponenter. Förutom att tunnfilmskomponenter klarar högre frekvenser så kan produktionskostnaden bli lägre eftersom relativt billiga icke-piezoelektriska substrat som t.ex. kisel kan användas. Denna möjlighet att välja substrat och piezoelektriskt tunnfilmsmaterial som t.ex. aluminiumnitrid (AlN) gör produktionen av komponenter i GHz området kostnadseffektiv och flexibel. Denna teknik användes av Agilent Technologies vid tillverkningen av tunnfilms-bulkakustiska resonatorer (FBAR) som var först med att starta masstillverkning av FBAR år 2001. Genom att använda material som AlN vars deponeringsmetod är förenlig med tillverkningen av integrerade kretsar (IC) så kan traditionellt två olika inkompatibla teknologier integreras som därmed kan resultera i ytterligare kostnadseffektivisering och miniaturisering. Bild 41 visar exempel på två vanligt förekommande substratmaterial inom traditionell teknologi med en enkristall av kvarts (a), samt tunnfilmsteknologi med en kiselskiva belagd med ett tunt lager metall (b).

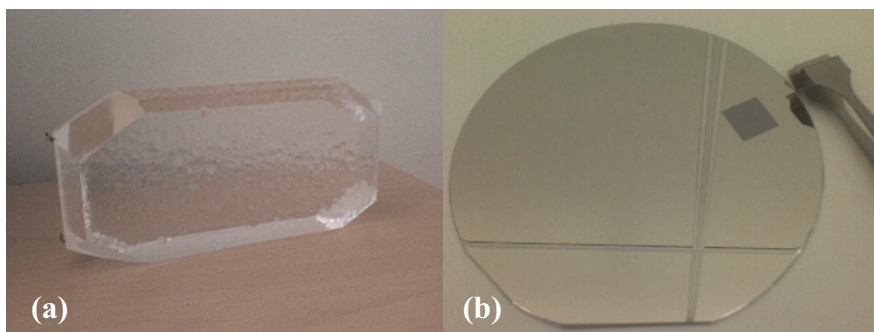


Bild 41. (a) ett stort stycke enkristall av kvarts och (b) en kiselskiva med ett tunt lager sputter-deponerad metall på ytan.

Forskningsarbetet som presenteras i denna avhandling har fokuserats på delar som är viktiga för integreringen av tunnfilmskomponenter med IC-teknologin men arbetet har också bidragit till utveckling inom båda forsk-

ningsområdena var för sig. Ett viktigt och återkommande material i arbetet är AlN, antingen som piezoelektriskt material i elektroakustiska komponenter eller som elektriskt isolerande material i IC-tillämpningar. I elektroakustiska komponenter som t.ex. resonatorer sker en kontinuerlig omvandling av elektrisk energi till akustisk energi (ljudvågor) i strukturen och vice versa. För att nå optimal prestanda måste alla former av energiförluster (mekaniska och elektriska) till omgivningen minimeras. En typ av resonatordesign kallas SMR (solidly mounted resonator) där den akustiska isoleringen mot substratet (omgivningen) utgörs av ett multilager av tunna lager av material, sk. Braggreflektor. Genom att välja elektriskt ledande material i reflektorn kan denna förutom akustisk isolering samtidigt definiera ena (eller båda) elektroderna vilket resulterar i en minskad serieresistans, bättre Q-värde, öka förmågan att klara högre effekter samt utgöra en del av kapslingen av komponenten (artikel II). Detta är en robust design som ger stora fördelar vid integrering med andra komponenter och där t.ex. crosstalk mellan sensorer i kontakt med vätskor kan minimeras (artikel III). Just olika typer av sensorer utgör en enorm marknad där FBAR-teknologin, integrerad med IC-teknologin ger möjlighet till pålitliga, små och billiga mobila sensor enheter.

I utvecklingsarbetet av elektroakustiska komponenter har alternativa processer använts som är vanliga inom IC-processning, t.ex. kemisk-mekanisk polering (CMP) för planarisering av substrat. I artikel I används denna metod för att lösa typiska problem inom FBAR tillverkning, som sprickbildning i AlN-filmen p.g.a. underliggande steg runt elektrodkanter och elektro- eller akustomigration i elektroder. Arbetet omfattar också syntetisering av nickel-silicid (NiSi), ett material som inom IC-teknologin används som kontakter i CMOS-transistorer. För att kunna använda NiSi som elektrodmaterial i FBAR's krävs en tjockare film än vad som traditionellt används i CMOS-processer vilket har medfört att en helt ny tillverkningsprocess för tjock silicid har utvecklats. Resultatet är en deponeringsprocess för flera hundra nanometer tjock silicid med hög ytjämnhet och låg resistivitet, lämplig som elektrod i högpresterande FBAR's (artikel IV och V).

I många av tillämpningarna är materialkaraktisering av AlN en viktig del för att kontrollera filmtextur och renhet som är avgörande för de piezoelektriska egenskaperna, eller ytjämnhet som är viktigt vid sammanfogning av skivor i en bondningsprocess. Metoder för analys och karaktisering av material har därför varit av central betydelse i denna avhandling. Bild 42 visar exempel på några av de analysinstrument som använts i detta arbete.

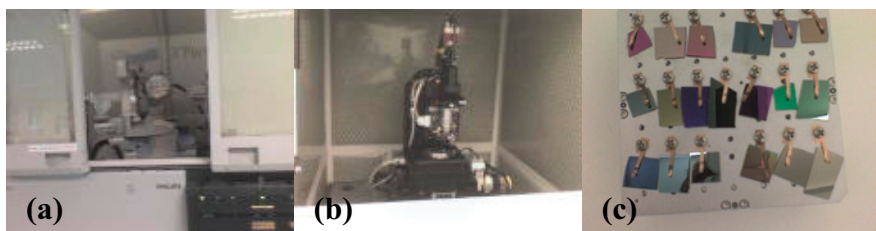


Bild 42. Några analysinstrument som använts i detta arbete, (a) röntgendiffraktometer (XRD), (b) atomkraftsmikroskop (AFM) och (c) provhållare för röntgenspektroskopi med ett antal AlON filmprover.

Slutligen har AlN studerats för IC-tillämpningar som "high-k" dielektrika, passiveringslager eller som ett alternativ till SOI (silicon on isolator) substrat (artikel VI, VII och VIII). Med en serie experiment har AlN-filmer med varierande grad av kristallinitet och syreinhåll studerats. Resultaten visar att AlN med högt syreinhåll har sämre dielektriska egenskaper trots att amorf-filmer generellt har lägre läckström än polykristallina filmer p.g.a. av färre korngränser. För att kunna använda AlN som material i SOI substrat har arbetet fokuserats på att utveckla en bondningsprocess för överföring av ett enkristallint kisellager till en sputtrad AlN-yta. Med denna metod har SoAlN (silicon on aluminiumnitride) substrat tillverkats och jämförts med kommersiella SOI substrat. Resultaten av mätningar på komponenter definierade på de båda substraten visar en förbättring av den termiska ledningsförmågan hos SoAlN jämfört med SOI.

Resultaten av denna avhandling visar på många gemensamma tekniska lösningar och förbättrade processer som möjliggör en full integrering av IC och tunnfilmselektroakustik (TEA). Resultaten kan dessutom användas inom båda teknologierna var för sig för att uppnå bättre egenskaper och prestanda.



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