DEVELOPMENT OF A SUSPENDED, ROBUST, THERMALLY INSULATED MICRO CHAMBER OF THICK SILICON DIOXIDE FOR MICROTHRUSTERS AND MICROREACTORS

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Abstract: Using the technique refilling etched high aspect ratio trenches through thermal oxidation, chambers for microreactors and microthrusters thermally insulated by thick silicon dioxide structures has been fabricated. The components, with integrated heaters, have been imaged using an infrared camera and their insulating capabilities have been confirmed. The chamber top wall temperature is increased 250ºC with 1 W of supplied power. The design has been proven successful but some processing aspects are yet to be solved.

Keywords: microreactor, microthruster, thermal insulation, trench oxidation

INTRODUCTION

Due to the versatile processing capabilities and material characteristics, silicon is widely used for microreactors [1] and micropropulsion systems [2]. However, its high thermal conductivity can cause heat loss or unwanted heating of parts of the structures. To mitigate this problem, suspending, interfacing structures can be made to offer a high thermal resistance, either through their shape or material. Materials such as Pyrex or quartz glass are typically used because of their low thermal conductivity (and also because of their low cost, optical properties and because they are moe inert than silicon). However, the possibility to structure them in micromachining processes is somewhat limited.

Another approach is to fabricate suspending tube structures of thin silicon nitride films formed by Low Pressure Chemical Vapor Deposition (LPCVD) for thermal insulation [3]. The typical 2 µm thin silicon nitride tube walls have low thermal conductivity because their cross-section is small and have relatively low thermal conductivity. However, such tubes can also be fragile.

In this paper, the development of robust micro chambers thermally insulated by thick silicon dioxide is reported. The thick oxide is realized using deep reactive ion etching (DRIE) of trenches, which are refilled through oxidation of the remaining silicon [4]. Using this technique, fabrication of thick bulk oxide as well as thinner structures is enabled. By controlling by design where thick oxide is grown, channels and chambers with high aspect ratio, and heat-conducting silicon structures embedded in the oxide can be realized. The chambers developed here are used as reaction chamber in microreactors or as plenums and nozzles in a Free Molecule Micro Resistojet (FMMR).

First, the working principle and design of the devices are presented. This is followed by a description of the fabrication process, and a characterization of the devices and their fabrication.

FABRICATION PRINCIPLE AND DESIGN

Thick silicon dioxide is created by DRIE etching high aspect ratio trenches in silicon and refilling them through oxidation [4]. During thermal oxidation of silicon, 0.44 µm of silicon will grow to a 1.00 µm thick silicon dioxide film. Consequently, the surface will be raised by 0.56 µm above the initial silicon surface. So, provided the ratio of etched trench opening width to interlaying silicon pillar width is 0.56/0.44, the silicon oxidation will, in theory, oxidize all silicon so that the trench between to pillars will be completely refilled just when all silicon in the pillars has been oxidized. Too wide silicon pillars will result in residual, embedded silicon, while to thin pillars will leave trenches open.

When designing the lithography masks for the trench etching, care must be taken to compensate for widening of the pattern due to lithography and undercut during etching. The thickness of the oxide created, is limited by the etch depth of the narrow trenches, whose widths can not be larger than a few micrometers for a practical oxidation time.

Here, the thick oxide is used as walls of the chambers and channels in microreactors and FMMRs. The microreactors presented here, Fig 1, have two or three fluid connections through vias in the bottom wafer from which channels lead into a chamber with thin silicon walls, The chamber is embedded in thick silicon dioxide. On its top, there is a silicon thermal via through the oxide so that there is a thermal conducting connection between the chamber and a heating metal meander on top of the silicon via. A thin thermal oxide (not shown in Fig. 1) between the silicon via and the metal provides electrical insulation. In the FMMRs, exhaust expansion slots are etched through the silicon via in-between the metal meander lengths.

An FMMR is a thruster capable of low-pressure operation because it does not rely on pressure driven flow. Instead, a gaseous or liquid propellant exits the plenum through the long, narrow expansion slots in

which the flow is molecular, *i.e.* the slot width is smaller than the molecule mean free path, and molecules will collide more with the surrounding walls than with other molecules in the gas. By heating the slot walls, the gas molecules will gain energy from the walls and increase their exit velocity from the thruster. In contrast to thrusters based on pressure-driven flow, such as cold gas thrusters or resistojets, the shape of the nozzle is not critical in an FMMR.

FABRICATION

Two double side polished 4" diameter, 525 µm thick (100) silicon wafers (Topsil Semiconductor Materials A/S, Denmark) are used as substrates. Microreactors and FMMR thrusters are fabricated on the same wafer and the only difference is that the FMMRs have one additional mask patterning and etching step.

After an RCA cleaning process, the wafers are thermally oxidized to grow a 1 µm thick silicon dioxide film before standard UV lithography using 1 µm thick positive photoresist (Shipley 1813, Rohm and Haas, Germany) and silicon dioxide plasma etching (Tegal 110 S/DE, Tegal Corporation, USA) is used to pattern alignment marks on both wafer frontsides.

A 1000 W oxygen plasma (300-series, PVA TePla, Germany) is used to remove photoresist and polymer residue before the wafer frontsides are patterned using UV lithography. Oxide plasma etching is used to open the oxide mask pattern for etching of silicon trenches on the wafer frontsides. In the masks used here, the trench and pillar widths are 2.0 and 2.8 µm, respectively.

After plasma removal of the resist, the top wafers

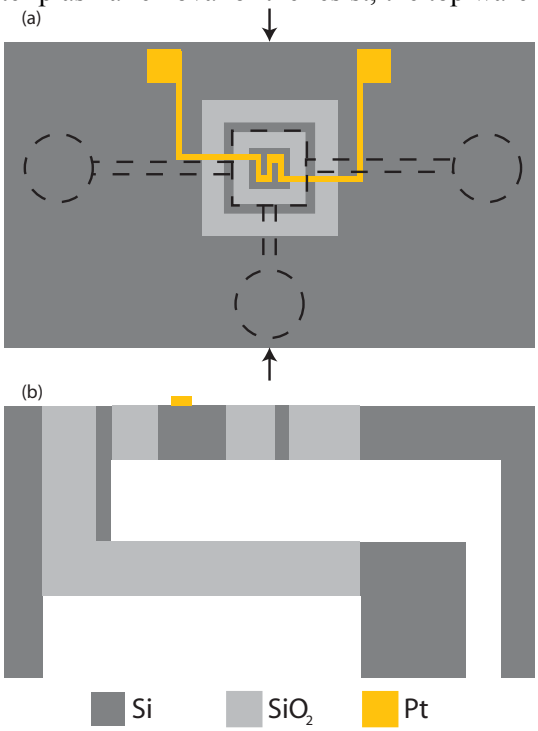

Fig. 1. Schematic of the microreactors with: (a) top view, and (b), cross section along the line indicated by arrows in (a).

backside is patterned using UV lithography and oxide plasma etching to open the oxide mask pattern for silicon trenches etched from the wafer backside, and the flow channels and chamber openings.

The resist is removed in oxygen plasma and 4 µm thick negative photoresist (ma-N 1440, Micro Resist Technology GmbH, Germany) is spun on the top wafer's backside before it is patterned using UV lithography. The resulting mask covers the trench pattern so that only the channel and chamber pattern is open and DRIE etched (Tegal 110 S/DE, Tegal Corporation, USA) using high-etch-rate recipe to a depth of about 475 µm.

After the DRIE, the resist is removed with oxygen plasma and the backside is ethched using a high aspect ratio recipe. The etch rate in the channel and chamber pits is lower than in the trenches.

Using the high-aspect-ratio DRIE recipe, the trenches on both wafers frontsides are etched to a depth of about 70 µm (meaning that there is some through etch on the top wafer where the trenches reach the channels and chambers).

Etch residues are removed using oxygen plasma, and subsequent RCA cleaning. The wafers are wet oxidized in 1100ºC (VF-1000, Koyo Thermo Systems) for 43 hours to grow a 3.8 µm thick silicon dioxide film refilling the trenches.

Positive photoresist (AZ9260, Clariant Corporation, USA) diluted with methyl ethyl ketone and AZ EBR (Clariant Corporation, USA) (1:4:20) is sprayed (EVG 101, EVG Group, Austria) on the bottom wafer backside to form a 6 µm thick film and openings for in- and outlet vias, and for cavities under the chambers and surrounding oxide. After UV lithography, the exposed oxide is etched using plasma etching before the resist is removed and 1 µm aluminium is sputter deposited (CS 730S, von Ardenne Anlagentechnik GmbH, Germany) on the wafer frontside. Exposed silicon is then DRIE etched using the high etch rate recipe until the wafer is through etched. Using photoresist developer (Microposit 351, Rohm and Haas, Germany) the protective aluminium on the frontside is removed.

Next, the metal heaters on the top wafer frontside are patterned using lift-off. A 6 µm layer of diluted AZ9260 is sprayed on the wafer and patterned using UV lithography before 120 nm aluminium is sputter deposited on the frontside. An ultrasonic acetone bath is used to remove the photoresist and excess aluminium.

To form the pattern for the FMMR expansion slots, the top wafer is again patterned with sprayed AZ9260 and UV lithography. This resist layer will also serve as protection layer during the wafer dicing. For protection during dicing, also the backside wafer is covered with a layer of sprayed resist.

The wafers are diced (DAD 361, Disco Corporation, Japan) and the dies from the top wafer containing FMMR thrusters are sorted out and attached

to a carrier wafer (covered by 1 µm of aluminium) using a 2.8 µm thick layer of Shipley 1813 photoresist which is baked at 90ºC in a oven before being ramped to 120ºC and further baked for 40 minutes (including ramping time). The oxide (including the oxide on the chamber inside) and silicon is plasma and DRIE etched, respectively, to open the expansion slots.

Photoresist is removed from the dice using acetone and ethanol before complete devices are realized by gluing top and bottom dice together using epoxy (Epoxy Rapid, Bostik, Sweden).

CHRACTERIZATION

Fabricated devices are first examined using optical and scanning electron microscope (SEM) imaging.

Using an infrared camera (A40, FLIR Systems, USA) with a macro objective (Close-up lens 18 µm, FLIR Systems, USA), two microreactor devices (top wafers dice only) are examined using thermography while the heaters are powered by a power supply (TTi QL355TP, Thurlby Thandar Instruments, UK), through manual probe heads (PH120, Süss MicroTec, Germany). The supplied voltage is increased from 0 V to 12.5 and 13.5 V for device I and II respectively. At these voltages, it is noticed that the temperature does not reach a steady state, indicating overloading of the heater. At this point, the power supply is switched off. The voltages, currents and measured temperature are logged.

The two devices tested are similar except for two parameters: the oxide frame (the outer oxide area, Fig. 1(a)) surrounding the chamber is 200 µm and 1470 µm wide for device I and II, respectively, and the total heater circuit resistance is 76 and 90 Ω, respectively. The heater resistance itself is, however, equal to 72 Ω in both devices, but device II has longer conductors from the heater to the contact pads. The cubic shaped chamber side lengths are about 500 µm in all directions, and the silicon via on the chamber top is about 260×260 µm in lateral size and about 40-50 µm deep.

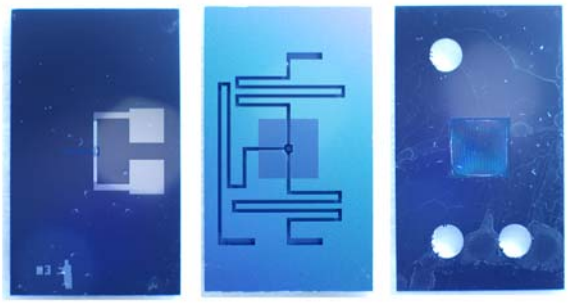

Fig. 2. Overview images of the top chip frontside (left), its backside (middle), and bottom chip frontside (right). On the chip frontside, the metal pattern is visible together with the silicon via surrounded by oxide. The top chip backside shows the channels, chamber and the thick surrounding oxide while in the bottom chip picture, the thick oxide membrane and in- and outlets are visible. The chip size is 1×1.7 cm.

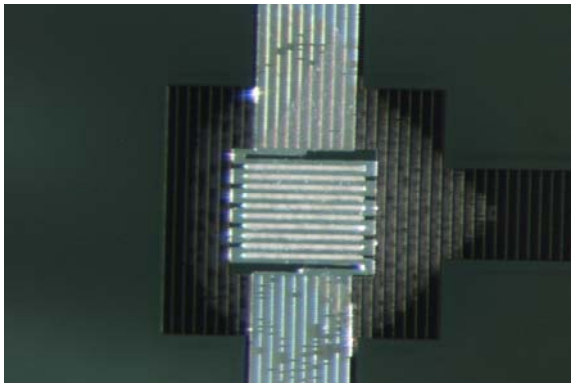

Fig.3. Microscope image of a FMMR chip. The expansion slots, 10 µm wide and 220 µm long, are visible as light rectangles between the heater meander. The light area in the oxide is light going through the thick oxide membrane.

RESULTS

Overview images of the top wafer front- and backsides and the bottom wafer top side are shown in Fig. 2.

Microscope close-up and an SEM image of an FMMR are shown in Fig. 3 and 4, respectively.

Fig. 5 shows an infrared image of device I when heated.The silicon vias' average temperature increase measured with the infrared camera for different input powers (calculated from the logged voltages and currents multiplied) is shown in Fig 6.

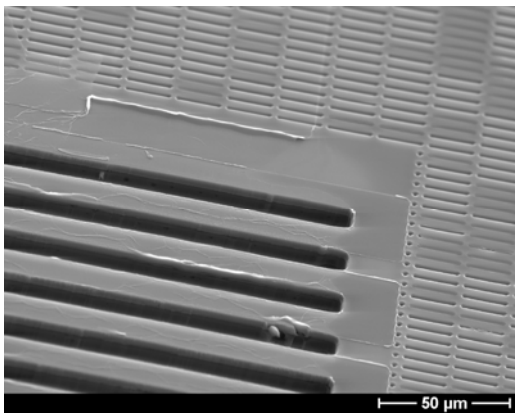

Fig.4. SEM image of the FMMR expansion slots (large openings), surrounded by the aluminium heater and silicon via which is embedded in the thick oxide where the pattern after the etched trenches is still visible.

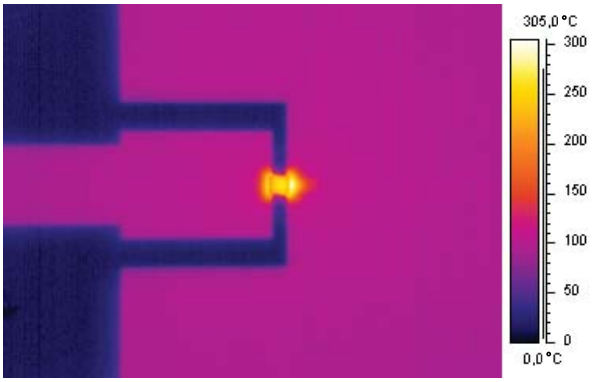

Fig. 5. Infrared image showing the difference in temperature distribution when device I is heated with 1 W and with the heater switched off.

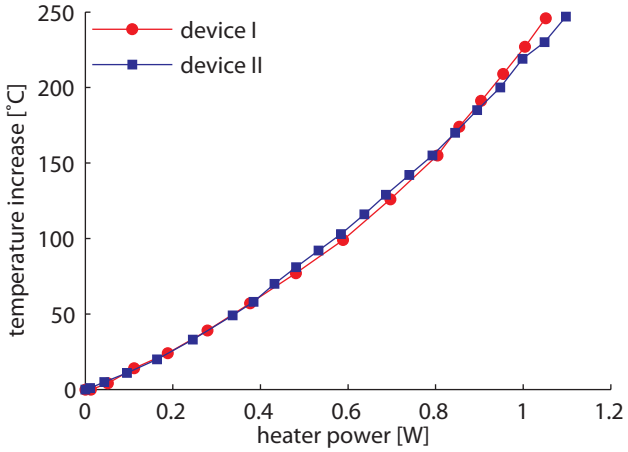

Fig. 6. The temperature increase of the silicon via on top of the chamber for different supplied power level. The temperature is here measured with an infrared camera.

DISCUSSION AND CONSLUSIONS

Microreactors and FMMRs using thick silicon dioxide as heat insulating structures have been fabricated and examined using optical, SEM and infrared imaging.

The devices presented here have been fabricated to confirm process parameters and device design. It is evident that 525 µm thick wafers can not be used since etching of high-aspect-ratio trenches of those depths is very hard, or even impossible. Thinner wafers must be used or even better, instead of using etching through whole wafers, the critical parts, *i.e.* parts containing, or being embedded in, thick oxide could be fabricated in the device layers (with thicknesses of about 50 µm) of two SOI-wafers which are fusion bonded together before the handle layer on one (the top) side is removed to form a top surface close to the chamber. Fluid interfaces and cavities under the chamber could be etched in the bottom wafer handle layer.

With appropriate design, the wafers could be fusion bonded prior to trench-refill oxidation but care has to be taken so that the inner parts are not sealed from the oxygen before being refilled.

Here, aluminium was used for the metal heaters due to the simplicity. In the final devices, platinum or another metal more suitable for high temperatures must be used.

It was found that there were some silicon residues in the thick oxide meaning that, provided that the etch recipe does not change, the mask openings for the trenches should be increased.

The infrared imaging shows that, although well insulated, the power needed to heat the silicon via to a certain temperature is independent of the width of the silicon frame around it. One would expect that more oxide would mean that the heat loss is smaller and hence the power needed would be less. Silicon residue in and under the thick oxide could be the reason why this is not detectable. With an input power of about 1 W, the temperature increase of the silicon via is 250ºC.

The FMMRs have not been fully tested. Using this design it is believed that the power consumption could be kept low, because the heaters would be well isolated. Also, it is possible to fabricate arrays of isolated thruster units on one device where different units could be heated separately. Fig. 7 shows a schlieren image of a prototype from which seven plumes, each from a separate unit, are expelled (but here driven by pressure).

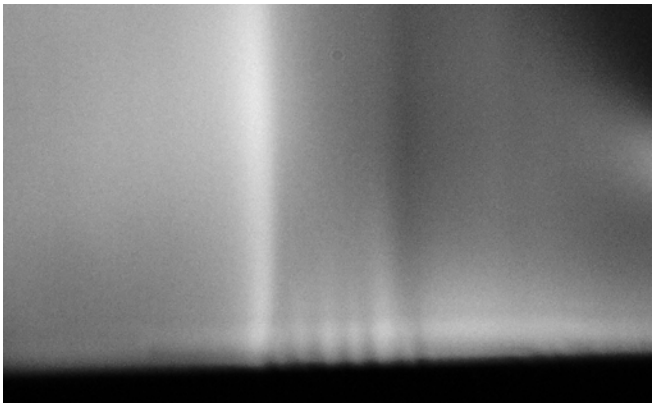

Fig.7. Schlieren image of exhausted gas from a FMMR chip with seven different thruster units expelling pressurized xenon. The distance between the jets furthers to the right and left is about 600 µm.

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