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Towards Solution Processed Electronic Circuits Using Carbon Nanotubes

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Abstract

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Emerging macro- and flexible electronic applications such as foldable displays, artificial skins, and smart textiles grow rapidly into the market. Solution-processed thin-film transistors (TFTs) based on single-walled carbon nanotubes (SWCNTs) as the semiconductor channel can offer high performance, low cost and versatility for macro- and flexible electronics. Major challenges to the development of SWCNT-based TFTs include: (i) hysteresis in their transfer characteristics (TCs), (ii) difficulties in simultaneous achievements of high on-state current I_{on} and large on/off current ratio I_{on}/I_{off}, and (iii) poor uniformity and scalability resulting from the poor solution processability. This thesis aims at developing reliable and simple process techniques for fabrication of the SWCNT-based TFTs that possess the afore-stated characteristics. It presents a systematic investigation to not only explore the fundamental device physics, but also develop novel fabrication methods for enhancement of device performance.

First, issues related to the measurement of gate capacitance (C_g), the determination of current scalability, and the hysteresis in randomly networked SWCNTs are properly addressed. This leads to the establishment of a comprehensive methodology for extraction of carrier mobility (μ) for the SWCNT-based TFTs. In detail, the large hysteresis is effectively suppressed by adopting a pulsed drain current-gate voltage (I_d-V_g) method in which the polarity of the gate pulse was alternating during the measurement. Different from most reported methods in the literature, C_g is accurately determined in our case by performing direct capacitance-voltage measurement on the TFTs.

Second, with the employment of functional composites comprising SWCNTs embedded in a semiconducting polymer, poly-9,9 dioctyl-fluorene-cobithiophene (F8T2), as the semiconducting channel via facile solution processes under ambient conditions, the fabricated TFTs exhibit outstanding electrical performance with: (i) negligible hysteresis, (ii) high μ, (iii) high I_{on} and large I_{on}/I_{off}, (iv) excellent uniformity and dimensional scalability, and (v) good stability. These highly desired performance parameters are achieved owing to an ideal composite structure with metallic SWCNTs being selectively removed and the remaining semiconducting SWCNTs being well wrapped by the polymer matrix.

Finally, the developed TFTs basing on the SWCNT/F8T2 composite are used as the building block to construct some logic circuits. The resultant inverters, NANDs, and NORs are found to retain the small-hysteresis characteristics, with a cut-off frequency reaching 100 kHz. The results presented in this thesis advance the state-of-art SWCNT-based macroelectronics.

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Dedication to
my family

List of Papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I. **On Gate Capacitance of Nanotube Network**
Z Liu, J Li, Z-J Qiu, Z-B Zhang, L-R Zheng, S-L Zhang, IEEE Elec. Dev. Lett, vol. 32, no. 5, pp. 641-643, 2011.

II. **Mobility Extraction for Nanotube TFTs**
Z Liu, Z-J Qiu, Z-B Zhang, L-R Zheng, S-L Zhang, IEEE Elec. Dev. Lett, vol. 32, no. 7, pp. 913-915, 2011.

III. **Solution-Processable Nanotube/Polymer Composite for High-Performance TFTs**
Z Liu, Z-B Zhang, Q Chen, L-R Zheng, S-L Zhang, IEEE Elec. Dev. Lett, vol. 32, no. 8, pp. 1299-1301, 2011.

IV. **Small-Hysteresis Thin-Film Transistors Achieved by Facile Dip-coating of Nanotube/Polymer Composite**
Z Liu, H Li, Z-J Qiu, S-L Zhang, Z-B Zhang, Adv. Mater, vol. 24, pp. 3633-3638, 2012.

V. **Solution-Processed Logic Gates Based On Nanotube/Polymer Composite**
Z Liu, X Gao, Z Zhu, Z Qiu, D Wu, Z-B Zhang, S-L Zhang, Revised submission to IEEE Trans. Electron Device, 2013.

Related Publications

I. **Thin-Film Field-Effect Transistors Based on Composites of Semiconducting Polymer and Carbon Nanotubes**
Z Liu, Z-B Zhang, M Qu, J Li, A Cabezas, L-R Zheng, S-L Zhang, Oral presentation at the 217th Electrochemical Society (ECS) Meeting, Vancouver, Canada, Apr. 25-30, 2010.

II. **Hysteresis-Free Thin-Film Transistors Achieved by Novel Solution-Processing of Nanotube/Polymer Composite**
Z Liu, H Li, Z-J Qiu, L-R Zheng, S-L Zhang, Z-B Zhang, Poster at the Material Research Society (MRS) meeting, San Francisco, USA, Apr 09-13,2012.

III. **Ink-jet printed thin-film transistors with carbon nanotube channels shaped in long strips**
J Li, T Onander, A López Cabezas, B Shao, Z Liu, Z-B Zhang, I Jõgi, X Gao, M Boman, L-R Zheng, M Östling, H-E Nilsson, S-L Zhang, J Appl Phys, vol. 109, no. 8, 084915, 2011.

VI. **Inkjet printing of stripe-featured single-walled carbon nanotube thin film transistors**
J Li, M Qu, Z Liu, A López Cabezas, B Shao, T Unander, Z-J Qiu, Z-B Zhang, J Zhou, Y Huang, L-R Zheng, H-Erik Nilsson, S-L Zhang, Oral presentation in Materials Research Society (MRS) Fall Meeting, Dec. 2, 2009, Boston.

Symbols & Acronyms

C	Total capacitance of the nanotube network
C_A	Accumulation capacitance
C_D	Depletion capacitance
C_Q	Quantum capacitance
C_g	Gate capacitance
C_P	Parallel-plate capacitor
C_{papa}	Parasitic capacitance
d	Nanotube diameter
E_g	Bandgap
f_c	Characteristic frequency
f_m	Measurement frequency
f_T	Cut-off frequency
g_m	Transconductance
I_d	Drain current
I_{dsat}	Drain current in saturation region
I_{on} (I_{off})	On (off) -state current
I_{on}/I_{off}	On/Off current ratio
k	Propagation constant
L	Channel length
L_{nt}	Nanotube length
m	Current exponent
p	Surface coverage
p_c	Percolation threshold
R	Total resistance of the nanotube network
R_c	Contact resistance
t_{off} (t_{on})	Pulse off (on) period
t_{ox}	Gate oxide thickness
V_g	Gate potential
V_g^{max}	Measurement range
V_t	Threshold voltage
V_{in}	Input voltage
V_{out}	Output voltage
V_{dd}	Supply voltage
W	Channel width
Z_0	Characteristic impedance of the nanotube network

α	Attenuation constant
μ	Carrier mobility
ε_0	Vacuum permittivity
ε_{ox}	Relative permittivity of gate oxide
ρ	Nanotube density
ρ_c	Critical nanotube density
w	Angular frequency
ΔV_H	Hysteresis gap
1-D	One-dimensional
2-D	Two-dimensional
AFM	Atomic force microscopy
ALD	Atomic layer deposition
AP	Alternating polarities
APTS	3-aminopropyltriethoxysilane
a-Si	Amorphous-Si
CNT	Carbon nanotube
CP	Conventional pulsed method
C-V	Capacitance-voltage
D	Drain
DGU	Density gradient ultracentrifugation
DS	Drop spacing
EBE	Electron-beam evaporation
F8T2	Poly(9,9-dioctylfluorene-co-bithiophene)
HMDS	Hexamethyldisilazane
IGZO	InGaZnO
MIS	Metal-insulator-semiconductor
m-SWCNT	Metallic single-walled carbon nanotube
OTS	Octadecyltrichlorosilana
P3AT	Poly(3-alkylthiophene)s
PFO	Poly(9,9-dioctylfluorenyl-2,7-diyl)
PMMA	Poly(methyl methacrylate)
RBM	Radial breathing mode
RT	Room temperature
S	Source
SAM	Self assembly monolayer
SDBS	Sodium dodecylbenzene sulphonate
SWCNT	Single-walled carbon nanotube
s-SWCNT	Semiconducting single-walled carbon nanotube
Si-MOSFET	Si metal-oxide-semiconductor field effect transistor
Si≡OH	SiO_2 surface-bonded water molecule
TC	Transfer characteristic
TFT	Thin film transistor
TL	Transmission line
TMA	Trimethylaluminum

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Zhiying Liu
Apr. 2013 Uppsala

Contents

1. Introduction

In parallel with the development of microelectronics technology with more transistors in a smaller area, a new branch of applications that require the electronics to spread over a large area, often referred to as macroelectronics [1], has emerged. The term of macroelectronics is related to flexible electronics since the products can be manufactured on flexible plastics, papers as well as textiles with extraordinary bendability or stretchability. The development of macro- and flexible electronics opens up a large variety of novel applications such as foldable displays [2], printed thin-film solar cells [3], artificial skins [4], solid-state lighting [5], etc, as shown in Fig. 1.1 [6]. Currently, such products grow exponentially to the market. It is estimated by FlexTech that by 2017, the market of macro- and flexible electronics products in total including photovoltaics, OLED, lighting, integrated displays, etc. will exceed $60B annually [6].

For macro- and flexible electronics, mechanical flexibility, portability, and low fabrication cost, instead of high density of high-speed transistors, are the desirable properties. Take displays as an example, thin-film transistors (TFTs) with carrier mobility (μ) around 1 $cm^2V^{-1}s^{-1}$ and dimensions of the order of 10 μm are sufficient [7]. Currently, the state-of-art thin films such as amorphous silicon (a-Si) and polycrystalline silicon (poly-Si) can well fulfill these requirements and have grown into a huge industry. However, large–area displays are still expensive due to the high manufacturing

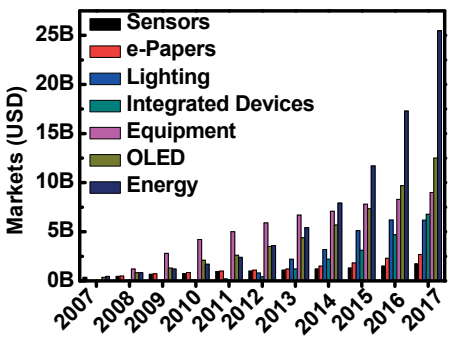

Fig. 1.1 Predicted market growth of macro- and flexible electronics applications [6].

cost caused by the unavoidable sophisticated vacuum processes. Conventionally, Si based devices lack mechanical flexibility unless sophisticated layer transfer technique is utilized [8].

Motivated by their light-weight, flexibility, and multi-functionality, organic materials, such as semiconducting polymers, have attracted special attention. An added advantage with the organic materials is their relative ease in deposition on various substrates through low temperature solution processes [3,9]. The compatibility of organic materials with the newly developed printing techniques such as gravure printing, screen printing, and ink-jet printing on flexible substrates enables the high-throughput, ultra-low cost manufacture of flexible products [2,10,11]. However, those organic materials usually suffer from two shortcomings. One is the inferior μ which is generally lower than that of a-Si. Although the low μ value might still suffice for certain applications, enhancements in μ would facilitate the exploration of a wider range of possibilities [1]. The other challenge is the poor electrical stability under bias stress or in the ambient air, which is represented by threshold voltage (V_t) shift and on-state current (I_{on}) degradation [12,13]. These are severe effects since the devices may fail in operation. It is clear that a new class of materials is necessary to alleviate these restrictions.

Metal oxides, including single metal compounds (*e.g.*, In, Ga, Zn, and Sn) and alloys such as InGaO, ZnSnO, InZnO, and InGaZnO (IGZO) represent a special class of new and attractive TFT materials. Among them, IGZO is particularly interesting since it can offer μ values ranging from 1 to 100 $cm^2V^{-1}s^{-1}$, although it is amorphous rather than polycrystalline [14]. The processing temperature for amorphous IGZO can range from room temperature (RT) up to >300 ^oC. At RT, μ remains higher than 1 $cm^2V^{-1}s^{-1}$, which is of great potential for flexible electronic applications. However, these materials suffer from severe stability issue due to the generation of oxygen vacancies. Typically, they are also rigid mechanically, similar to a-Si films.

Concurrently, carbon nanotubes (CNTs), since the discovery by Iijima in 1991 [15], have gained enormous attention due to their unique structural, mechanical, and electrical properties. A single-walled carbon nanotube (SWCNT) can be viewed as a thin, long and hollow cylinder rolled from a graphene sheet along its circumferential direction, as shown in Fig. 1.2 [16]. The high aspect ratio (length-to-diameter, $>10^3$) and the giant specific surface area (1600 m^2/gram) are critical for chemical and biochemical sensing applications. Mechanically, CNTs possess a Young's modulus at ~1 TPa and a tensile strength about 150 GPa, demonstrating excellent flexibility and robustness. Owing to the molecular homogeneity and quasi one-dimensional (1-D) structure, SWCNTs are expected to exhibit near ballistic transport [17]. In 1998, the first transistor based on an individual SWCNT was fabricated and it was proven with extremely high intrinsic μ (~3000 $cm^2V^{-1}s^{-1}$) and high current-carrying capacity (7000 μA/μm) [18]. Subsequent publications confirmed μ of individual SWCNTs to be in the range of 10^3-10^5 $cm^2V^{-1}s^{-1}$ [19,-

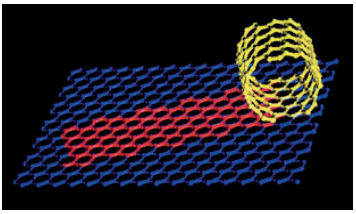

Fig. 1.2 Schematic illustration of an SWCNT rolled from a graphene sheet [16].

20], which exceeds that of most semiconductors and suggests the possibility of SWCNTs in high-speed electronics applications.

When synthesized in a usual way, SWCNTs can be either metallic (m) or semiconducting (s) dependent on a special parameter called chirality. A serious consequence of this uncertainty in electronic properties is a low fabrication yield for transistors since only s-SWCNTs are desired as the channel materials while m-SWCNTs are contaminants. Furthermore, as-grown s-SWCNTs vary in nanotube length (L_{nt}) and diameter (d). The latter property determines the electronic properties especially the bandgap (E_g) following a simple relationship $E_g \sim 1/d$ [17]. It is also difficult to precisely manipulate and translate SWCNTs due to their tiny size. Problems remain in making reproducible devices with uniform transistor performance in terms of I_{on}, on/off current ratio (I_{on}/I_{off}), V_t, etc. As a consequence, in spite of their extraordinary transport properties, electronic products with large amounts of individual-SWCNT transistors are hard to realize.

Random nanotube networks comprising a large quantity of individual SWCNTs have gained particular interest because the electrical characteristics of the resultant TFTs become less dependent on the properties of individual SWCNTs. Performance fluctuation from device to device can thus be significantly reduced. In 2003, the first SWCNT-network TFTs were reported by Snow *et al* through a simple drop casting process and the devices exhibited excellent μ (10 $cm^2V^{-1}s^{-1}$) [21]. Later, the first medium-scale integrated digital circuits fabricated on flexible plastic foil based on SWCNT-network TFTs were realized [22], which has escalated the interests in the CNT technology. SWCNT-network TFTs are particularly attractive for marco- and flexible electronics since low temperature solution-based fabrication approaches can be utilized [23-30]. TABLE 1.1 gives a comparison of the SWCNT-based TFTs with other types of TFT technologies. The SWCNT-network TFTs are considered as one of the most promising candidates for marco- and flexible electronics due to their ease in fabrication and excellence in performance.

TABLE 1.1 Comparison of transistors based on different materials

	Silicon	***a-Si***	***Ploy-Si***	***Organic***	***Metal oxides***	***SWCNTs***
Substrate	Rigid*	Rigid*	Rigid*	Flexible	Rigid/ Flexible	Flexible
Process	Litho-graphy	Vacuum	Vacuum	Solution	Sputtering	Solution
Process T (^{o}C)	High	150-350	250-550	Low	RT->400	Low
Cost	High	High	High	Low	Variant	Low
Mobility (cm^2/Vs)	400-1500	<1	30->100	10^{-5}-10	1-100	10-100
Stability	Good	Poor	Poor	Poor	Poor	Good

* It is possible to transfer devices from rigid substrates to flexible foils by the techniques developed in [8].

Despite the tremendous progress in the SWCNT-based TFTs, several important issues still await proper addressing. This includes both unveiling the underlying device physics and enhancing the device performance. For the SWCNT-network TFTs, the carrier transport is usually described by the conventional models developed for Si metal-oxide-semiconductor field effect transistors (Si-MOSFETs). It is noted that, unlike Si-MOSFETs, the electrical property of the SWCNT networks is dominated by the two-dimensional (2-D) percolation pathways through the nanotube sticks from the source (S) to the drain (D) terminals [20,31,32]. The conventional models for Si-MOSFETs are unable to accurately describe the behaviors of the SWCNT networks [33,34]. One example is that the reported μ values for the SWCNT networks extracted using the commonly used method show a large variation. This variation is closely related to the percolation geometrical parameters unique for the SWCNT networks including nanotube density ρ (μm^{-2}), L_{nt}, and channel length L [18,35,36]. Moreover, the gate capacitance (C_g) of the nanotube networks cannot be simplified by a parallel-plate capacitor (C_P) due to the inhomogeneity of the percolating network [21,23,37,38]. Particularly for low density nanotube networks, C_g can be seriously overestimated by using C_P, leading to an erroneous estimate of μ. A systematic investigation and a comprehensive understanding of the physics of the percolation transport dominated nanotube networks are necessary.

On the other hand, to improve the electrical performance of the SWCNT-network TFTs, a number of challenges must be overcome. The most prominent issues are: (1) poor solution processability of SWCNTs, leading to a poor fabrication yield and inferior device performance of the resultant TFTs [21]; (2) coexistence of s-SWCNTs and m-SWCNTs, resulting in difficulties

in simultaneous achievement of high I_{on} and large I_{on}/I_{off} [21,23,33,39]; and (3) huge hysteresis exhibited in the current-voltage characteristics of typical SWCNT-based TFTs due to the charging/discharging between SWCNTs and their surroundings [40,41].

It is well-known that pristine SWCNTs are difficult to be individually dissolved in most commonly used solvents. Nanotubes tend to aggregate forming bundles due to the strong van der Waals interactions. Nanotube aggregation poses a serious hindrance to the development of solution processable TFTs. To debundle and disperse SWCNTs, a range of methods have been proposed and evaluated. They include high-concentration surfactant solutions such as sodium dodecyl sulphate [42] and the superior sodium dodecylbenzene sulphonate (SDBS) [43], DNA wrapping [25,44], and polymer wrapping such as poly(9,9-dioctylfluorenyl-2,7-diyl) (PFO) [45,46] and recently reported regioregular poly(3-alkylthiophene)s (P3AT) [47]. Among these schemes, an air-stable fluorene based polymer, poly(9,9-dioctylfluorene-co-bithiophene) (F8T2), has been proven of having strong interactions with SWCNTs and capable of solubilizing SWCNTs efficiently [48]. Therefore, the combination of polymer and SWCNTs, yielding nanotube/polymer composites, is extremely interesting for solution processing of the SWCNTs.

Additionally, ordinarily synthesized SWCNTs are a mixture of m- and s-SWCNTs: about 33% metallic and 67% semiconducting. In order to attain a large I_{on}/I_{off}, the density of SWCNTs in the network must be in an appropriate range where the s-SWCNTs percolate but the m-SWCNTs do not [39]. However, low-density networks usually lead to low I_{on}. The difficulty in simultaneously achieving high I_{on} and large I_{on}/I_{off} sets a severe restriction on the application of such devices. Various approaches have been proposed to eliminate the m-SWCNT paths including selective synthesis [49], electrical breakdown [50], gas-phase reaction [51], selective chemical functionalization [52], lithography-assisted stripping [22], filtration to obtain y-junctions [53], dielectrophoresis [54], DNA [44] or agarose gel-assisted [55] separation, and density gradient ultracentrifugation (DGU) [56]. However, most of the methods either add difficulties in fabrication processes or lack repeatability in device performance. Recent studies suggest that, polymers, such as PFO [45] and P3AT [47], can effectively remove m-SWCNTs by centrifugation due to selective interactions and preferential binding of certain SWCNT structures by the polymer macromolecules. Hence, the use of nanotube/polymer composites may lead to s-SWCNT-enriched materials, which is essential for logic circuit applications.

Furthermore, SWCNT-TFTs are frequently characterized by huge hysteresis in their transfer characteristics (TCs), which is represented by a giant V_t shift back and forth when the gate potential (V_g) is swept forwardly and reversely. The presence of hysteresis complicates the understanding of device physics, *e.g.*, it defeats the ordinary procedures for μ extraction. It also

results in unstable operation of the TFTs, which is unacceptable in practical applications. This phenomenon is generally attributed to charging/discharging of the SWCNTs through their interactions with the surroundings, *e.g.*, water molecules bound on the SiO_2 surface [41,57-60] and H_2O/O_2 in the atmosphere [41,60,61]. To combat this issue, pulsed I_d-V_g methods are proposed to effectively suppress the trapping/detrapping during the measurement [62-64]. In practice, reduction of hysteresis has been realized via various methods such as SiO_2 surface treatment [65], suspension of the SWCNTs [66], adoption of high capacitance gate dielectric [67], passivation by organic [41,60] or inorganic materials [67], and so forth. However, all these treatments require sophisticated and expensive process conditions such as vacuum processing. An inexpensive and simple route towards hysteresis-free SWCNT-based TFTs is in strong demand.

This thesis aims to develop reliable techniques for SWCNT-based TFTs through solution processes that can offer the desired performance with (i) small hysteresis, (ii) high I_{on} and large I_{on}/I_{off}, and (iii) excellent uniformity and dimensional scalability. A strong focus is placed on understanding of the fundamental device physics. It is hoped that working on these two aspects in parallel will lead to generation of knowledge regarding electrical behavior and fabrication techniques for nanotube/nanowire-based novel devices. The thesis is structured as follows:

Chapter 2 discusses the architectures and device physics related to the SWCNT-network TFTs. Specifically, hysteresis phenomenon in nanotube based TFTs is described.

Chapter 3 details the experimental approaches regarding the preparation of SWCNT suspensions, solution processing of the devices as well as the electrical characterization techniques. Particularly, a standard procedure to extract μ of the nanotube TFTs is established upon a proper treatment of all the challenges. In detail, C_g of the SWCNT-networks is determined by conducting direct capacitance-voltage (C-V) measurements on the TFTs. Hysteresis is suppressed by the adoption of a pulsed I_d-V_g method with gate pulses of alternating polarities (AP).

Chapter 4 describes the electrical performance of the solution processed nanotube network TFTs in terms of hysteresis suppression, I_{on} rise and I_{on}/I_{off} increase, stability, uniformity and scalability improvements. The mechanisms underlying the performance enhancements are unveiled. Finally, representative logic circuits are demonstrated based on the developed nanotube/polymer TFTs.

Chapter 5 summarizes the appended publications by also revealing the close connections among them.

Finally, Chapter 6 concludes the whole thesis and also suggests future research directions.

2. Fundamentals

2.1 Thin-film transistor (TFT) architectures

In conventional Si-MOSFETs, the gate (G) electrodes are at the surface of the devices. In contrast, the majority of SWCNT-TFTs adopt a bottom-gate configuration, in which the S/D electrodes and the semiconductor channel appear at the top of the device (Fig. 2.1(a) and (b)). This design is a natural choice for a-Si TFTs in display applications since the S/D electrodes can directly contact with the pads of the pixels. It is also an obvious choice for various sensors because the functional parts, typically the semiconductor channel, can be exposed directly to the sensing targets. Moreover, this configuration is simpler to fabricate since the SWCNT networks can be dispersed or directly grown on the insulator.

A common-gate configuration that all the designed TFTs share one gate electrode, as shown in Fig. 2.1(a), is widely used to demonstrate the concept of SWCNT-TFTs. This is mainly due to the convenience in device manufacturing. However, it is not appropriate in practice since those TFTs cannot be controlled individually to properly perform a circuitry function. Local-gate TFTs that each transistor is controlled by its own gate electrode, as displayed in Fig. 2.1(b), are therefore necessary.

Interestingly, there are few publications discussing the top-gate TFTs until recently [67,68]. In top-gate structures, the gate insulator and gate electrode are deposited on top of the semiconductor channel, as shown in Fig. 2.1(c). Recently, it is reported the dielectric layer on top of the SWCNT channel not only serves as a qualified gate insulator, but also generates an effective passivation layer for the devices [67]. Yet, it is challenging to grow insulators on top of the SWCNTs since the electronic properties of both parties, *i.e.*, insulators and SWCNTs, might be severely affected by the subsequent processes [69]. In general, it is hard to assure whether bottom-gate or top-gate is the better structure to choose. In this thesis, back-gate structures are adopted for all the SWCNT-TFTs under investigation.

The structures of the TFTs are usually optimized when engineering on the device performance. One example is the self-aligned structure which has been well established in Si technology [70]. With this structure, the overlap between the G and S/D electrodes can be ignored, leading to minimal parasitic capacitance (C_{papa}). As a consequence, the working frequency of the devices will be significantly enhanced, as will be discussed later.

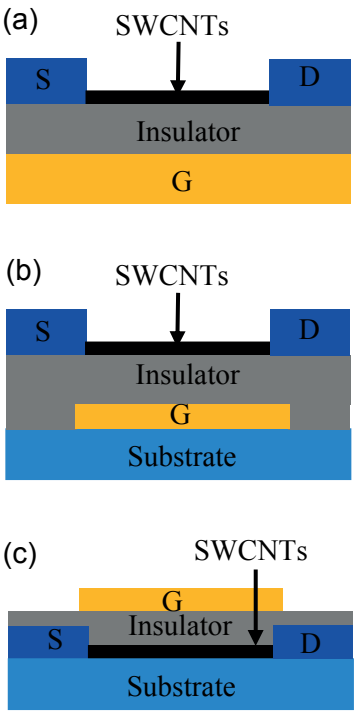

Fig. 2.1 Schematic representations for (a)-(b) bottom- and (c) top-gate SWCNT-TFTs, with (a) common- and (b) individual-gate configurations.

2.2 Percolation transport in nanotube networks

In an individual nanotube, if the charge transport is ballistic and the tube has perfect contacts, the conductance of the quasi 1-D nanotube is $4e^2/h$ (155 μS), corresponding to a resistance of 6.5 kΩ [15]. In devices, electrical contacts to an s-SWCNT are non-ideal and it leads to an additional contact resistance R_c. R_c frequently dominates the device performance because of the formation of Schottky barriers at the interface between the metal electrodes and the s-SWCNT. A series of experiments have clarified the importance of Schottky barriers in SWCNT transistors [18-20]. Javey *et al* reported a near Ohmic contact between Pd electrodes and large diameter SWCNTs (>2 nm) and ballistic SWCNT-FETs with hole mobility as high as 4000 $cm^2V^{-1}s^{-1}$ [19].

Although individual nanotubes have shown extraordinary μ, devices based on single SWCNTs are difficult to manufacture and reproduce. An alternative solution is to use a large number of SWCNTs to form the channel of a TFT. This design works well especially for marcoelectronics since the TFT dimensions are usually much larger than the size of an SWCNT. In this

case, the device performance mainly depends on the collaborative and statistical distribution of the SWCNTs instead of the property of a single tube. A viable approach is to use aligned SWCNTs which are located in parallel in the channel [33,71]. However, alignment of SWCNTs requires sophisticated processes and the yield of the devices is low. As an alternative, random networks of SWCNTs, which comprise a large quantity of tubes with random orientations, are relatively easier to produce by direct growth on substrates or dispersion from solutions.

In a 2-D random SWCNT network, each tube can be treated as a rigid stick with a fixed length L_{nt}. The sticks are oriented randomly in a rectangular channel with length L and width W. For a large-area TFT with $L>>L_{nt}$ and when ρ is low, the SWCNTs can only be treated as isolated "islands" in the channel region. There is no conduction pathway and the network is insulating. The SWCNT sticks start to interconnect with one other and form continuous pathways when ρ increases above the critical density ρ_c being determined by $\rho_c=4.23^2/\pi L_{nt}^2$ [31-33]. A continuous increase in ρ leads to more percolation paths and increase in the conductance.

In an SWCNT-network TFT, the carriers percolate from S to D through one or more percolating paths. Each percolating pathway consists of several sticks and the intersections between adjacent sticks. In this case, the electron transport from one stick to the adjacent one is rate-limiting in conductance instead of the charge transport in an individual tube. The drain current (I_d) of the TFTs depends on the average path length ($>L$) and the total number of paths available for conduction. Therefore, increasing ρ and reducing the tube-to-tube contact resistance are two essential solutions to enhancing I_{on}. Previous studies have shown that m- (s-) SWCNTs conduct well to other m- (s-) SWCNTs, but the m-to-s contacts cause a huge resistance due to the Schottky barrier at the interface [72]. As a consequence, the conductance of the percolating networks is dominated by the tube-tube interjunctions. It is natural to treat the percolating nanotube networks as a transmission line (TL). The TL model is described in Appendix A.

It is also worth mentioning that the percolation behavior of SWCNT networks is complicated by the coexistence of m- and s-SWCNTs. In high-density SWCNT networks where a high I_{on} is obtained, the majority of the SWCNTs percolate including the undesired m-SWCNT pathways, leading to a significant degradation in I_{on}/I_{off}. In contrast, low-density networks can avoid the contamination of the m-SWCNTs and ensure a relative large I_{on}/I_{off}. However, I_{on} is generally low due to the limited number of percolation paths. Thus, it is difficult to achieve both high I_{on} and large I_{on}/I_{off} in the presence contaminating m-SWCNTs. This sets one of the major obstacles for SWCNT-TFTs. By carefully tailoring the shape of the networks, for example, long strips [20] or Y-junction long nanotubes [46], higher I_{on}/I_{off} can be obtained with a network of relatively denser SWCNTs. However, the most effective method is to increase the fraction of s-SWCNTs. Theoretical

calculations indicate that I_{on}/I_{off} can be immune to the presence of m-SWCNTs when the fraction of s-SWCNTs exceeds 90% [39].

2.3 Electrical characteristics of SWCNT-network TFTs

From the "top-down" view

At present, the electrical models of Si-MOSFETs are widely used for describing the operation of TFTs and analyzing the carrier transport in the devices. Similar to organic TFTs [6], the I_d-V_g behavior of the SWCNT-network TFTs can be modeled by a traditional "top-down" approach in which the network is treated as a homogeneous bulk material. In this model, the TFTs turn on when V_g is higher than V_t. At low drain bias (V_d<V_g-V_t), a linear region exists in which I_d is dependent on V_d and the DC behavior can be described by,

$$I_d = \mu C_g \frac{W}{L}(V_g - V_t)V_d \tag{2.1}$$

I_d saturates at higher V_d ($V_d \geqslant V_g$-V_t) and it can be represented by,

$$I_{dsat} = \mu C_g \frac{W}{2L}(V_g - V_t)^2 \tag{2.2}$$

From the "bottom-up" view

The classical model simplified in equations (2.1) and (2.2) usually focuses on uniform materials and indicates a current scaling relationship in form of $I_d \propto 1/L$. However, the percolating SWCNT networks are inhomogeneous in terms of L_{nt}, L, and ρ, indicating the inadequacy of using these equations to model the TFT behaviors or estimate the device performance. As shown Fig. 2.2(a), for a network with a certain ρ, only the SWCNTs lying in the percolation paths (yellow dotted lines) contribute to I_d, while the SWCNTs not in the percolation paths are inactive to current conduction. When L is reduced by a factor of n (n>1), the original SWCNTs taking part in percolation are still conductive and contribute to a current of nI_d. Meanwhile, part of the SWCNTs that were isolated previously may now become part of the bridge between S and D as shown in Fig. 2.2(b) (the red dashed line), and thus contribute to an additional current ΔI_d. The total current will therefore be higher than nI_d. In other words, the traditional electrical model from the "top-down" view is inadequate in analyzing a 2-D nanotube network. Instead, a "bottom-up" approach that takes the percolation geometry of the nanotube networks into consideration is proposed and developed [31,34]. In this model, the stick percolating networks satisfy the following finite-size scaling relationship [34],

$$I_{\mathrm{d}} = \frac{A}{L_{\mathrm{nt}}}\xi\left(\frac{L_{\mathrm{nt}}}{L}, \rho L_{\mathrm{nt}}^2\right) \times f\left(V_{\mathrm{g}}, V_{\mathrm{d}}\right) \tag{2.3}$$

where the proportionally constant A depends on C_{g}, tube diameter d, and stick–stick interaction parameter. Function ξ represents the geometrical contribution with parameters L_{nt}, L, and ρ while function f is more of the electrical contribution including the effects of V_{g} and V_{d}. It is found that equation (2.3) is universal for arbitrary geometrical and biasing conditions.

For long channel TFTs with $L \gg L_{\mathrm{nt}}$, the carriers travel through the intersects of nanotubes and diffusive transport dominates. The electrical contribution function f can be expressed by,

$$f\left(V_{\mathrm{g}}, V_{\mathrm{d}}\right) = \left(V_{\mathrm{g}} - V_{\mathrm{t}}\right)V_{\mathrm{d}} - \beta V_{\mathrm{d}}^{\ 2} \tag{2.4}$$

where β=0.5. And the geometrical scaling function ξ is,

$$\xi\left(\frac{L_{\mathrm{nt}}}{L}, \rho L_{\mathrm{nt}}^2\right) = \left(\frac{L_{\mathrm{nt}}}{L}\right)^{m\left(\rho L_{\mathrm{nt}}^2\right)} \tag{2.5}$$

where m is the current scaling exponent which only depends on the network coverage p. Here, $p=\rho L_{\mathrm{nt}}^2$. m decreases monotonically with increasing p. The simulation results [33] show that for high coverage networks (*e.g.*, $p \geqslant 19$), ξ approaches the classical limit with m=1. For a sparser network with p near the percolation threshold $p_{\mathrm{c}}=4.236^2/\pi \approx 5.7$ [31], $m \gg 1$.

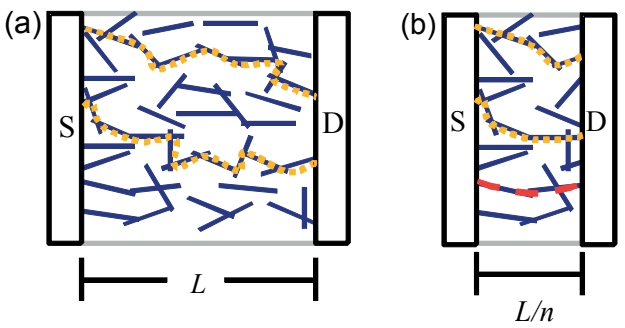

Fig. 2.2 (a) A percolating SWCNT network with channel length of L. The yellow dotted lines represent two percolation pathways. (b) When L is reduced to L/n, an additional percolation path occurs as indicated by the red dashed line.

2.4 Hysteresis in SWCNT-based TFTs

Hysteresis appears as a result of V_t variation with the range, speed, and direction of V_g sweep (Fig. 2.3 (a)). It is unfortunately a commonly observed phenomenon in SWCNT-based transistors [40,41]. This phenomenon was also frequently observed in the Si/SiO_2 system in the early days of Si-MOSFETs primarily induced by the presence of mobile ionic charges like Na^+, Li^+, K^+, and H^+ in the gate dielectric (*i.e.*, SiO_2) [74]. It led to delay of the practical application of Si-MOSFETs. Hysteresis can be effectively developed into memory devices [40]. But in most other cases, even a small degree of hysteresis is detrimental and hence unwanted. Thus, it is a critical parameter although much less discussed compared with other issues such as μ.

In SWCNT-based transistors, hysteresis is observed in both individual tube and network devices. Recently, more focus has been put to unveil the underlying mechanisms [41,57-61]. The reported sources of hysteresis in the literature can be summarized in Fig. 2.3(b): (A1) oxide trapped charges (holes or electrons), (A2) mobile oxide charges (ionic impurities) [74], (B1) interface traps between the SWCNT channel and the gate insulator, including the well-discussed and widely-accepted oxide surface bound -OH groups [41,57-60], and (B2) environmental adsorbents particularly H_2O and O_2 molecules [41,60,61].

Particularly, for TFTs with SiO_2 as the gate insulator, hysteresis of the SWCNT-based transistors primarily originates from mechanisms B1 and B2. The SiO_2 surface-bound water molecules (Si≡OH) serve as electron traps at the interface. The charging/discharging of these traps by carriers in the

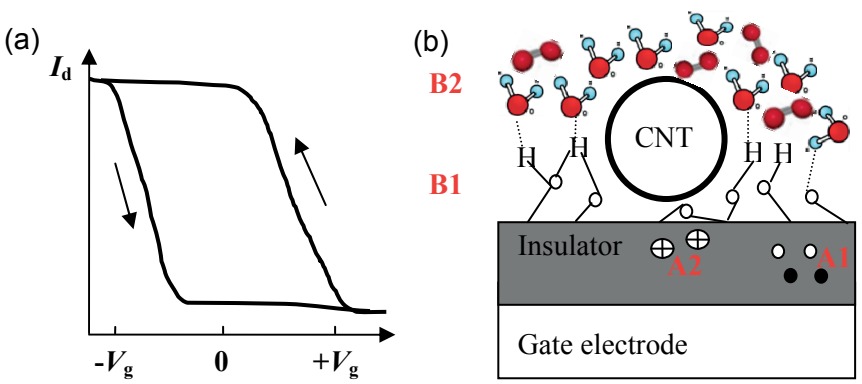

Fig. 2.3 (a) Schematic TCs and (b) sources of hysteresis for the SWCNT-based transistors.

channel region electrostatically modulates the SWCNTs, thereby changing the current level of the devices. Initially in the off-to-on (reverse) sweep where V_g is positive, electrons are trapped by those Si≡OH groups. When V_g sweeps toward negative direction, more holes are attracted to balance the virtual gate induced by the trapped charges. These excess holes result in an increased I_d. In contrast, the on-to-off (forward) sweep starts with a negative V_g and the trapped electrons are emptied quickly. Thus, a lower I_d is observed when V_g sweeps form negative to positive (Fig. 2.3(a)). The physisorbed H_2O/O_2 molecules around the SWCNTs severely influence the density of the Si≡OH groups [60,61] and therefore the degree of hysteresis in the devices. This explains why hysteresis is more pronounced in a humid environment [75].

To suppress hysteresis, annealing the samples under vacuum can reduce the density of water molecules [41]. Surface treatment with hydrophobic self-assembly monolayers (SAMs) such as octadecyltrichlorosilana (OTS) [65] or dielectrics, *e.g.*, divinyltetramethyl siloxanebis-(benzocyclobutene) derivative [58], would lead to an –OH free surface. Suspending the SWCNTs can avoid the interface with SiO_2. Other methods including encapsulation with poly(methyl methacrylate) (PMMA) [41] or Methylsiloxane [60] could effectively passivate the surrounded trap sites.

3. Experimental Approaches

3.1 Dispersion of nanotubes in solution

The basic requirement for solution process is a stable solution or suspension of the electronic materials. In our experiments, dissolving nanotubes by surfactant and polymer wrapping are the two methods investigated to prepare the SWCNT suspensions.

3.1.1 Surfactant aided solubilization

The hydrophobicity of the SWCNT surface can be altered via surface wrapping by surfactants such as SDBS. The SDBS molecule comprises two parts with one terminal being hydrophobic (-CH3) and the other hydrophilic. The strong interaction between the benzene ring in the SDBS molecule and the sp^2 hybridization structure of the SWCNTs enables the wrapping of the surface of SWCNTs. Meanwhile, the hydrophilic terminals provide steric repulsion on the SWCNTs and effectively stabilize them in the solvent.

To prepare a water-based SWCNT suspension, as received HipCo SWCNTs from Unidym (average diameter 1.1 nm) were bath-ultrasonically added into de-ionized water containing 1 wt.% SDBS followed by tip-sonication. Then, the suspension was centrifuged at 16000 g overnight. The upper 70% of the supernatant was carefully collected for TFT fabrication. This method is widely used in the research community and further developed by multiple DGU steps to separate the m- and s-SWCNTs in solution [56].

However, it is noted that the surfactants contain a great deal of impurities, *e.g.*, Na^+. The utilization of high-power sonication also creates defects in C-C bonds as well as trims the tubes into short segments. Consequently, the electronic properties of the SWCNTs are adversely affected, which is undesired for TFT applications. Dispersion of SWCNTs without degradation of the material is in strong demand.

3.1.2 Polymer aided solubilization

A number of polymers have been identified to assist dispersion of SWCNTs in various media [45-48]. In contrast to the surfactant method that all the tubes are coated, polymer macromolecules usually preferentially wrap a certain type of nanotubes with certain diameters or chirality. Hence, highly

selective solubilization can be achieved. An air-stable aromatic polymer, F8T2, is selected in our work to disperse the SWCNTs. The F8T2 molecules contain fluorene rings in the backbones which are close to the surface structure of SWCNTs. The strong π-π stacking between SWCNTs and the polymer can enable a good wrapping outcome. Experimentally, around 2–3 mg as received HiPco-SWCNTs were ultrasonically added into a 50-mL F8T2 solution in toluene (0.2 mg/mL). Then, the mixture was utilized for device fabrication by simple dilution. Alternatively, it was centrifuged at 13300 g for 60 min and the supernatant was used as the starting material for device manufacturing.

3.2 TFT fabrication

3.2.1 Substrate preparation

Common back-gate structure

As described in Section 2.1, the common back-gate configuration (Fig. 2.1(a)) is the most convenient structure for testing the electrical behavior of new semiconducting materials. The process flow to fabricate the TFTs is schematically illustrated in Fig. 3.1. It started with heavily n-type doped Si wafers as the substrate as well as the gate electrode. Then, a thermally grown 150-nm SiO_2 layer served as the gate insulator. Afterwards, the SiO_2 surface was functionalized by a Hexamethyldisilazane (HMDS) SAM layer by loading the whole wafer into an oven at 110 °C for 30 min, which is commonly used in Si-technology for improving the adhesion of photoresist during lithography processing. In CNT technology, the surface functionalization can be also achieved by utilizing 3-aminopropyltriethoxysilane (APTS), that is believed to significantly enhance the adhesion of SWCNTs [76]. To coat a monolayer of APTS, the whole wafer was immersed into 1 mL APTS in Chloroform for 30 minutes followed by baking at 110 °C for 10 minutes. After that, the S and D electrodes comprising a bi-layer of 35-nm Pd on top of 5-nm Ti were defined by electron-beam evaporation (EBE) followed by a standard lift-off procedure. The gap between the S and D electrodes, *i.e.*, *L*, was varied from 5 to 200 μm. The channel area was then opened in a newly coated 1.2-μm-thick photoresist layer. Then the substrate is ready for the formulation of the channel material to bridge the gaps between S and D.

Local back-gate structure

The structure of an individual back-gate TFT was designed as shown in Fig. 2.1(b). Metal islands consisting of a tri-layer metal stack, *i.e.*, 1-nm Al/40-nm Au/10-nm Ti, serving as individual back-gate electrodes, were grown on SiO_2 by combining EBE with lift-off. The thin Al film was easily oxidized in the presence of O_2, serving as the nucleation layer for the subsequent growth

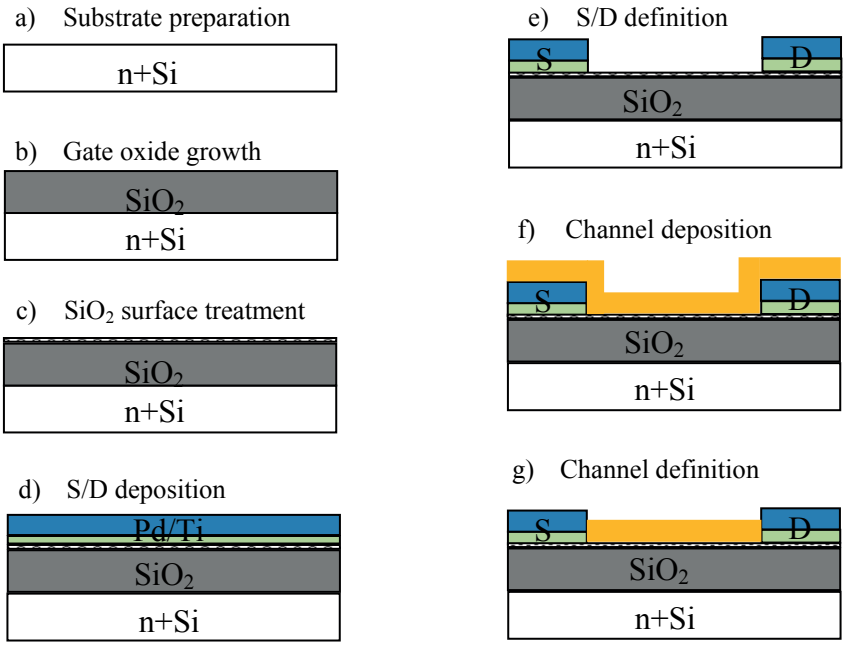

Fig. 3.1 Schematic representation of the fabrication process for a common back-gate SWCNT-based TFT.

of gate dielectric by means of the atomic layer deposition (ALD) process [77]. A 10-nm thick ALD AlO_x was grown at 300 ^oC using trimethylaluminum (TMA) and H_2O as the reaction precursors. Similar to the TFTs with the SiO_2 gate insulator, the AlO_x surface was functionalized with HMDS followed by the construction of the S/D electrodes. Finally, the channel area was opened in a newly coated photoresist layer

3.2.2 Channel formation

Drop casting of aqueous solution

By simple drop-casting to deposit the SWCNT aqueous solution on top of the chips with pre-defined S/D electrode pairs, SWCNT random networks were obtained. After water evaporation and removal of photoresist in Acetone, SWCNT network channels were formed and TFT fabrication completed.

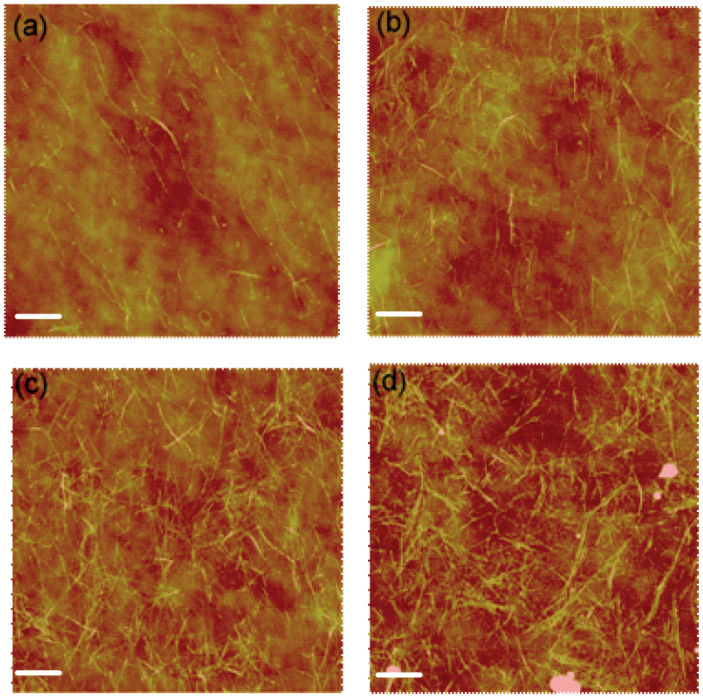

Fig. 3.2 AFM images of SWCNT networks with different *p*: (a) 1.8, (b) 6.5, (c) 9.9, and (d) 16.6. The scale bars are 1 μm.

SWCNT networks with various nanotube densities imaged by means of atomic force microscopy (AFM) are shown in Fig. 3.2. The surface coverage *p* of the networks was obtained by counting the number of the SWCNTs in the images and measuring the length of the tubes. Obviously, when *p* is low (1.8) as shown in Fig. 3.2(a), nanotubes are isolated from each other. With increasing *p* (6.5 in (b)), SWCNTs contact with each other and percolation pathways eventually form in the channel region. Further increase of *p* (9.9 in (c)) leads to more percolation routes. When the density of SWCNTs is high, as shown in Fig. 3.2(d) with p=16.6, the SWCNTs start to agglomerate. Although the drop-casting method is extremely simple, it lacks repeatability and is of low yield due to the poor controllability. In our experiments, the best yield for the conducting TFTs is around 70% but the devices show unacceptable performance variations.

Spin-/dip-coating of nanotube/polymer composites

Both spin- and dip-coating methods are widely used in organic device fabrications. Compared with drop casting, these two methods are more controllable. During spin-coating, an excess amount of SWCNT/F8T2 solution is

placed on the substrate surface. The substrate wafer is then set to rotate at high speed in order to spread the fluid by the centrifugal force. The morphology of the thin film formed is strongly dependent on the spin speed and duration. For instance, spin-coating the SWCNT/F8T2 mixture at 2000 rpm (revolutions per minute) for 30 sec typically results in 10-20 nm thick composite films. Extremely thin films, assumed to be monolayer, could be obtained by further increasing the spin speed. With spin-coating, the yield for conducting devices can approach 100%.

Dip-coating provides an alternative route for depositing uniform thin films. Recently, it has been shown that higher μ can be achieved if the organic film is deposited by dip-coating instead of spin-coating [78]. In our experiments, the chip was simply immersed in the SWCNT/F8T2 composite solution (the supernatant after centrifugation) and kept stewing for 5-10 hours in ambient conditions. It was then pulled out from the solution carefully to avoid jitters. The composite deposited itself on the substrate. SWCNT/F8T2-TFTs with both SiO_2 and AlO_x as gate insulator were successfully fabricated by such a facile dip-coating process. Compared with the SWCNT/F8T2-TFTs fabricated by spin-coating, dip-coating provides comparatively thicker composite films and better surface coverage in the channel. This feature renders outstanding device performance in terms of hysteresis elimination, I_{on} increase, as well as uniformity improvement, as will be discussed in Chapter 4.

Inkjet printing of the composites

By an additional step of filtration with a membrane of pores 0.2 mm in diameter for the SWCNT/F8T2 mixture, we have performed inkjet printing of the composite solution on a Dimatix desktop inkjet printer [79]. As shown in Fig. 3.3(a), the drops of the SWCNT/F8T2 composite are jetted at a uniform velocity of 5 m/s, implying a proper viscosity and surface tension of the composite solution.

In printing electronics, the desired printed lines would be smooth, even, narrow, and straight. However, the printing process itself is dependent on a range of parameters such as substrate temperatures, drop frequencies, and drop spacing (DS) [80]. In Fig. 3.3(b), by carefully tailoring DS during parameter optimization, various line morphologies on SiO_2 substrate are obtained. When DS is as small as 20 μm, discreet bulges along the line length separated by segments of uniform narrow lines are observed. This can be attributed to the outflow of the additional fluid during printing. With increasing DS, the bulges become narrower. This tendency persists until DS is reduced to 55 μm where a smooth and straight track is obtained. These lines have uniform smooth edges and tops, along with the narrowest width of $\sim$ 60 μm. With a further decreased DS, for instance, at 60 μm, the drops are too far to interact with each other, leading to islands in the patterns.

Subsequently, inkjet-printed SWCNT/F8T2 TFTs were fabricated with heavily doped n^+-Si as the gate electrode and 150 nm SiO_2 as the gate insulator. The S/D electrodes were inkjet-printed using a commercial available Cabot CCI-300 conductive ink containing 19-21 % weight of nano-silver particles. The topview image by AFM of the composite film beside one of the Ag electrode is shown in Fig. 3.3(c). It is found that the long, curved SWCNTs are lying in the matrix of F8T2. Although the concentration of the nanotubes in the thin film is so low that the SWCNTs are non-percolated, I_{on} of the TFTs is still enhanced due to the presence of the highly conductive SWCNTs embedded in the polymer matrix [84]. In Fig. 3.3(d), TC of an inkjet-printed SWCNT/F8T2-TFT with L=60 μm and W=100 μm is depicted. I_{on}, extracted at V_g=-40 V and V_d=-2 V is about 40 nA. Meanwhile, $I_{on}/I_{off}>10^5$ is achieved, which has the potential for logic circuit applications. It is expected that further optimization on the formulation of the composite ink would lead to continuous improvements of the electrical performance.

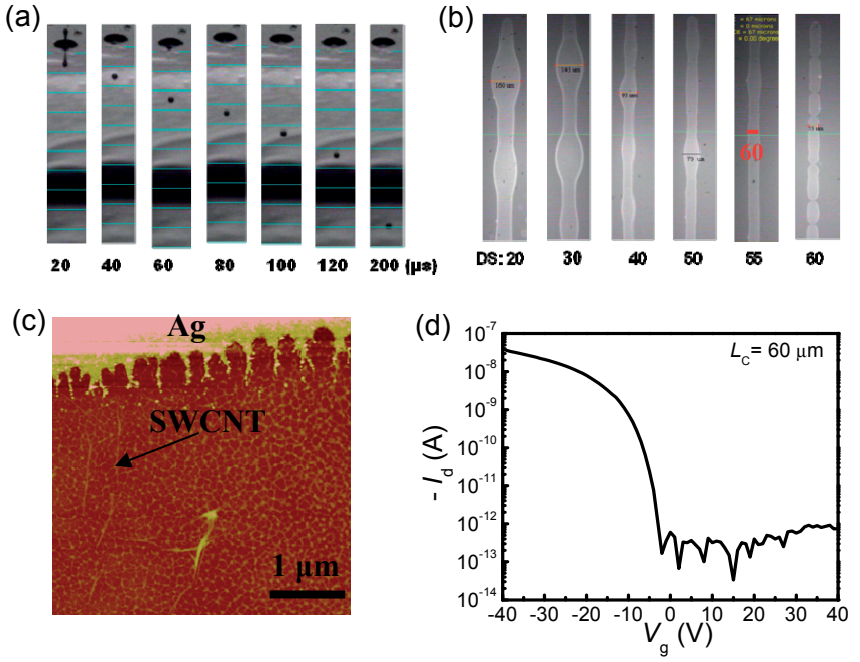

Fig. 3.3 (a) Optical image of the SWCNT/F8T2 drops during jetting process. (b) Line patterns of the SWCNT/F8T2 composite with various drop spacings. (c) An AFM image in height mode of an inkjet-printed SWCNT/F8T2 composite film. (d) A TC of an inkjet-printed SWCNT/F8T2-TFT with V_g scanned from −40 to +40 V and V_d fixed at -2 V. W and L of the TFTs were 60 and 100 μm, respectively.

3.3 Electrical characterizations

3.3.1 Hysteresis suppression by pulsed I_d-V_g method

The TCs of the SWCNT-based TFTs were characterized through a semiconductor analyzer (Agilent 4156C or Keithley 4200SCS). In conventional I_d-V_g measurement, V_g is continuously swept step by step as shown in Fig. 3.4(a). At each step, the bias is held for a certain period of time to ensure an accurate measurement, particularly for small current. In the presence of charging/discharging effects with a time constant comparable with the measurement time, the trapped charges can serve as an additional virtual gate that modulates the carriers in the channel region. In a DC sweep, the charges remain trapped until the gate polarity is switched, thereby leading to the widely observed hysteresis in the TCs of the SWCNT-TFTs. Fig. 3.4(b) presents the I_d-V_g characterization results of an SWCNT-network TFT with p=6.5 in DC mode. When V_g is swept forwardly and reversely, a huge gap is observed. The hysteresis gap can be defined by $\Delta V_H=V_t^r-V_t^f$ with V_t^r and V_t^f the V_t values obtained from the reverse and forward TCs. Obviously, ΔV_H increases continuously with increasing the measurement range (V_g^{max}) and reaches about 56 V at V_g^{max}=40 V.

A conventional pulsed (CP) I_d-V_g measurement method was conducted by measuring I_d at each data point for a dwell time of t_{on} followed by a period during which V_g returned to zero (t_{off}), as indicated in Fig. 3.4(c). The trapped charges could effectively relax when V_g bias was removed. Thus, ΔV_H was significantly reduced. A shorter t_{on} and longer t_{off} is expected to lead to smaller ΔV_H. In 2006, Lin, *et al* reported that pulsed measurements with a time constant below 500 μs provided reproducible TCs of TFTs based on individual SWCNTs [85]. Later, small ΔV_H was obtained for SWCNT transistors by applying pulsed I_d-V_g measurements with t_{off} as long as 10 sec in vacuum [62]. As shown in Fig. 3.4(d), much narrower gaps were obtained by CP method compared with DC. As expected, smaller ΔV_H is observed with longer t_{off}. It is reported that the characteristic time constant for charge detrapping is around 8 s [63]. In Fig. 3.4(d), it is found that ΔV_H drops to about 6 V for V_g^{max}=40 V with t_{off} =60 s. However, the residual ΔV_H is rather persistent and difficult to be completely eliminated in ambient, indicating that V_g pulses of the same polarity still cause the charge accumulation during a sweep loop.

Alternatively, a pulsed sweep method by using gate pulses of alternating polarities (AP) as shown in Fig. 3.4(e) was introduced to suppress hysteresis [64]. In this method, a negative pulse is applied followed by a positive one of the same amplitude and duration. The charge trapped in the positive pulse could now be driven out in the followed negative one. Thus, the hysteresis can be effectively suppressed. As shown in Fig. 3.4(f), hysteresis-free TCs can indeed be obtained when the AP method is applied. With AP method, all

the TCs merge and can be recognized as the intrinsic property of the TFTs. Moreover, this method is extremely interesting since it avoids the requirements of expensive fast instruments or long waiting time as is necessary for the CP method. In **Paper II**, similar results were obtained with an SWCNT-network TFT with p=9.9.

It is worth mentioning that those pulsed V_g methods can be also transferred to C-V measurements in order to suppress the hysteresis presented in C-V curves (see Section 3.3.2).

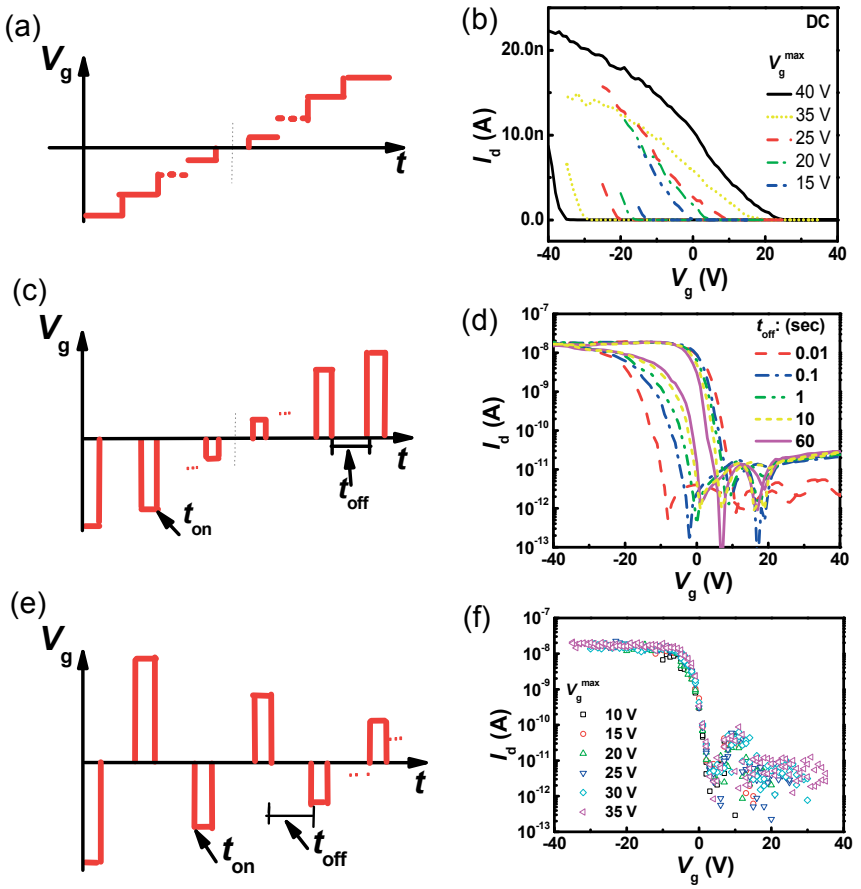

Fig. 3.4 Sketches for I_d-V_g measurements and TCs for an SWCNT-TFT with p=6.5 in (a, b) DC, (c, d) CP, and (e, f) AP modes, respectively. For all the measurements, V_d=-1 V.

3.3.2 Gate capacitance (C_g) of networked nanotubes

Gate capacitance C_g is a crucial parameter for transistors since it is the measure of gate control over the channel conductance as well as the basis to extract μ and estimate the transient behavior of devices and integrated circuits. An accurate determination of C_g is of paramount importance for SWCNT-TFTs as well. In early studies, C_g of the SWCNT-network TFTs is approximated by the capacitance of a parallel-plate system, C_P, which is simply determined by $C_P=\varepsilon_0\varepsilon_{ox}/t_{ox}$ with t_{ox} as the gate oxide thickness, ε_0 and ε_{ox} the relative permittivity of the gate insulator and the permittivity in vacuum [81]. However, unlike Si-MOSFETs in which the semiconducting channel is homogeneous, the conduction of the nanotube networks is determined by the stick-percolation which depends strongly on the geometrical parameters [31-34] as discussed extensively earlier. Thus, use of C_P can lead to an erroneous estimation of C_g. More rigorously, C_g of the nanotube networks can be calculated by examining the metal-insulator-semiconductor (MIS) capacitor with consideration of the electrostatic coupling between the nanotubes [37,38], which leads to an analytical expression for calculation of C_g [38],

$$C_g = \left\{ C_Q^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_{ox}} \ln\left[\frac{\Lambda_0}{R_{nt}} \frac{\sinh(2\pi t_{ox}/\Lambda_0)}{\pi}\right] \right\}^{-1} \Lambda_0^{-1} \qquad (3.1)$$

where C_Q=4.0 X 10^{-12} F/cm is the quantum capacitance of the nanotubes [82], $1/\Lambda_0$ is the nanotube density (μm^{-1}) in the network , and R_{nt} is the radius of the tubes. This model was widely adopted in the literatures thereafter [24-28,53]. However, complications arise since the calculated C_g value is very sensitive to R and $1/\Lambda_0$ used in equation (3.1). But they are both difficult to quantify for a random network with large amounts of nanotubes.

Experimentally, the capacitance of an individual SWCNT was measured in 2006 by directly performing *C-V* measurements on a top-gated FET configuration with a single nanotube as the conduction channel [83]. For SWCNT networks, the measurement of C_g is still controversial. To characterize C_g of the SWCNT-network TFTs, Cao *et al.* executed *C-V* measurements on a dish-shaped MIS capacitor formed by gold, HfO_2, and SWCNT networks, giving rise to a measured C_g being about one third of the capacitance of the HfO_2 [22].

For a percolating network, only those nanotubes in the percolation pathways contribute to the current conduction. It is therefore natural to suggest that C_g only takes the contributions of the percolated SWCNTs into account. However, the measurement on a MIS structure includes those SWCNTs that do NOT contribute to the current conduction, consequently leading to an overestimation of C_g. A direct *C-V* measurement on the TFT configuration provides a more sensible and accurate determination of C_g of the nanotube

networks [29]. The *C-V* measurement setup for this novel measurement arrangement on the SWCNT-network TFTs with its equivalent circuit is illustrated in Fig. 3.5. The G electrode of the TFT is connected to the CV-High terminal while the S and D are both connected to the CV-Low terminal of the LCR meter (HP4284A from Agilent), as shown in Fig. 3.5(a). During *C-V* measurements, a small AC signal at a measurement frequency of f_m is superimposed to the DC bias V_g. The parasitic capacitance, mainly originated from the overlap between G and S/D electrodes, can be determined by measuring on the TFT structure without any nanotubes in the channel. Then, the capacitance of the SWCNTs can be calculated by subtracting the parasitic capacitance from the total capacitance measured from the TFTs (cf. Fig. 3.5(b)).

With the consideration of the percolation behavior and the measured capacitance by the direct *C-V* measurement on TFT configurations, the nanotubes in the percolating network can be divided into 3 categories as depicted in Fig. 3.5(a): (i) percolated nanotubes (black solid lines) that contribute to both conductance and capacitance; (ii) isolated nanotubes (blue dashed lines) lying in the channel region by themselves that contribute to neither capacitance nor conductance; and (iii) non-percolated tubes but connected with the S/D electrodes or the percolation pathways that contribute to capacitance but not to conductance.

Cleary, MIS structures include all the 3 classes of nanotubes, which would overestimate C_g. The measured capacitance through direct *C-V* measurements on TFTs solely contains type (i) and (iii). The isolated ones (type (ii)) are effectively excluded. This is more accurate compared to the MIS

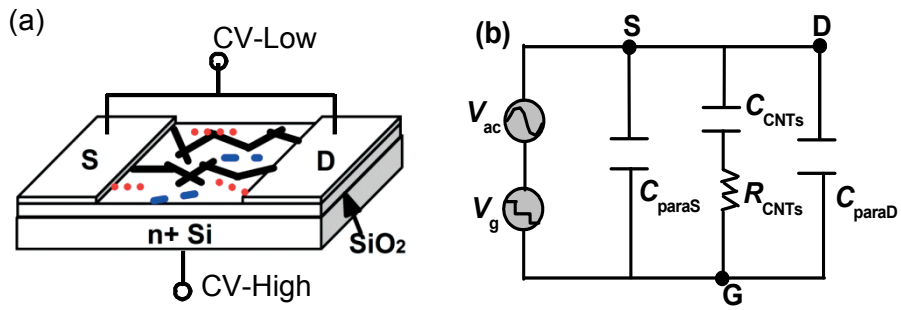

Fig. 3.5 (a) Sketch of the *C-V* measurement setup on an SWCNT-network TFT. The stick percolation network consists of (i) percolated tubes (black solid lines), (ii) isolated tubes (blue broken lines), and (iii) tubes connected to the S/D electrodes or the percolating pathways but non-percolated (red dotted lines). (b) Equivalent circuit of the *C-V* measurement arrangement.

structures. Moreover, the Monte Carlo simulation shows that the non- percolated nanotubes (type (iii)) are insignificant for the total amount of the SWCNTs (**Paper I**). Thus, a more reliable measurement of C_g is established.

Dependence of C_g on measurement frequency

In **Paper I**, *C-V* measurements were performed directly on SWCNT-network TFTs at different f_m. A consistent tendency is found that the accumulation capacitance C_A (extracted at V_g=−40 V) stays constant at low f_m and starts to drop over a critical frequency f_c. In addition, the frequency dispersion of the measured capacitance is quantitatively analyzed by the RC TL model described in Appendix A. The good agreement of the measured f_c values with the ones calculated from equation (A.8) confirms the validity of the TL model. Therefore, C_g of the SWCNT-network TFTs can be effectively extracted in the low frequency region where no TL effect occurs.

For SWCNT-network TFTs, the channel resistance in the depletion region R_{off} is much higher than that in the accumulation region R_{on}. According to the TL model, $f_c \propto R^{-1}$. It is expected that f_c for depletion capacitance C_D is much lower than that for C_A. Fig. 3.6(a) shows the frequency response of C_D (extracted at V_g=+40 V) for TFTs with p=9.9 and 16.4. It is found that f_c is ~5 kHz for C_D when p=16.4, which is significantly lower than that of C_A (~80 kHz, in **Paper I**). Similar result is found for C_D and C_A of the TFT with p=9.9. Hence, a larger difference in C_A and C_D of a device with the 150-nm-thick SiO_2 gate insulator is found in **Paper I** compared with a device with a 30-nm-thick SiO_2 gate insulator [84]. The green dotted line has a decaying slope of -1/2, implying the validity of the TL effect once again.

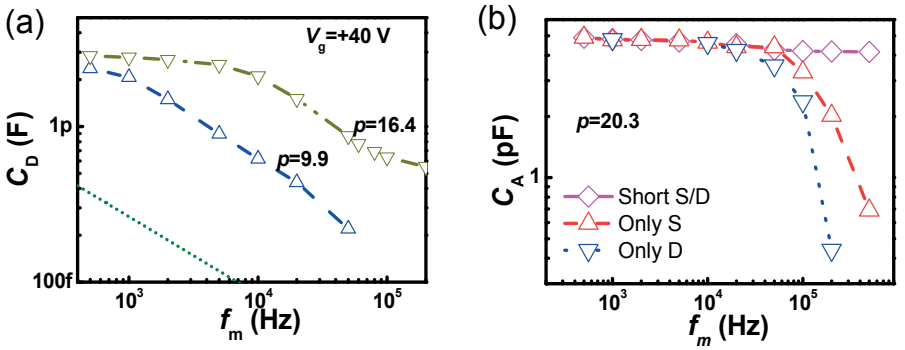

Fig. 3.6 (a) C_D (extracted at V_g=+40 V) as a function of f_m for the TFTs with p=9.9 and 16.4. (b) C_A as a function of f_m for the TFTs with p=20.3 with different connection setups.

As discussed in **Paper I**, the root of TL effect is carrier injection from the electrodes to the nanotubes in the channel region. Once there is nanotubes have connections with electrodes, TL effect exists. We have further tested the frequency response of a TFT (p=20.3) with V_g applied between G and only S (D) electrode, with D (S) floating, as shown in Fig. 3.6(b). It can be seen that with only S (D) setup, the capacitance also possesses frequency response with a lower f_c.

Dependence of C_g on nanotube density

Intuitively, the capacitance of the percolating networks increases with increasing nanotube density. Theoretical calculations indicate that the increase of C_g with ρ continues until the distance between the nanotubes is approximately the same as the thickness of the gate insulator [21]. In **Paper I**, C_g is more accurately obtained through direct C-V measurements in the region of $f_m<f_c$ in order to avoid the TL effects. Fig. 3.7 shows the measured C_g with different nanotube densities. It is clear that a higher C_g is obtained for devices with a denser network (denoted as red rectangular). It is also observed that C_g extracted with the absence of the TL effect is considerably smaller than C_P (denoted by blue dashed line in Fig. 3.7). Furthermore, compared with C_g calculated using equation (3.1), the measured C_g is even higher. This is attributed to the difficulties in determining the geometrical parameters in equation (3.1). The effective area of the SWCNT networks, evaluated by C_g/C_P, approaches 1 for a sufficiently dense film. In this region, the utilization of an MIS structure is a proper simplification. While for a film with low-density nanotubes, $C_g/C_P<1$ and the extracted mobility via C_P would be severely underestimated.

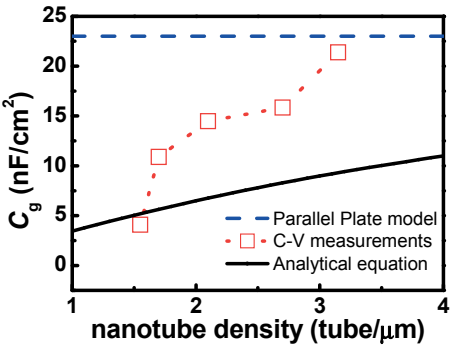

Fig. 3.7 C_g of the SWCNT-network TFTs as a function of nanotube density. C_g obtained from C_P (blue dashed line), equation (3.1) (black solid line), and direct C-V measurements (red rectangular) are included for comparison.

3.4 Mobility (μ) extraction

Carrier mobility μ is one of the most important indicators of device performance. μ of the SWCNT-network TFTs could be extracted by referring to the traditional model for Si-MOSFETs expressed in equation (2.1), as many did in earlier days of nanotube research [81]. However, it has been found that the reported μ values for the SWCNT-based TFTs suffer from huge variations, leading to the great difficulties in making a sensible assessment within the research communities [18,35,36]. Surprisingly, the variations are not only dependent on process differences but also the geometrical parameters such as L, ρ, and L_{nt}.

In general, the challenges in μ extraction involve the following aspects. Firstly, the effective C_g of a stick-percolating network is lower than C_P, particularly for low-density nanotube networks (Section 3.3.2). Secondly, the transport of SWCNT-network TFTs scarcely satisfies the relation $I_d \propto 1/L$ (Section 2.3). Thirdly, TCs of SWCNT-network TFTs frequently suffer from substantial hysteresis (Sections 2.4 and 3.3.2). Therefore, a new procedure to extract μ by addressing all these challenges is necessary.

3.4.1 Dependence of μ on hysteresis

The validity of μ extraction by equation (2.1) is based on the assumption that the transconductance g_m can be unambiguously determined. Since g_m is the first derivative of the I_d-V_g curve, V_t should not be related to V_g. In Fig. 3.4(b), it is obvious that V_t^f extracted from the TCs in DC mode increases with increasing V_g^{max}. The opposite is true for V_t^r as it decreases with increasing V_g^{max}. An invariant V_t, *i.e.*, a hysteresis-free I_d-V_g characteristics is essential for the extraction of μ. This issue has been, unfortunately, undermined in a large number of publications that have made direct extraction of μ without clarifying their sweep conditions.

TABLE 3.1 summarizes the g_m values for our SWCNT-network TFTs

TABLE 3.1 g_m values for SWCNT network TFTs with different p

p	g_m^f (nS) by DC[a]	g_m^r (nS) by DC[a]	g_m^f (nS) by CP[a]	g_m^r (nS) by CP	g_m (nS) by AP
5.4	0.38	0.20	0.21	0.36	0.33
6.5	1.95	0.96	1.08	1.85	1.50
9.9	27.7	13.6	16.2	24.8	20.3
16.4	64.3	28.5	35.2	57.5	50.3
20.3	120	74.5	80.5	108.0	113

[a] g_m^f and g_m^r is extracted from the TC curves with V_g^{max}=30 V in DC and CP modes, respectively.

with different p, extracted using the TC curves obtained in DC, CP and AP modes. With DC method, it can be found that g_m values vary by a factor of 2-3 when V_g is swept forwardly and reversely. This large discrepancy can lead to erroneous interpretations. With reference to the AP results, the forward DC sweep results in an overestimate of g_m (μ) while the the reverse one gives rise to an underestimate. When CP method was employed where a much smaller ΔV_H was obtained, it was expected that the discrepancy would be much smaller. But in TABLE 3.1, it is found that the variation of g_m is only slightly smaller compared with that obtained from DC method, confirming the great importance of hysteresis-free TCs in μ extraction. The adoption of AP method has resulted in hysteresis-free TCs, and thus consistent g_m values. Therefore, the g_m values extracted by the AP method is considered representative of the intrinsic device property, which is the starting point for a reliable determination of μ.

3.4.2 Dependence of μ on C_g

Since μ is inversely proportional to C_g, the determination of C_g is one of the most important steps for extraction of μ. For the SWCNT-network TFTs, the majority of the publications use C_g values calculated from either C_P or the more rigorous cylindrical model presented by equation (3.1). Obviously, utilization of C_P underestimates μ by the ratio C_P/C_g. For the calculated C_g according to equation (3.1), μ can be either underestimated or overestimated due to the lack of accuracy in determining percolation geometrical parameters. In contrast, C_g through a direct C-V measurement can be straightforwardly utilized in the extraction owing to its accuracy.

It is expected from Fig. 3.7 that, for the low-density networks where C_g/C_P is small, μ is severely underestimated by C_P. When p increases, C_g/C_P approaches 1 and the use of C_P for μ extraction is a proper approximation. This is an important advance towards an accurate extraction of μ for the SWCNT-network TFTs.

3.4.3 Dependence of μ on current scaling behavior

In Si-MOSFETs, $I_d \propto 1/L$. By considering the percolation geometry of the nanotube networks, a more universal model presented by equations (2.3)-(2.5) has been proposed as discussed in Section 2.3. According to this model, μ can be represented by,

$$\mu = \frac{1}{\frac{W}{L_{nt}}\left(\frac{L_{nt}}{L}\right)^m} \frac{g_m}{C_g V_d} \tag{3.2}$$

For high-density SWCNT networks with m=1, μ is consistent with that extracted from the standard method for Si-MOSFETs. While for low-density SWCNT networks, m increases rapidly with decreasing p since the non-percolated SWCNTs in long-channel TFTs can become conductive when L is reduced. In this case, μ can be underestimated by a factor of $(L/L_{nt})^{m-1}$ if the standard method for Si-MOSFETs is employed. The underestimation of μ is severe particularly for a large system with $L>>L_{nt}$.

Starting with the hysteresis-free TCs, μ of the SWCNT networks can be well estimated by combining the directly measured C_g with the appropriately considered m. A geometrical parameter independent μ is obtained and this result is involved in **Paper II**. The extraction method allows for a reliable evaluation of electrical performance for SWCNT-based TFTs.

4. Carbon Nanotube TFTs and Circuits

4.1 Development of solution processing technology

The stable nanotube/polymer composite solution prepared (see Section 3.1) possesses excellent solubility of individual s-SWCNTs, which is ideal for achieving devices with good gating behavior (**Papers III-V**). Fig. 4.1(a) shows the optical image of a SWCNT/F8T2 composite solution after centrifugation, which is stable for months when stored in ambient conditions. The UV-Vis-NIR absorption spectrum of the SWCNT/F8T2 composite solution before and after centrifugation are compared in Fig. 4.1(b). Obviously, significantly sharp and much better resolved absorption peaks are observed for the SWCNT/F8T2 solution after centrifugation in the wavelength range of 600-1600 nm. The peaks are labelled as S_{11} and S_{22}, representing the first and the second optical transitions of the s-SWCNTs. This can be attributed to a higher ratio of individual SWCNTs in the SWCNT/F8T2 solution after removing the large bundles by the centrifugal forces [86]. For the SWCNT/F8T2 solution, peaks corresponding to m-SWCNTs (in the region of 400-600 nm) can unfortunately not be distinguished due to the huge F8T2 asorption background in the same region. Therefore, we turned to another characterization technique, Raman spectroscopy.

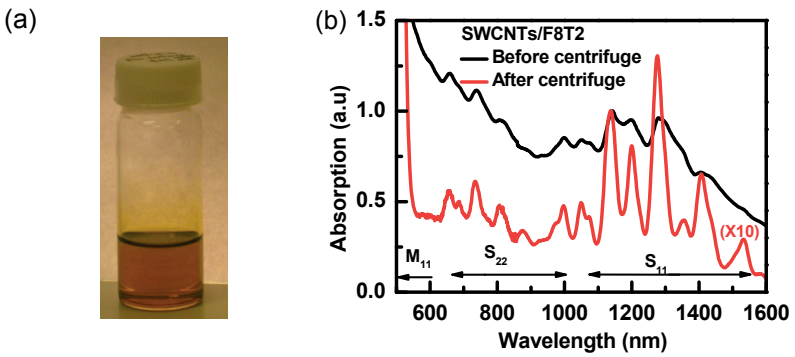

Fig. 4.1 (a) Optical image of the SWCNT/F8T2 composite solution after centrifugation. (b) Absorbance spectra for the SWCNT/F8T2 composite solution before and after centrifugation process.

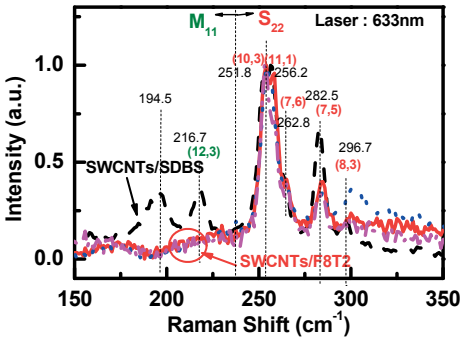

Fig. 4.2 RBM spectra at 633 nm for thin films prepared by SWCNTs/F8T2 at 3 different locations with reference to that prepared by SWCNTs/SDBS.

To characterize s- and m-SWCNTs in the composite films, Raman spectroscopy was employed. Generally, with Raman spectroscopy one measures the energy shift of photons resulting from generation or annihilation that are elastic in a sample. It can provide information about phonon structure, electronic structure and defects. In CNTs, the phonon energy corresponding to the so-called radial breathing mode (RBM), in which the circumference expands and contracts, is inversely proportional to the CNT diameter. Laser excitation at different wavelengths brings nanotubes of different diameters into resonance [15]. Here, Raman spectroscopy with a laser wavelength at 633 nm was employed for the SWCNT/F8T2 composite films and the results of randomly selected 3 locations are shown in Fig. 4.2. For reference, the Raman data for the SWCNT/SDBS films are displayed as well. With the 633 nm wavelength, it is found that the two m-SWCNT peaks at 195 and 217 cm^{-1} are absent, suggesting a substantially decreased fraction of the m-SWCNTs in the SWCNT/F8T2 composite solution after centrifugation [15]. The Raman characterization results provided strong evidence for the removal of m-SWCNTs in the composites. A composite material enriched with individual s-SWCNTs is essential for fabrication of high performance TFTs.

4.2 Hysteresis suppression

Through simple solution processes such as spin-coating or dip-coating, TFTs based on the SWCNT/F8T2 composite (SWCNT/F8T2-TFTs) were fabricated. In **Paper IV**, we have found that the hysteresis behavior of the TFTs is closely related with the surface morphology of the composite films in the channel. The SWCNT/F8T2-TFTs prepared by dip-coating with a relatively long soaking time (5 hours) display a negligibly small hysteresis when V_g is

swept forwardly and reversely. This is remarkable since huge hysteresis is frequently observed for SWCNT-based TFTs [40,41]. Correspondingly, a high density of SWCNTs is found to be embedded in the polymer matrix, indicating a good protection of the SWCNTs by F8T2. In contrast, the SWCNT/F8T2-TFTs manufactured by spin-coating show an unacceptably hysteresis behavior (*i.e.*, ΔV_H=28 V). This huge hysteresis is also observed for the TFTs in **Paper III** and could be effectively eliminated by I_d-V_g measurements in AP mode. By examining the surface morphology of the spin-coated thin film, it is found that the majority of the SWCNTs are directly contacting with SiO_2 or the atmosphere.

We have further examined the TCs as well as the surface morphology for the SWCNT/F8T2-TFTs prepared by dip-coating with reduced soaking time (a few minutes). Islands of composite films formulate in the channel region within which only part of the SWCNTs is embedded in the polymer matrix as shown in Fig. 4.3(a). The rest of the SWCNTs are directly exposed to the SiO_2 surface or the ambient air (inset of Fig. 4.3(a)). With such films, ΔV_H was typically around 6 V for $|V_g^{max}|$=20 V, cf. Fig. 4.3(b). This value is larger than the near zero ΔV_H obtained from the SWCNT/F8T2-TFTs for a longer soaking period, but it is significantly reduced compared to that of the compo site devices manufactured by spin-coating. Therefore, a strong correlation between ΔV_H and the degree of the protection of SWCNTs by F8T2 in the composite films is established with a smaller ΔV_H for a better protection.

For the mechanism of hysteresis suppression in the dip-coated SWCNT/F8T2-TFTs, it is likely that the SWCNTs are wrapped by F8T2 to certain thickness. Thus, the SWCNT/SiO_2 and SWCNT/atmosphere interfaces have been effectively isolated by the hydrophobic polymer. The

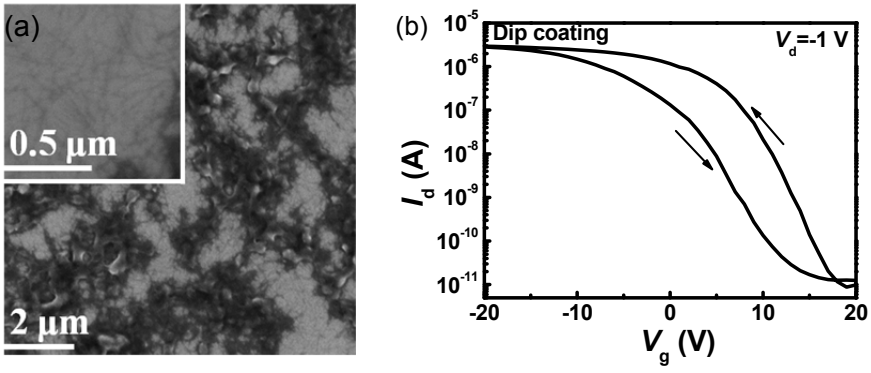

Fig. 4.3 (a) SEM images and (b) TCs of the SWCNT/F8T2-TFTs fabricated by dip-coating in a short duration. For the TFT, L=50 µm and W=100 µm.

presence of polymer at these interfaces can serve as an electron barrier to tunneling from the SWCNTs to the nearby trap sites [58]. Consequently, hysteresis for the SWCNT/F8T2-TFTs is effectively eliminated.

Chun, *et al.* suggested that the use of an appropriate hydroxyl-free gate dielectric could effectively passivate the electron traps present on the SiO_2 surface [58]. This is further supported by Aguirre *et al.* in their study on the chemical nature of substrates and the switching behavior of the SWCNT-based TFTs [61]. In our TFTs, the SiO_2 surface was treated with siloxane-terminated SAM of HMDS. It is likely that the traps appearing around the SWCNTs, such as the Si≡OH groups, would be passivated by the hydrophobic SAM layer since such a SAM can provide a tunneling barrier to the trap sites. This idea finds experimental proof in reference [65] in which hysteresis-free TCs were obtained for SWCNT-TFTs on an OTS treated SiO_2. However, in our experiments, huge hysteresis was found to persist for the spin-coated SWCNT/F8T2-TFTs although the SiO_2 surface was similarly coated with an HMDS SAM. This immediately suggests that HMDS is not critical for the hysteresis suppression due to the fact that traps around the SWCNTs cannot be completely passivated by the siloxane-terminated SAM [58].

To further prove the effect of the SAM of HMDS, we have fabricated SWCNT/F8T2-TFTs on bare SiO_2 (without HMDS) by the identical dip-coating process as those small hysteresis devices. This was achieved by removing the HMDS by means of oxygen plasma which is a standard procedure in silicon technology. The TCs obtained using the same measurement settings as in **Paper IV** , *i.e.*, $|V_{gmax}|$=20 V and V_d=-1V, are shown in Fig. 4.4. It clearly shows that even without HMDS, ΔV_H of the dip-coated SWCNT/F8T2-TFT is about 3 V. Although this value is slightly larger than what is obtained for the dip-coated SWCNT/F8T2-TFTs in the presence of HMDS, it is much smaller than ΔV_H of the spin-coated composites devices. This result confirms that HMDS is NOT a key factor for the hysteresis reduction. The slightly smaller ΔV_H obtained from the dip-coated SWCNT/F8T2-TFTs on SiO_2/HMDS might be resulted from the hydrophobicity of SiO_2/HMDS which facilitates a better self-assembly of the hydrophobic SWCNT/F8T2 composite film.

We also fabricated individual bottom-gate SWCNT/F8T2-TFTs with a 10-nm thick AlO_x layer grown by ALD as the gate insulator (**Paper V**). Similar to the TFTs on SiO_2, dip-coating and spin-coating were used to form the composite channel. For dip-coating, a comparatively longer soaking time (overnight) was utilized. TCs of SWCNT/F8T2-TFTs prepared by dip- coating is again negligible while it is unacceptable large for the spin-coated one, similar to those for the TFTs with SiO_2 as the gate insulator. In these devices, the capacitance for the thin AlO_x layer is about 619 nFcm^{-2}, which is considerably higher than that for the 150 nm SiO_2 which is 23 nFcm^{-2}. In

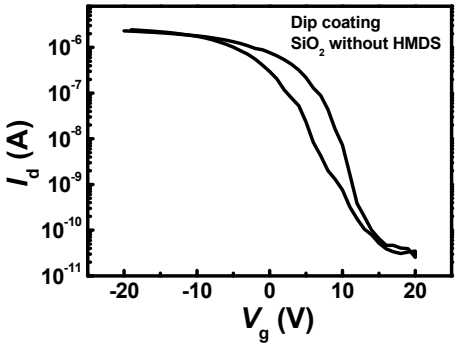

Fig. 4.4 TCs of a dip-coated SWCNT/F8T2-TFT on bare SiO_2. V_d was fixed at -1 V.

agreement with device physics, it has been shown that use of a high- capacitance gate insulator leads to a much smaller ΔV_H [36,67,68]. However, ΔV_H remains large for the spin-coated devices, indicating the presence of large amounts of trap sites on AlO_x (**Paper V**). This is in accordance with the reported water adsorption on an AlO_x surface [69].

To conclude, the absence of substantial hysteresis with the dip-coated SWCNT/F8T2-TFTs is independent of the pretreatment of the SiO_2 surface or type of the gate insulator (SiO_2 versus Al_2O_3). It is exclusively attributed to the isolation of the SWCNTs by the F8T2 matrix from the trap sites on the surface of gate insulator and H_2O/O_2 molecules in the atmosphere. It further confirms the effectiveness of the hysteresis suppression through the formation of a nanotube/polymer composite. Compared with the other reported methods for hysteresis reduction that often require deposition of additional layers or handling in inert/vacuum environments [41,60,65-67], the present method is simple, robust, solution processable, and operational under ambient conditions.

4.3 Switch performances

Theoretically, the decease of the m-SWCNT fraction in the percolation dominated networks leads to a substantially decreased probability of m-SWCNT pathways [33,39]. Thus, large I_{on}/I_{off} can be assured with a high-density s-SWCNT network in which high I_{on} can be achieved. The developed SWCNT/F8T2 composite solution has been proved with enriched s-SWCNT SWCNTs in Section 4.1. Hence, it is expected that the dip-coated SWCNT/F8T2-TFTs would simultaneously offer high I_{on} and large I_{on}/I_{off}. Fig. 4.5 compares I_{on} (extracted at V_g=-20 V, V_d=-1 V) verse I_{on}/I_{off} for 40 dip-coated SWCNT/F8T2-TFT and 40 SWCNT-TFTs prepared using the

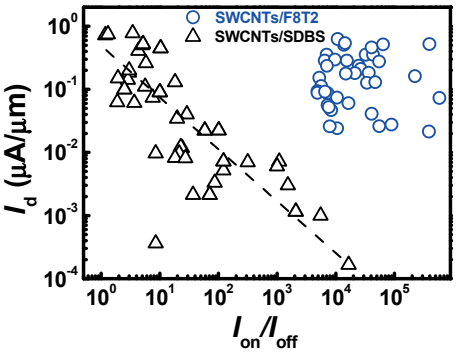

Fig. 4.5 I_{on} vs. I_{on}/I_{off} for 40 dip-coated SWCNT/F8T2-TFTs in comparison with similarly processed SWCNT-TFTs.

SWCNT/SDBS aqueous solution with various L. When I_{on}/I_{off} is at $\sim 10^4$, I_{on} of the dip-coated SWCNT/F8T2-TFTs is about 2 orders of magnitude higher than that of the SWCNT-network TFTs. It can be also found that for the SWCNT-network TFTs, I_{on}/I_{off} decreases quickly with increasing I_{on}, which is widely observed for SWCNT-based TFTs [19,21,33,39]. In contrast, the dip-coated composite TFTs possess a large I_{on}/I_{off} at 10^4–10^5 which is irrespective of I_{on}. This property is ideal for logic circuit applications.

4.4 Uniformity and scalability

The uniformity of the SWCNT-based TFTs has also been characterized in **Paper IV** by both optical and electrical methods. It is found that the intensity of the G-phonon band in the composite channel is considerably uniform, indicating a homogeneous distribution of SWCNTs in the composite film. Meanwhile, the distribution of I_{on} is rather narrow with a standard deviation less than 10%. This is superior to the reported results using other methods [26]. Excellent dimensional scalability of the TFTs is also found in **Paper IV**. By examining I_{on} of the TFTs with different L, an $I_{on} \propto 1/L$ relationship (*i.e.*, the current exponent m=−1) is obtained. This confirms a sufficiently high density of SWCNTs present in the composite film [33]. At each L, it is found that the variation of I_{on} of the TFTs is generally small, illustrating again the high-uniformity feature of such devices. The excellent uniformity and scal ability allows for the design of logic circuits in a controllable manner as in the case with Si-MOSFETs.

4.5 Ambient and operational stabilities

From the viewpoint of organic transistors, most semiconducting polymers are unstable especially when they are exposed to air or under electrical stress [10,11]. Various methods have been proposed to improve the stability of the polymer devices by engineering on their chemical structures [87] or optimizing the fabrication processes [88,89]. In contrast, SWCNTs themselves are stable and robust. By exploiting and combining the strengths of both constituents, the synergy can lead to stable nanotube/polymer composites. For F8T2-TFTs, it is reported that these devices show a severe degradation of I_{on} in ambient air or under gate bias stressing [90], although it is much better than other polymers [8]. This is also observed in **Paper III**, in which I_{on} reduced by more than 70% after a 90-days storage in air and sharply drops by 90% under a negative gate-bias stress. For the dip-coated SWCNT/F8T2-TFTs, studies of the long-term air stability and time transient of I_{on} under gate bias were performed. As can be seen in Fig. 4.6(a), no observable degradation of the TCs is found for such a TFT after being stored in air for 120 days. By monitoring the change in I_{on} (I_d(t), extracted at V_g=-20 V and V_d=-1 V) under a negative gate bias stress in Fig. 4.6(b) (left panel), the TFT shows a relatively stable operation with a decrease in I_d(t) by less than 15% after 1000 s. It indicates that a small amount of carriers is trapped during stress. After the stress is released (right panel), I_d(t) quickly recovers from the lowest current level due to the removal of the trapped carriers. Similar tendency is observed for the spin-coated SWCNT/F8T2-TFTs. The precise mechanism

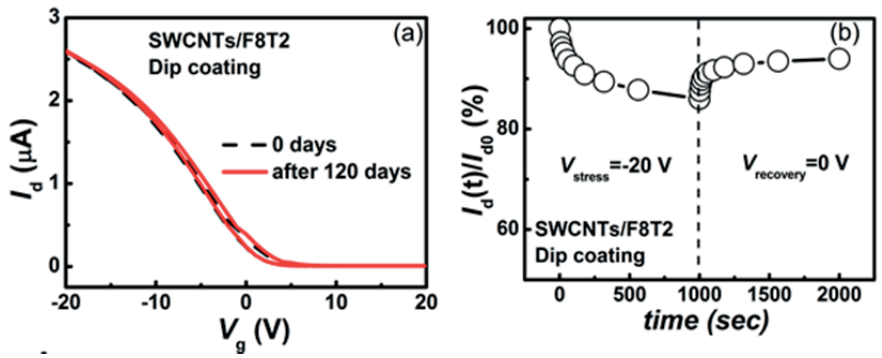

Fig. 4.6 (a) TCs of a dip-coated SWCNT/F8T2-TFT measured after fabrication (black dashed lines) and after being stored in air for 120 days (red solid lines). V_d was fixed at -1 V. (b) Time transient of the on-state current I_d(t) (extracted at V_g=-20 V and V_d=-1 V) under gate bias at V_{stress}=-20 V for 1000 s. This stress was removed for another 1000 s.

of the charge trapping remains to be confirmed, and a separate study focusing on stability issues is needed.

4.6 Logic circuits

The merits of our SWCNT/F8T2-TFTs including small-hysteresis, high I_{on}, large I_{on}/I_{off}, good stability, uniformity and scalability are among the desired features for logic circuit applications. The superior device performance allows us to construct some basic logic circuits. Firstly, we investigated one of the most fundamental circuit units, the inverter, by connecting a dip-coated SWCNT/F8T2-TFT (common back-gate configuration with 150 nm SiO_2 as gate insulator) with an off-chip resistor R at 1 MΩ. The inverter functions well with high voltage swing, near zero hysteresis and DC gain at ~2.5 (**Paper IV**).

We further designed and fabricated inverters by combining two individual-gate SWCNT/F8T2-TFTs with the 10-nm AlO_x as gate insulator. The design is based on the p-type logic, as shown in Fig. 4.7(a). One diode-connected TFT, denoted as "Ta", serves as a resistive load with $R_a=1/g_{ma}$. Here, g_{ma} is determined by the first derivative of equation (2.2). The other TFT, "Tb", drives the signal. When the input voltage (V_{in}) is "high" (*e.g.*, -1.5 V), Tb turns ON and operates as a low-resistance load R_{b1}, which satisfies the relationship $R_{b1}<<R_a$. Thus, the output voltage, $V_{out}=(R_{b1}/R_a+R_{b1})V_{dd}$ with V_{dd} as the supply voltage, will be "low" (close to 0 V). On the other hand, when V_{in} is "low", transistor Tb is in the OFF state and serves as a high-resistance load R_{b0} with $R_{b0}>>R_a$. Therefore, $V_{out}=(R_{b0}/R_a+R_{b0})V_{dd}$ is close to V_{dd}. To ensure a large output swing and then a large signal gain, the channel width to length ratio W/L for "Ta" is designed to be 1/10 of that for "Tb".

Fig. 4.7(b) presents the SEM top view image of a fabricated inverter with $W_b=L_b=W_a=0.1L_a=20$ μm. At a given supply voltage of V_{dd}=-1.5 V, the output voltage (V_{out}) as a function of the input voltage (V_{in}), *i.e.*, the voltage transfer characteristics (VTC) of the inverter, is shown in Fig. 4.7(c) (the left axis). It is found that the output swing reaches 1.4 V which is 95% of $|V_{dd}|$. The maximum gain of the inverter reaches ~4, cf. Fig. 4.7(c), right vertical axis, indicating that the inverter has a good capability of signal amplification. Furthermore, the hysteresis between the forward and backward sweeps is also negligible, which is a direct result of the small hysteresis TFTs.

By adding another transistor to the inverter, either in parallel or in series with the pull-down transistor, logic circuits NOR and NAND, respectively, were constructed in **Paper V**. These results confirm an excellent function of the circuits based on the SWCNT/F8T2-TFTs. Our demonstration of these logic circuits sheds light on the nanotube-based electronics in the near future.

The dynamic response of the inverters was also investigated in both **Paper IV and Paper V**. The cut-off frequency, f_T, was obtained by measuring the AC response of the inverter with input signals at various frequency. Theoretically, f_T can be estimated by,

$$f_T = \frac{g_m}{2\pi\left(C_g + C_{para}\right)} \geq \frac{\mu V_{dd}}{2\pi L^2} \tag{4.1}$$

For the inverters fabricated using an SWCNT/F8T2-TFT (L=50 μm), with an off-chip resistor, it is found that f_T is at the level of 10 kHz (**Paper IV**). Note that this value is obtained for the TFT with a common gate configuration where a huge C_{para} exists between the Si substrate gate and the large size S/D metal pads. It is expected that a higher f_T can be achieved by controlling the parasitic effects. In **Paper V,** using individual-gate TFTs, the inverter possesses an f_T at about 100 kHz. It is higher than that obtained from common gate devices due to the smaller L (20 μm) as well as the lower C_{para}. However, this value is much lower than the theoretically calculated one from equation (4.1), implying the necessities of a better control of the parasitics, *e.g.* a self-aligned structure [70]. It is noted that the dimensions of the solution-processed TFTs are compatible with novel printing techniques, making them more attractive for ultra-low cost marcoelectronics and printing electronics.

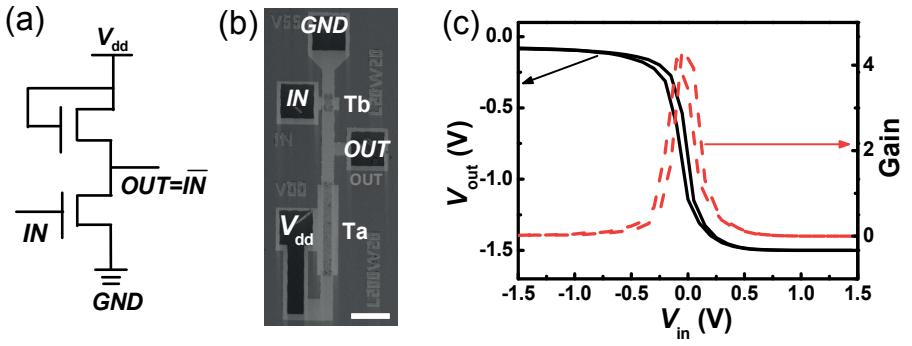

Fig. 4.7. (a) Circuit schematic, (b) top-view photograph and (c) DC response of a p-type inverter. *W*/*L* for the load TFT (Ta) is 1/10 of that for the drive TFT (Tb). In (c), the DC gain of the inverter is also presented. The scale bars in (b) is 100 μm.

5. Overview of the Appended Papers

Paper I presents a systematic investigation of one of the most important transistor parameters, C_g, with random SWCNT networks as the conduction channel. Different from conventional Si-MOSFETs in which the channels are made of homogeneous bulk materials, the electrical conduction in the SWCNT networks is percolation dominant. It is hence strongly dependent on the percolation geometrical parameters including nanotube density ρ, length L_{nt}, etc. [33]. The approximation of C_g by C_P using the parallel plate capacitor model widely adopted in Si-MOSFETs can lead to errors by orders of magnitude. The main source of errors is false inclusion of the SWCNTs that do not contribute to current conduction. In order to accurately determine C_g, *C-V* measurements were performed directly on the SWCNT-network TFTs. The measurement arrangement in fact presents a standard procedure used for extraction of C_g for Si-MOSFETs. Monte Carlo simulations were performed in this paper to precisely determine the amount of SWCNTs needed for C_P versus that contributing to C_g. A substantial difference in them is found in the region near the percolation threshold p_c. According to the calculation results, the measured capacitance coincides well with the effective C_g. This method was utilized to analyze C_g of the TFTs with different nanotube coverage. The relation between C_g and p is then unveiled. Meanwhile, frequency dispersion is observed at high f_m, and this behavior can be well accounted for by the introduction of an *RC* TL model. By measuring C_g in the region where TL effect is negligible, C_g of the nanotube networks can be more accurately determined. The technique established in **Paper I** has been adopted in the rest of the thesis including the other appended papers for both SWCNT-network TFTs and SWCNT/F8T2-TFTs, since it is essential for the determination of μ.

Intuitively, μ is an intrinsic parameter of the material which represents the transport characteristics of the semiconductor. However, for SWCNT-based transistors, a large variation is found in the reported μ values. This is not only related to the process conditions, but also affected by the percolation geometrical parameters [18,35,36]. This is counter-intuitive and hinders a sensible evaluation of device performance, which calls for the consideration of establishing a standard procedure to extract μ of the nanotube TFTs. This motivates the work in **Paper II**. In this paper, the challenges posed for μ extraction are analyzed including C_g, current scaling behavior, and hysteresis. To combat the hysteresis issue, a novel AP pulsed I_d-V_g method is

proposed to eliminate the frequently observed huge hysteresis with the SWCNT-TFTs. The AP method is simple, effective and suitable also for TFTs with spin-coated SWCNT/F8T2 composites, as shown in **Paper III**. This method is in fact recommended in the research community as a must-to-do for μ discussions [91]. Starting with hysteresis-free TCs, μ of the SWCNT-network TFTs can be extracted using the measured C_g in **Paper I** as well as a proper consideration of the current exponent m. This is of particular significance for TFTs with low-density SWCNTs in the network. By properly addressing all these challenges, a comprehensive methodology for μ extraction is established and the resultant μ values are independent of percolation geometries. This procedure has been applied in **Papers III-V** to evaluate the device performance.

The devices made from SWCNT/surfactant-aqueous solutions by drop casting in **Papers I** and **II** have shown certain potential for high-performance TFTs. However, they still suffer severely from the shortcomings of low μ, small I_{on}/I_{off}, huge hysteresis, and poor uniformity. Solubilizing SWCNTs by polymer wrapping provides an alternative route towards solution-processed TFTs with improved electrical performance and these efforts are presented in **Papers III-V**. In **Paper III**, the air-stable semiconducting polymer F8T2 was chosen for dissolving the SWCNTs in solution using simple ultra-sonication processes. Individual or small bundles of nanotubes, instead of the unwanted large bundles, are obtained in the composite films prepared by a spin-coating process. The resultant SWCNT/F8T2-TFTs are found to possess a high μ approaching 10 $cm^2V^{-1}s^{-1}$ with relatively high SWCNT concentrations. It is worth noting that this mobility value is comparable to that obtained for TFTs with the SWCNT/surfactant-aqueous solution. When the SWCNT concentration is reduced for a large I_{on}/I_{off} at 10^6, μ remains at 0.3 $cm^2V^{-1}s^{-1}$. In addition, the environmental and operational stabilities of the SWCNT/F8T2-TFTs are both remarkably improved as compared to those for F8T2-TFTs without SWCNTs. The excellent stability was further confirmed by the SWCNT/F8T2-TFTs and circuits fabricated in **Papers IV and V**.

However, the TFTs in **Paper III** still suffer from huge hysteresis as well as from difficulties in simultaneous achievement of high I_{on} and large I_{on}/I_{off}. These have been the main obstacles for the development of SWCNT-based TFTs. In **Paper IV**, the fabricated SWCNT/F8T2-TFTs via a simple dip-coating process exhibit negligible hysteresis, high μ (in the range of 10-20 $cm^2V^{-1}s^{-1}$) as well as large I_{on}/I_{off} (10^4-10^5) without the necessity of any complex treatment. This is accomplished thanks to the unique composite structure with s-SWCNTs being well wrapped by the surrounded F8T2. The presence of F8T2 effectively isolates SWCNTs from the SiO_2 surface as well as from the H_2O/O_2 in the atmosphere. The selective removal of m-SWCNTs by F8T2 is attributed to the preferential interaction between s-SWCNTs and F8T2 macromolecules. The s-SWCNT-enriched composite material enables

the use of thicker composite films with high-density nanotubes in the channel without compromising the demand on a large I_{on}/I_{off}. The uniformity of the devices has therefore been significantly improved. As a result, a current scaling relation of $I_{on} \propto L^{-1}$ is achieved.

Our achievements with the SWCNT/F8T2-TFTs of excellent electrical performance such as high μ, large I_{on}/I_{off}, good stability, good uniformity and dimensional scalability have facilitated the realization of logic circuits. These results are presented in **Paper V**. In this paper, small logic circuits including inverters, NANDs, and NORs were designed and fabricated using individual-gate SWCNT/F8T2-TFTs with dip-coated composite thin films on a thin AlO_x gate dielectric. These circuits operate with small hysteresis, high cut-off frequency at 100 kHz, and low supply voltage at -1.5 V. Till then, the story about solution processed electronic circuits based on SWCNTs have been completed.

In all appended papers, the author's contribution includes channel material preparation, device and circuit design, device fabrication, electrical characterization, data analysis and manuscript writing.

6. Summary and Outlook

TFTs have gained enormous attention for their applications in macro- and flexible electronics. The implementation is, however, still largely restricted by several major technical challenges, especially optimization of the channel material which can simultaneously offer low-cost fabrication, mechanical flexibility and excellent electrical performance. SWCNTs offer enormous potential to meet these requirements. In this thesis, systematic investigations have been carried out with a overall goal of boosting the electrical performance of the solution processed SWCNT-based TFTs. In detail, high μ, large I_{on}/I_{off}, zero hysteresis, good stability, good uniformity and scalability are the desired characteristics. The studies have not only generated new knowledge/understanding of device physics, but also led establishment of experimental procedures and techniques to enhance the device performance. The major achievements of this thesis can be concluded as follows:

(1) C_g of the SWCNT-network TFTs can be obtained by applying direct C-V measurements on the TFTs. By doing so, the isolated nanotubes that do NOT contribute to current conduction are effectively excluded in the measured C_g. Thus, it is more accurate compared with C_g determined by other methods such as using a MIS structure. It is found that the parallel-plate capacitor model is valid in the high-density nanotube region (as expected) while it severely overestimates C_g for networks of low SWCNT density.

(2) Frequency dispersion of the measured C_g is studied by employing an RC TL model. It points to the importance of measuring C_g in the frequency region where no channel charging effects occur. This is crucial for a reliable μ extraction.

(3) A novel pulsed I_d-V_g measurement method in AP mode is proposed to mitigate the influence of severe hysteresis on μ extraction for the SWCNT-based TFTs. This method is simple, effective and necessary when hysteresis cannot be eliminated during device fabrication. It is essential to correctly extract the intrinsic μ of the nanotube based TFTs.

(4) A comprehensive procedure for μ extraction for the SWCNT-network TFTs is established with a concentration on alleviating the effects of hysteresis, determining the effective C_g and controlling the current exponent m. Most importantly, it is proven that the extracted μ independent of the geometrical parameters can represent the intrinsic property of the SWCNT networks. The established extraction procedures provide a powerful tool in the μ extraction for nanotube-based TFTs.

(5) The combination of SWCNTs with F8T2 enables TFT fabrication by solution-phase processing under ambient conditions with good electrical performance. This specific composite provides a promising pathway to manufacturing high-performance, low-cost flexible macroelectronics.

(6) The huge hysteresis typically present in the SWCNT-based TFTs is effectively suppressed using the SWCNT/F8T2 composite processed by a simple dip-coating technique. It is confirmed that the hysteresis reduction relies on the isolation of SWCNTs by F8T2from the surface of gate insulator as well as from the H_2O/O_2 in the atmosphere.

(7) Outstanding switching performance with high I_{on} and large I_{on}/I_{off} is achieved with the dip-coated SWCNT/F8T2-TFTs, where the m-SWCNTs are selectively removed by the preferential interaction between s-SWCNTs and F8T2. With high-density SWCNTs in the composite, the TFTs are characterized by remarkable uniformity and excellent geometrical scalability.

(8) Some fundamental logic circuits are realized using individual-gate SWCNT/F8T2-TFTs prepared by dip-coating as the basic building block. The eminent electrical characteristics such as small hysteresis and high cut-off frequency up to 100 kHz are obtained.

Although significant progress has been made, much remains to be done towards the ultimate macroelectronics of mechanical flexibility and stretchability. And all this should ideally be realized using simple and low-cost manufacturing technologies. The following ideas concerning specifically future SWCNT-based TFTs are discussed as follows:

(1) Although the currently obtained μ in the range of 10-20 $cm^2V^{-1}s^{-1}$ is by itself outstanding for solution processed SWCNT networks, it is still far below the reported value of 80 $cm^2V^{-1}s^{-1}$ obtained by using as-grown chemical vapor deposited SWCNTs [20]. This leaves room to improve by, for instance, better sources of SWCNTs or other elaborate treatments.

(2) Printability of SWCNTs should be further improved by tailoring the formulation of the functional composites, since the printing quality determines the morphology of the SWCNT-networks. The latter (morphology) plays an essential role for device performance [80].

(3) Realization of flexible TFTs requires proper treatments of flexible substrates in order to guarantee device performance and yield. Techniques such as surface priming of flexible substrates are necessary for this purpose.

(4) Both parasitic resistance (contact resistance) and parasitic capacitance (overlapped capacitance) pertaining to the present TFTs need proper device design and process realization in order to reduce their negative effects on circuit performance. For instance, parasitic resistance/capacitance would reduce the response speed of a circuit. Self-aligned device architectures common in Si-MOSFET technologies can be a path to pursue.

(5) More sophisticated logic circuits, such as decoders and ring oscillators, await a better control of the switching performance of the TFTs.

(6) Studies of the stability of the SWCNT/polymer-based TFTs are necessary in order to explore the mechanism(s) as well as means to enhance the device performance.

Sammanfattning på svenska

Parallellt med den enastående utveckling som sker inom mikroelektroniken, med ständigt mindre och snabbare komponenter, så växer idag ett nytt spännande område fram inom elektroniken. Det är inom området makroelektronik och flexibel elektronik. Genom att försöka göra elektroniska kretsar i material som är flexibla, töjbara och billiga så kan helt nya tillämpningsområden bli möjliga inom vilken traditionell mikroelektronik inte är användbar. Böjbara displayer, elektronik i textilier, elektronik som kan sättas på huden, elektronik som går att trycka på t ex papper och plaster, samt många fler tillämpningar som skulle bli möjliga om ny teknologi kan utvecklas inom området.

Hittills har dock tillämpningar begränsats av flera tekniska problem. Speciellt problemet att finna ett optimalt material för den aktiva elektriska komponenten som samtidigt kan erbjuda låg tillverkningskostnad, mekanisk böjbarhet och tillräckligt bra elektriska egenskaper har varit svårt.

Användning av kolnanorör, så kallade *Single Wall Carbon Nanotubes* (SWCNT), i tunnfilmstransistorer (TFT) för makroelektronik och flexibel elektronik har väckt mycket stort intresse på senare tid. Kolnanorör har unika egenskaper som erbjuder en mycket lovande lösning. I denna avhandling har möjligheten att tillverka tunnfilmstransistorer utgående från SWCNT uppblandade i en lösning systematiskt undersökts. Ett antal centrala viktiga egenskaper har undersökts för att göra det möjligt för SWCNT att användas inom flexibel elektronik. En hög mobilitet μ, dvs rörligheten på elektriska laddningar, en stor skillnad mellan ledningsström och läckström utryckt i kvoten I_{on}/I_{off}, ingen hysteres, god stabilitet, jämn kvalitet, och skalningsbarhet är önskvärda egenskaper som alla har undersökts och förbättrats i avhandlingsarbetet.

Undersökningarna har inte enbart gett nya kunskaper och insikter i elektriska komponenters fysik, utan har också lett till nya experimentella tillvägagångssätt och tekniker för att förbättra komponenternas prestanda. Avhandlingens främsta bidrag till forskningsfältet kan sammanfattas i följande punkter:

(1) Gate-kapacitansen C_g hos TFT med SWCNT-nätverk har bestämts genom att direkt mäta kapacitans som funktion av spänning hos transistorn. Genom en sådan mätning så kommer isolerade kolnanorör inte att påverka C_g. Metoden är mer noggrann än andra metoder som t.ex. mätningar på metall–isolator–halvledarstrukturer, *metal–insulator–semicondutor* (MIS). Det

visar sig att plattkondensatormodellen som förväntat gäller för användning av kolnanorör med hög packningstäthet, medan den allvarligt överskattar Cg för glesare nätverk.

(2) Frekvensberoende av uppmätt C_g har studerats genom att tillämpa en modell där kolnanorörsnätverket betraktas som en transmissionsledare med stora förluster modellerade som resistanser och kapacitanser. Resultatet visar att det är viktigt att mäta C_g vid ett frekvensintervall där det inte sker någon uppladdning av nanorörsnätverket. Detta är helt avgörande för en korrekt beräkning av mobiliteten μ.

(3) En ny metod där I_d-V_g mäts pulsat med växlande polaritet har utvecklats för att undertrycka inverkan av hysteres på mobilitetsuppskattning hos SWCNT TFT. Denna metod är enkel, effektiv och till och med nödvändig i de fall då hysteres inte kan undvikas vid komponenttillverkningen. Den är väsentlig för att noggrant kunna extrahera mobiliteten hos kolnanorörsbaserade tunnfilmstransistorer.

(4) En utförlig procedur för mobilitetsextraktion från SWCNT-nätverksbaserade TFT har tagits fram, där tonvikten lagts på att undvika hysteres, att bestämma den effektiva gate-kapacitansen C_g, och att kunna styra strömmens exponent m. Viktigast är att det visas att den extraherade mobiliteten μ kan representera en inneboende egenskap hos nanorörsnätverket som är oberoende av geometrin. Det presenterade tillvägagångssättet utgör fortsättningsvis ett kraftfullt verktyg för mobilitetsextraktion från nanorörsbaserade tunnfilmstransistorer.

(5) Kombinationen av SWCNT och den halvledande polymeren F8T2 har möjliggjort tillverkning i normal atmosfär av TFT med goda elektriska egenskaper. Materialkombinationen utgör en verkligt lovande väg till att tillverka böjbar makroelektronik med god prestanda till låg kostnad.

(6) Den stora hysteres som är typisk för SWCNT TFT har effektivt undertryckts genom att applicera SWCNT/F8T2-blandningen men en enkel doppteknik. Det bekräftas att hysteresminskningen härrör från att F8T2 isolerar SWCNT såväl från ytan på gate-dielektrikat som från vatten och syre i atmosfären.

(7) Doppbelagda SWCNT/F8T2-TFT gav bra switchegenskaper med hög ledningsström I_{on} och hög avstängningskvot I_{on}/I_{off}. De goda egenskaperna härrör från att metalliska kolnanorör selektivt kan avlägsnas då halvledande kolnanorör preferentiellt interagerar med F8T2. Vid en hög halt av SWCNT i kompositen karaktäriseras tunnfilmstransistorerna av god uniformitet och mycket god geometrisk skalbarhet.

(8) Några grundläggande logiska kretsar har konstruerats med SWCNT/F8T2-TFT tillverkade med doppteknik. Kretsarna karaktäriseras av mycket goda elektriska egenskaper såsom låg hysteres och hög brytfrekvens, upp till 100 kHz.

Även om väsentliga steg har tagits mot en fulländad makroelektronik med böj- och sträckbarhet så återstår mycket att göra. Idealt skall tillverkningen

också vara enkelt och billigt. Följande idéer presenteras angående framtida utvecklingsmöjligheter:

(1) Även om den härmed uppnådda mobiliteten i intervallet 10-20 $cm^2V^{-1}s^{-1}$ i och för sig är unikt hög för lösningsprocessade SWCNT-nätverk så är den ändå långt ifrån de 80 $cm^2V^{-1}s^{-1}$ som uppmätts för CVD-belagda SWCNT [22]. Det ger utrymme för förbättringar, t.ex. genom att använda andra leverantörer av SWCNT eller genom att utveckla beläggningsmetoden.

(2) Tryckbarheten av SWCNT skulle kunna förbättras ytterligare genom att skräddarsy sammansättningen hos kompositen. Tryckkvalliten bestämmer morfologin hos nätverken, vilket i sin tur påverkar komponenternas prestanda.

(3) Skapandet av böj- och sträckbara tunnfilmstransistorer kräver korrekt behandling av de flexibla substraten för att garantera goda prestanda. Förbehandling av substraten, s.k. *priming*, behövs för detta.

(4) Både parasitiska resistanser och –kapacitanser som följer med dagens tunnfilmstransistorer kräver riktig komponentdesign och –tillverkning för att minimera negativa konsekvenser för hela kretsen. Till exempel så kan dessa parasitegenskaper minska responshastigheten hos en krets. Självlinjerande komponentarkitekturer, liknande de som används vid konventionell mikroelektroniktillverkning, kan vara en framkomlig väg.

(5) Mer sofistikerade logiska kretsar, som avkodare och ringoscillatorer, får invänta utvecklandet av TFT med mer uniform switchbarhet

(6) Stabilitetsstudier av SWCNT/polymer-baserade TFT är nödvändiga för att förstå och förbättra komponenternas beteende.

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Appendix A

Transmission line impedance of a nanotube network

It is natural to consider a nanotube network as a lossy TL [73], as shown in Fig. A.1, with discrete elements r and c. According to the basic TL model,

$$\begin{aligned} r &= R / L \\ c &= C / L \end{aligned} \tag{A.1}$$

where R and C are the total resistance and capacitance of the nanotube network, respectively. The characteristic impedance Z_0 of the TL can be given by,

$$Z_0 = \sqrt{r / j\omega c} = \frac{(1-i)}{\sqrt{2}}\sqrt{r / \omega c}$$

$$\omega = 2\pi f \tag{A.2}$$

where ω is the angular frequency and f is the signal frequency. According to the lumped parameter model, the total impedance of a TL can be expressed as,

$$Z = R + \frac{1}{j\omega C} = R - j\frac{1}{\omega C} \tag{A.3}$$

Combining (A.2) and (A.3), R and C of the nanotube network are determined by,

$$R = \sqrt{\frac{r}{2\omega c}} = \sqrt{\frac{r}{4\pi f_m c}} \tag{A.4}$$

$$C = \sqrt{\frac{2c}{\omega r}} = \sqrt{\frac{c}{\pi f_m r}} \tag{A.5}$$

The propagation constant k and the attenuation constant α can be written as,

$$k = \sqrt{r\, j\omega c} = \sqrt{\frac{1}{2}}(1+i)\sqrt{r\omega c} \tag{A.6}$$

$$\alpha = \sqrt{\frac{1}{2} r \omega c} = \sqrt{\pi r f_m c} \tag{A.7}$$

Thus, the characteristic frequency f_c can be determined by assigning the critical delay time $1/\alpha = L$, *i.e.*,

$$f_c = \frac{1}{\pi RC} \tag{A.8}$$

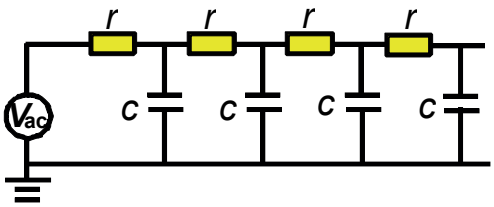

Fig. A.1 Equivalent circuit for a TL capacitively coupled to the ground.

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