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Design and Characterization of RF-LDMOS Transistors and Si-on-SiC Hybrid Substrates

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Abstract
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With increasing amount of user data and applications in wireless communication technology, demands are growing on performance and fabrication costs. One way to decrease cost is to integrate the building blocks in an RF system where digital blocks and high power amplifiers then are combined on one chip. This thesis presents LDMOS transistors integrated in a 65 nm CMOS process without adding extra process steps or masks. High power performance of the LDMOS is demonstrated for an integrated WLAN-PA design at 2.45 GHz with 32.8 dBm output power and measurements also showed that high output power is achievable at 5.8 GHz. For the first time, this kind of device is moreover demonstrated at X-band with over 300 mW/mm output power, targeting communication and radar systems at 8 GHz. As SOI is increasing in popularity due to better device performance and RF benefits, the buried oxide can cause thermal problems, especially for high power devices. To deal with self-heating effects and decrease the RF substrate losses further, this thesis presents a hybrid substrate consisting of silicon on top of polycrystalline silicon carbide (Si-on-poly-SiC). This hybrid substrate utilizes the high thermal conductivity of poly-SiC to reduce device self-heating and the semi-insulating properties to reduce RF losses. Hybrid substrates were successfully fabricated for the first time in 150 mm wafer size by wafer bonding and evaluation was performed in terms of both electrical and thermal measurements and compared to a SOI reference. Successful LDMOS transistors were fabricated for the first time on this type of hybrid substrate where no degradation in electrical performance was seen comparing the LDMOS to identical transistors on the SOI reference. Measurements on calibrated resistors showed that the thermal conductivity was 2.5 times better for the hybrid substrate compared to the SOI substrate. Moreover, RF performance of the hybrid substrate was investigated and the semi-insulating property of poly-SiC showed to be beneficial in achieving a high equivalent substrate parallel resistance and thereby low substrate losses. In a transistor this would be equal to better efficiency and output power. In terms of integration, the hybrid substrate also opens up the possibility of heterogeneous integration where silicon devices and GaN devices can be fabricated on the same chip.

Keywords: LDMOS, RF, losses, crosstalk, silicon carbide, Si-on-SiC hybrid substrate, wafer bonding, CMOS

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List of Papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I Johansson T., Bengtsson O., Lotfi S., Vestling L., Norström H., Olsson J., Nyström C. (2013) A +32 dBm LDMOS power amplifier for WLAN in 65 nm CMOS technology. *European Microwave Integrated Circuits Conference*, p. 53-56

II Lotfi S., Bengtsson O., Olsson J. (2014) 65 nm CMOS integrated LDMOS for WLAN and X-band applications. Submitted to *IEEE Transactions on Electron Devices*

III Lotfi S., Olsson J. (2013) Investigating reliability and stress mechanisms of DC stressed CMOS 65 nm RF-LDMOS by full gate current characterization. Submitted to *IEEE Transactions on Device and Materials Reliability*

IV Lotfi S., Li L-G., Vallin Ö., Norström H., Olsson J. (2012) Fabrication and Characterization of 150 mm Silicon-on-Polycrystalline-Silicon Carbide Substrates. *Journal of Electronic Materials*, 41(3):480-487

V Lotfi S., Li L-G., Vallin Ö., Vestling L., Norström H., Olsson J. (2012) LDMOS-transistors on semi-insulating silicon-on-polycrystalline-silicon carbide for improved RF and thermal properties. *Solid-State Electronics*, 70:14–19

VI Lotfi S., Vestling L., Olsson J. (2013) RF losses, crosstalk and temperature dependence for SOI and Si/SiC hybrid substrates, *Solid-State Electronics*, accepted for publication.

Author's contribution

I	Minor part of planning. DC- and small-signal measurements. Corresponding part of writing.
II	Part of planning and analysis. Involved in load-pull measurements. Significant part of writing.
III	Part of planning and analysis. All electrical measurements. All writing.
IV	Part of planning and analysis. Major part of fabrication and electrical characterization. Material characterization performed by L-G. Li. All writing. Simulations performed by J. Olsson.
V	Part of planning and analysis. Electrical characterization and all writing. Simulations performed by J. Olsson.
VI	Part of planning and analysis. Major part of fabrication, RF measurements, CV measurements, impedance spectroscopy and modeling. Involved in optical spectrometry. All writing. Simulations performed by J. Olsson.

Related work

The following papers are related to the work in the thesis but have not been included.

Lotfi S., Li L-G., Vallin Ö., Norström H., Olsson J. (2011) Mobility profiles and thermal characterization of SOI and Si-on-SiC hybrid substrates. *Proc. of 2011 IEEE International SOI conference*, Tempe, USA

Lotfi S., Vestling L., Olsson J. (2013) RF losses, crosstalk and temperature dependence for SOI and hybrid Si/SiC substrates. *Proc. of EUROSOI 2013 workshop*, Paris, France

Lotfi S., Vallin Ö., Li L-G., Vestling L., Norström H., Olsson J. (2011) LDMOS transistors on 150 mm silicon-on-polycrystalline-silicon carbide hybrid substrates. *Proc. of EUROSOI 2011 workshop*, Grenada, Spain, p.153-154

Lotfi S., Vallin Ö., Li L-G., Vestling L., Norström H., Olsson J. (2010) Electrical and thermal characterization of 150 mm silicon-on-polycrystalline-silicon carbide hybrid substrates. *Proc. of 2010 IEEE International SOI Conference*, San Diego, USA, p.115-116

Olsson J., Lotfi S. (2012) Self-heating and scaling effects of multi-finger LDMOS transistors on SOI and Si-on-SiC hybrid substrates with diamond heat spreading layer. *Proc. of EUROSOI 2012 workshop*, Montpellier, France, p.31-32

Li L-G., Lotfi S., Vallin Ö., Olsson J. (2014) Thermal characterization of polycrystalline SiC. *Journal of Electronic Materials,* accepted for publication.

Contents

List of abbreviations

6H-SiC	Single crystalline silicon carbide (6H)
AC	Alternating current
BiCMOS	Bipolar CMOS
BJT	Bipolar junction transistor
CMOS	Complementary metal oxide semiconductor
CMP	Chemical mechanical polishing
C_P	Equivalent parallel capacitance
C_S	Equivalent series capacitance
DC	Direct current
FN tunneling	Fowler Nordheim tunneling
GaAs	Gallium arsenide
GaN	Gallium nitride
GP-SOI	Ground plane-SOI
HCI	Hot-carrier injection
HF	High Frequency
HR	High resistivity (~1 kΩcm)
LDMOS	Lateral double-diffused metal oxide semiconductor field effect transistor
LR	Low resistivity (~1 mΩcm)
MOSFET	Metal oxide semiconductor field effect transistor
MR	Medium resistivity (~10 Ωcm)
NVA	Network Vector Analyzer
PA	Power amplifier
PAE	Power added efficiency
Poly-Si	Polycrystalline silicon
Poly-SiC	Polycrystalline silicon carbide
P_{OUT}	Output power
QBD	Charge-to-breakdown
RESURF	Reduced surface field
RF	Radio frequency
rms	Root-mean-square roughness
R_P	Equivalent parallel resistance
R_S	Equivalent series resistance
SiGe	Silicon germanium
Si-on-poly-SiC	Silicon on polycrystalline silicon carbide
SOI	Silicon on insulator

TEM	Transmission Electron Microscopy
WLAN	Wireless Local Area Network
XRD	X-ray Diffraction
Z	Impedance
α-Si	Amorphous silicon

List of symbols

$\hbar$	Reduced Planck's constant
E_i	Electric field over insulator
f	Frequency
f_{max}	Unity power gain frequency
f_T	Unity current gain frequency
g_d	Drain conductance
g_m	Transconductance
J	Current density
L	Channel length
m^*	Electron effective mass
q	Electronic charge
R_{ON}	On-resistance
R_{OUT}	Output resistance
V_d	Drain voltage
V_{dd}	Supply voltage
V_g	Gate voltage
W	Gate width
ε	Permittivity
ε_0	Vacuum permittivity
ε_∞	Dielectric constant at high frequencies
ε_r	Relative permittivity or dielectric constant
ε_s	Dielectric constant at low frequencies (static)
ρ	Resistivity
τ	Relaxation time
ϕ_B	Barrier height
ω	Angular frequency

1. Introduction

In the modern society of today we are more and more dependent on wireless communication systems as a consequence of the tremendous progress in the field the last couple of decades. The wireless communication market is increasing every year and everything from mobile communication base stations to single handheld devices have to operate at satisfactory levels [1]. With the progress, the demands grow larger, we want to surf fast on our smart phones, download data at high speeds and devices should be light weight and small in size. These demands translate into physical aspects such as operating at higher frequencies, making electronic components smaller in size and integrating the circuits to achieve fewer chips. Fabrication should be large in volume to be cost-effective and the devices themselves should have low power consumption and withstand high temperatures and other harsh environments.

There are many technologies available in the semiconductor industry, each adapted to one or several applications. Complementary Metal-Oxide Semiconductor (CMOS) is by far the most popular semiconductor technology and the choice of mass production for fabricating digital circuits today. In CMOS, components such as microprocessors, logic circuits and amplifiers are designed with Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) as building blocks. With CMOS technology it has been possible to downscale the MOSFET, which is an appealing property to foundries due to cost-effectiveness and feasibility. Today, the 22 nm node is in production where e.g. Intel uses a 3D-design to achieve the desired density capability [2]. As long as the performance needed is reached, CMOS will continue to be the choice of technology, but the time is coming where CMOS is difficult to downscale further without affecting performance and other solutions are being sought after [3].

For high frequency and high output power applications, such as power amplifiers (PA) for wireless portable devices and base stations, the bipolar junction transistor (BJT), with e.g. silicon germanium (SiGe) to boost the speed has been commonly used [4]. Preferably, the BJTs are integrated into the CMOS process (BiCMOS) [5], but the integration has drawbacks such as cost-effectiveness, since both digital and analog parts need to be optimized in the process.

To increase the performance further in terms of speed and high frequency performance, other compound semiconductors are ideal for high power and

high frequencies, e.g. gallium arsenide (GaAs) and gallium nitride (GaN). These materials are expensive and do not integrate easily with CMOS technology, which means that the applications of these materials are chosen accordingly. Foundries are of course interested in saving money and wafer sizes are increasing, and as for today, 300 mm wafer processes do not include power devices. When one-chip solutions are sought for at 300 mm, cascode circuits with MOSFETs are used in order to withstand high voltages and reach high RF power.

When requirements on higher power and high frequency performance using silicon were getting tighter, the MOSFET evolved into a lateral double diffused MOSFET (LDMOS) [6, 7]. The LDMOS transistor replaced the BJT in base stations during the 90's as higher operating frequencies became standard. The LDMOS offers better linearity [8] and implementation advantages compared to the BJT and is today also common in power amplifiers for radar systems [9]. Fabrication of the transistor is performed using common MOS processing techniques in standalone circuit building blocks; hence, integrating the RF device such as an LDMOS with CMOS has been a hot topic for a while [10].

Integrating a complete radio system in one single CMOS chip with no external devices would create tremendous opportunities for low-cost wireless applications. A one chip solution would decrease manufacturing costs, size and weight of e.g. a RF frontend module. An integrated driver for power amplifiers, where high voltage swings are required, could be implemented in the same chip as the digital circuits. The challenge lies in performance of the power amplifier in the intended application. High power, high efficiency and low noise are just a few of the requirements that have to be fulfilled. Integrating LDMOS in CMOS processes has been demonstrated by adding extra process steps or masks to existing CMOS processes at foundry [11-13]. However, low cost and low power consumption are demands driven by CMOS technology which implies that the challenge is to preferably not add extra masks or process steps to avoid extra cost or changes to existing device parameters [14] but still show the desired performance.

Combining analog and digital circuits in one chip consequently makes issues like crosstalk extra crucial. Adding isolating trenches, guard rings and wells between devices can reduce some of the coupling [15]. Substrate engineering would be one way to deal with crosstalk, where e.g. silicon-on-insulator (SOI) adds extra isolation underneath the devices [16], see schematic in Figure 1a. Furthermore, as CMOS is downscaled further and performance in fast low-power applications is difficult to enhance, SOI also shows benefits in higher performance [17]. The buried oxide decreases parasitic capacitances [18], and to further decrease the substrate losses, high resistivity SOI (HR-SOI) [16] has been introduced and is also in production and available on the market. Another solution which is not as widely researched as HR-SOI is low resistivity SOI (LR-SOI). It also shows increased

RF performance compared to medium resistivity SOI (MR-SOI), especially in crosstalk since the LR silicon behaves as a ground plane effectively shunting the signals to ground [19, 20]. The drawback with a SOI-material is the low thermal conductivity of buried oxide itself, which can cause device self-heating, especially for high power devices [21, 22], illustrated in Figure 1a. Attempts have been made to replace the oxide with a material with higher thermal conductivity such as diamond [23], aluminum nitride [24] and aluminum oxide [25] but e.g. large wafer production is of concern.

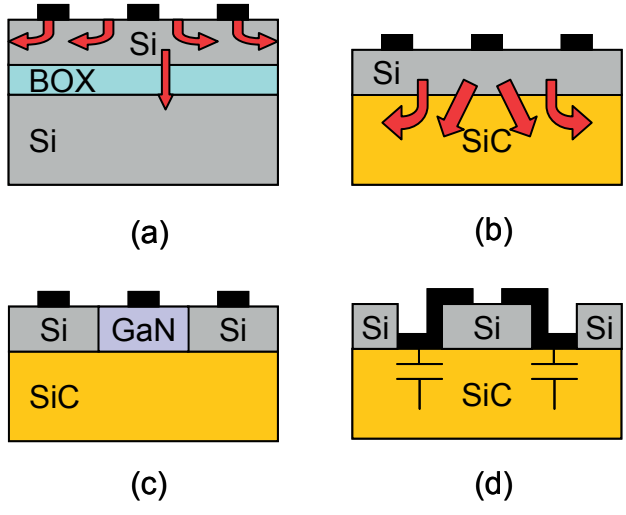

Figure 1. Heat dissipation in (a) SOI substrate and (b) the Si-on-SiC hybrid substrate. (c) Heterogeneous integration in the hybrid substrate with GaN. (d) Extrinsic metal deposited directly on top of the SiC-substrate obtaining only a small parasitic capacitance which decreases substrate losses and enhances efficiency.

Silicon carbide (SiC) offers both high thermal conductivity and semi-insulating properties [26] which would make a SiC substrate underneath silicon devices ideal for high thermal dissipation and low RF substrate losses, as illustrated in Figure 1b. This silicon-on-silicon carbide (Si-on-SiC) hybrid substrate [27] would also offer the possibility for heterogeneous integration, e.g. etching the silicon and growing GaN for power devices, enabling the integration of digital circuits, drivers and amplifiers on the same chip with additional benefits in less self-heating and lower substrate losses [28], see Figure 1c. Moreover, etching the devices free as silicon islands, the extrinsic metal can be deposited directly on SiC as illustrated in Figure 1d and thereby only contribute with a low parasitic substrate capacitance from the thick SiC substrate. Consequently, the output impedance increases for a transistor in a power amplifier and accordingly the performance increases in terms of efficiency and operating frequency.

Mobile phone communication, WLAN and radar systems demand high performance at high frequencies ranging from ~1-30 GHz. As CMOS technology is downscaled and low supply voltages follow, generating high power at high frequencies becomes challenging. The evolution of low-voltage wireless applications calls for one chip solutions where the RF frontend module and digital and baseband circuits can be integrated, see schematic in Figure 2.

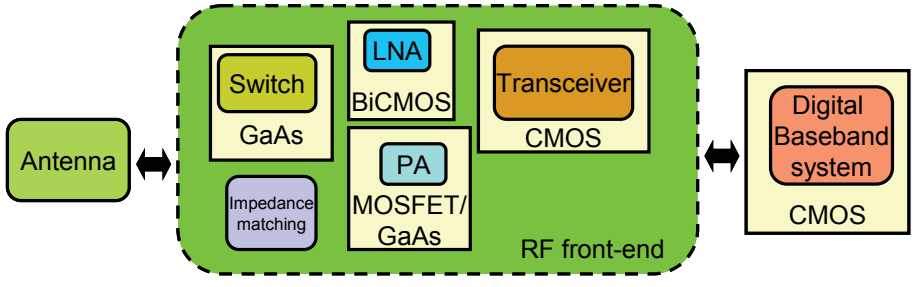

Figure 2. Schematic example of a radio communication system with antenna, RF frontend module and the digital processing block. Different semiconductor technologies are today used for the circuits, the separate chips are then stacked together.

In for example a 28 nm CMOS process, it can be challenging to achieve desired RF performance with integrated cascode MOSFET circuits due to e.g. thin gate oxides. Preferably, a single device is integrated that has a high breakdown voltage and low on-resistance to achieve high power performance and denser layout. Designing LDMOS transistors in CMOS without changing existing process steps has been reported in [29] where the RF power device was designed and integrated in a 0.18 µm CMOS process. To reduce chip size and costs, LDMOS transistors were developed and designed in this thesis for a WLAN power amplifier and fabricated in a 65 nm CMOS process without additional masks or process steps. The WLAN performance of this LDMOS device at 2.45 and 5.8 GHz is demonstrated in **Paper I**. At higher frequencies, for example X-band (8-12 GHz) for radar and communication, there are even fewer examples of integrated power devices. One example is [30] where an integrated LDMOS in 0.13 µm BiCMOS technology is demonstrated at 11 GHz, however adding masks in the fabrication process to achieve desired device properties. Since results from **Paper I** indicated that our LDMOS could be pushed into X-band, power performance in X-band at 8 GHz for this type of integrated device, is for the first time demonstrated in **Paper II**. The LDMOS transistor, which was implemented as a power amplifier to deliver high output power at high frequencies, showed a possible advantage as an integrated driver for high power GaN-based switched mode PAs. This concept is demonstrated in [14]. To deliver high

output power, the transistor may operate at high compression and close to breakdown which can cause degradation of the device and make the reliability questionable. Moreover, with the thin gate oxide of 50 Å in the 65 nm CMOS process and high fields due to a high breakdown voltage, the transistor is vulnerable to hot-carrier effects and gate tunneling which also affects the reliability and life-time performance [31]. Large-signal stress, DC stress and stress mechanisms related to the gate leakage current are investigated in **Paper II** and **Paper III**. Heading for operation in WLAN and X-band among other RF-power applications, this thesis also covers the design, fabrication and evaluation of a Si-on-poly-SiC hybrid substrate. To demonstrate the feasibility, since large wafers are attractive to foundries, 150 mm hybrid substrates were fabricated, being the first and only to this day [32][**Paper IV**]. Polycrystalline SiC (poly-SiC) was chosen due to the availability and lower cost compared to single crystalline SiC where poly-SiC also has the possibility to easily being manufactured in any size. The challenges with the implementation of the hybrid substrate lies in the wafer bonding process, achieving a void and stress-free substrate and obtaining a final substrate with controlled gettering and no electrical or lifetime degradation compared to bulk or SOI. The fabrication process together with thermal and electrical characterization is covered in **Paper IV**. The advantages in thermal and high frequency properties of the poly-SiC material makes it interesting for RF-LDMOS, and this type of transistor was demonstrated, for the first time, on the hybrid substrate in **Paper V**. Since the Si-on-poly-SiC hybrid substrate is a new unknown material which features high frequency benefits, these properties are studied in depth in **Paper VI.** There, the hybrid substrate is also compared in terms of RF losses and RF thermal behavior to other technologies such as bulk/SOI including HR-SOI and LR-SOI.

2. Theory

Depending on the application, RF power amplifiers can be based on a number of different types of transistors. For low power applications, MOSFETs [33] or MESFETS/HEMTs for III-V compounds [34] are common, while BJTs [4] or LDMOS transistors [7] are commonly used for high power applications. The output current and voltage of the transistor i.e. the DC characteristics, can give an initial insight to the RF power performance. However, a transistor operating as a RF power amplifier has a long list of figures of merit regarding performance and quality, which partly originates back to the DC characteristics but also depends on the type of operation. The output power the amplifier can deliver is dependent on the voltage and current that can be reached but also the gain. The efficiency tells us how the output power is related to the total power consumption. Another figure of merit is the linearity, which is the proportionality between the input signal and the output signal [35]. This is important in linear amplifiers, such as with class A, AB and C operation, while it is not as important for switch-mode amplifiers where class E, F or S is used [36]. To achieve desired linearity, class AB is for example typically operated with significant back-off from saturation. However, efficiency and linearity have an inverse relationship, where high linearity can be achieved but will cost in efficiency.

When searching for ways to increase the performance of a power amplifier, it is quickly evident that the maximum power, efficiency and gain are dependent on a number of factors. Non-linear effects, parasitic components and stress mechanisms can be evident and will limit the system performance. Moreover, the output power is not necessarily the power delivered to a load, unless the network has been matched in output and load impedances to ensure maximum power transfer. The following paragraphs will cover some of the parameters that have an influence on the performance of a transistor operating as a power amplifier. The sections are, among other, divided into the small-signal and large-signal case, since both these models can be helpful in explaining limits on power performance. It is however not straight forward to connect the discussion of the models to each other. Still, they can independently give an insight in what kind of effects that can be of concern regarding RF power transistors. Furthermore, the choice of substrate may influence the RF performance which is also addressed in this chapter.

2.1 Breakdown voltage and ON-resistance

The MOSFET (n-type), schematic cross-section in Figure 3a, is a three-electrode device which can amplify or switch signals. A positive gate voltage (V_g) creates an inversion layer under the gate oxide, and electrons can flow between the grounded source-electrode and drain-electrode, when a positive drain voltage (V_d) is applied. The breakdown voltage of the device is limited by the electric field at the gate drain-edge where dielectric breakdown occurs dependent on the gate oxide thickness (when $V_d > V_g$ or in OFF-state). For extremely scaled channel lengths, punch-through or breakdown between drain and source can occur before the oxide breakdown. In ON-state, a high enough field will also damage the gate oxide by hot-carrier injection (hot-carrier injection is discussed in Section 2.3).

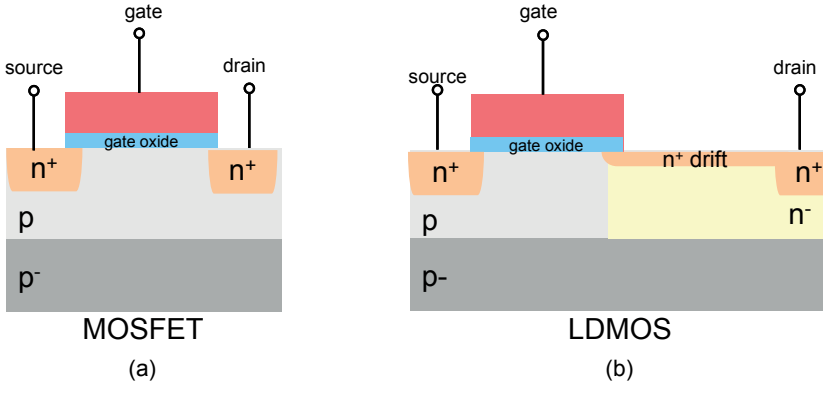

Figure 3. Schematic cross-sections of a (a) MOSFET (n-type) and (b) LDMOS (n-type) transistor.

The LDMOS transistor (n-type) in Figure 3b is basically a MOSFET but has an extended drain region to support a higher voltage and re-locate the electric field further from the gate drain-edge which reduces the risk of hot-carrier injection. Besides the advantage in re-locating the high electric field, the LDMOS offers the possibility of higher breakdown voltage. If the voltage can spread over a larger distance, the probability of impact ionization is lower and the supply voltage can be increased. When no voltage is applied to the gate and the transistor is in OFF-state, the drain voltage is supported by the reversed biased junction between p and n^- layer. A lower n^- doping and thicker layer increases the breakdown voltage but will also increase the on-resistance (R_{ON}) ($R_{ON}=V_{ON}/I_{ON}$ is illustrated in Figure 5). Since a low R_{ON} is required for high current and low losses, a trade-off in design for optimizing the two parameters has to be made. To achieve the combination of low R_{ON} and high breakdown voltage, the Reduced Surface Field (RESURF) technique can be used for lateral devices such as LDMOS transistors [37]. Having a thin n^- type layer on top of the p-type substrate in the drift region, as

pictured in Figure 4a, the p^- substrate will help deplete the n^- region from underneath and the high electric field will be located further away from the vulnerable gate-drain edge. This allows for thinner gate oxide design, which in turn can increase the transconductance (g_m) and therefore higher drain current and higher transition frequency (f_T), which results in better performance in terms of output power and increased operating frequency. The doping of the p^- substrate, p and n^- region have to carefully be calculated to ensure that the whole drift region length is utilized, compare to the case in Figure 4b. The breakdown voltage in the case of Figure 4a will be limited by the p^-/n^- vertical diode while the n^+ drift layer doping will determine R_{ON}. Keeping the n^- layer thin and highly doped, R_{ON} will stay low and at the same time, the breakdown voltage is increased. In other words, for optimization of the RESURF concept, there is a certain optimum dose that should maintain constant when deciding the n^- thickness and doping concentration.

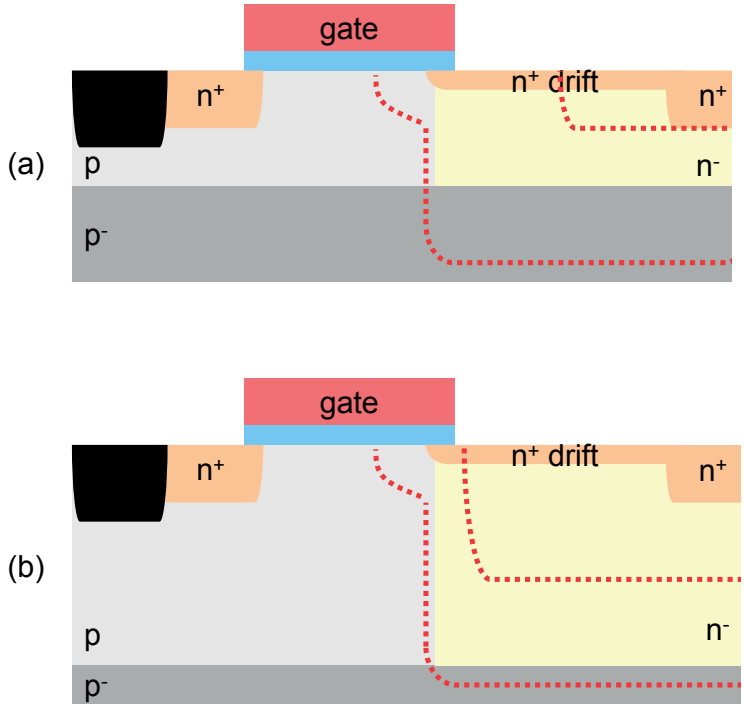

Figure 4. Schematic LDMOS cross-sections demonstrating the RESURF concept. (a) With a thin n^- layer, part of the drift region gets depleted by the help of the p^- substrate. (b) With a thick n^- layer, a high field is located near the gate-drain edge with the risk of increased hot-carrier effects.

2.2 Large-signal

R_{ON} determines the conduction power dissipation of a transistor and is defined by a number of intrinsic resistances which include e.g. the source resistance (R_{source}) and drain region resistance (R_d), besides the channel resistance. For a MOSFET, R_{source} and R_d are small compared to the channel resistance, but for a lateral device with an extended drain region, R_d becomes significant. Again, it is therefore important that the drift region doping is high to achieve a low R_{ON} and high current.

A transistor working as a power amplifier will swing between an ON and OFF-state (large-signal), illustrated in Figure 5. The dashed line represents the load line and shows at what maximum drain voltage and maximum drain current the transistor will operate.

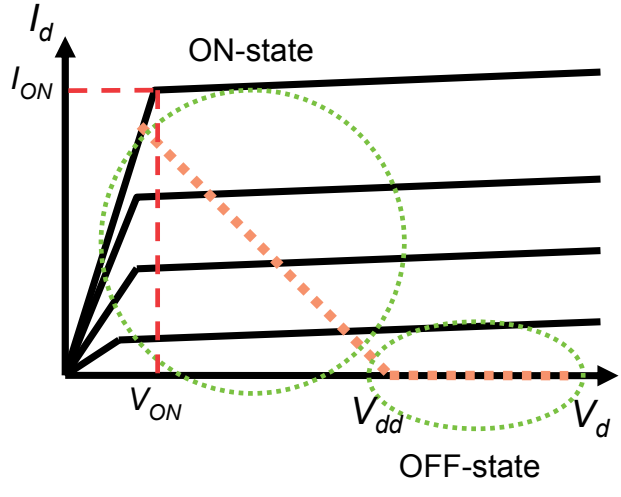

Figure 5. Illustrative graph of drain current versus drain voltage for a transistor with a load line (dashed line). R_{ON} is also illustrated as $R_{ON}=V_{ON}/I_{ON}$.

It is common for the drain voltage to reach a value two or even three times higher than the supply voltage (V_{dd}) [36] and therefore pushes the breakdown voltage to be high enough. In ON-state, R_{ON} will control how much current that is delivered where a lower R_{ON} equals to higher current. The output resistance (R_{OUT}) influences the output power in both ON and OFF-state, where a lower R_{OUT} causes a lower swing of the output voltage and accordingly results in a smaller voltage gain. The intrinsic voltage gain in ON-state is approximately:

$$A_{vi} = \frac{g_m}{g_d} = g_m R_{OUT} \qquad [1]$$

where g_m and g_d are the transconductance and drain conductance respectively. In OFF-state, although R_{OUT} approaches infinity, the output resistance in RF operation may not be treated as infinity due to parasitic capacitances. Hence, parasitic current may also be conducted when the transistor is supposed to be off (OFF-region), which in turn decreases the efficiency.

DC-measurements on a single transistor can only demonstrate the performance to a certain degree. The output characteristics from a DC-measurement tells us what currents and voltages the specific device can reach, but in order to fully evaluate the device, large-signal measurements at the intended frequency have to be performed in true operation conditions. Impedances of the power amplifier and surrounding devices, as the source and load, have to be monitored and matched to ensure maximum output power, efficiency and gain. This is performed using load-pull measurements [36] as done in **Paper I** and **Paper II**.

2.3 Stress mechanisms

As devices are downscaled, gate oxides get thinner and higher gate leakage currents follow which can cause transistor performance to degrade. Combined with high electric fields in power applications, the gate oxide integrity and stress mechanisms causing parameters to drift have to be evaluated. The MOSFET reliability is a widely studied subject, but the LDMOS as a not as old concept with a somewhat different design compared to the MOSFET needs a thorough investigation for understanding of the present stress mechanisms.

The gate leakage current can be related to the leakage current arising from stress mechanisms such as Fowler Nordheim tunneling (FN tunneling) and hot-carrier injection (HCI). FN tunneling refers to tunneling of electrons or holes through the gate oxide due to an electric field present over the gate oxide. The amount of tunneling increases exponentially with the applied electric field which makes the tunneling process easy to identify [38]:

$$J \propto E_i^2 \exp\left[-\frac{4\sqrt{2qm^*}\phi_B^{3/2}}{3\hbar E_i}\right] \quad [2]$$

where J is the current density, E_i is the electric field over the oxide, ϕ_B is the barrier height, m^* is the electron effective mass, $\hbar$ is the reduced Planck's constant and q is the unit of electronic charge.

In a MOSFET or LDMOS, the source contact is normally grounded, and in operation ($V_g>0$ and $V_d>0$), the FN tunneling is mostly located at the

source gate-edge where the electric field over the oxide is the greatest, see Figure 6. Moreover, at other biases, as in OFF-state or close to OFF-state (low gate voltage and high drain voltage) the field direction may be favorable for electrons to tunnel from the gate to drain instead.

Hot-carrier injection is a process that originates from electrons or holes gaining a kinetic energy that can surmount the barrier between the p-type substrate and the gate oxide, as illustrated for a p-type substrate in Figure 7. The barrier is ~3.2 eV for electrons and ~4.7 eV for holes, based on bandgap and electron affinity values of silicon and oxide. The carriers can gain the energy in several ways. Drain avalanche hot-carrier injection occurs when a high voltage applied to the drain accelerates the electrons into the depletion region of the drain. The electrons create electron-hole pairs by collisions where these electrons can gain enough energy to surmount the barrier and get trapped in the oxide or show up as gate current. The holes flow back to the substrate and give rise to a substrate current, and this process has been shown in MOSFETs to be worst at $V_d=2V_g$ (maximum substrate current) [39]. Another hot-carrier mechanism is the channel hot-carrier injection which occurs when both the gate and drain voltage are high, in MOSFETs when $V_d \approx V_g$ (maximum gate current), i.e. close to saturation point [40]. Electrons in the channel are driven towards the gate oxide due to the high gate voltage, and combined with the high drain voltage that accelerates them; they can get enough energy to surmount the barrier. These conditions are commonly used to determine a MOSFETs degradation behavior in a worst case scenario. However, the voltage conditions may differ for a LDMOS due to other features such as non-uniform channel doping and larger drain series resistance compared to the MOSFET.

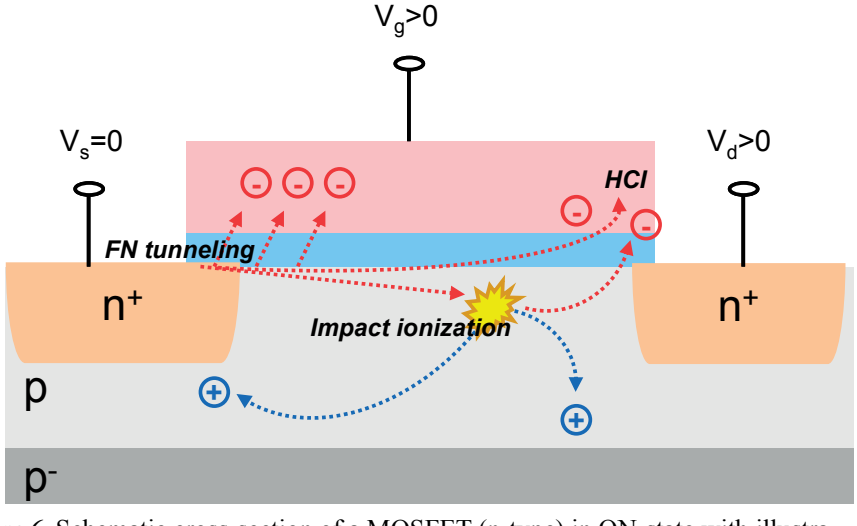

Figure 6. Schematic cross-section of a MOSFET (n-type) in ON-state with illustrative effect of FN tunneling and hot-carriers.

Both FN tunneling and HCI cause damage to the atomic structure in the oxide or the interface between the oxide and the silicon, and the carriers can show up as a gate leakage current or get trapped in the oxide. An increasing gate leakage current indicates induced defects and interface states and causes the output current to drift which degrades PA performance. Trapped charges can interfere negatively with transistor operation, e.g. for a MOSFET or LDMOS as in Figure 3. For example, negative trapped charges in the oxide increase the threshold voltage i.e. the current is reduced for a fixed bias point. Furthermore, trapped electrons in interface states can result in an increased surface depletion which increases R_{ON} [41] and a lower output current follows.

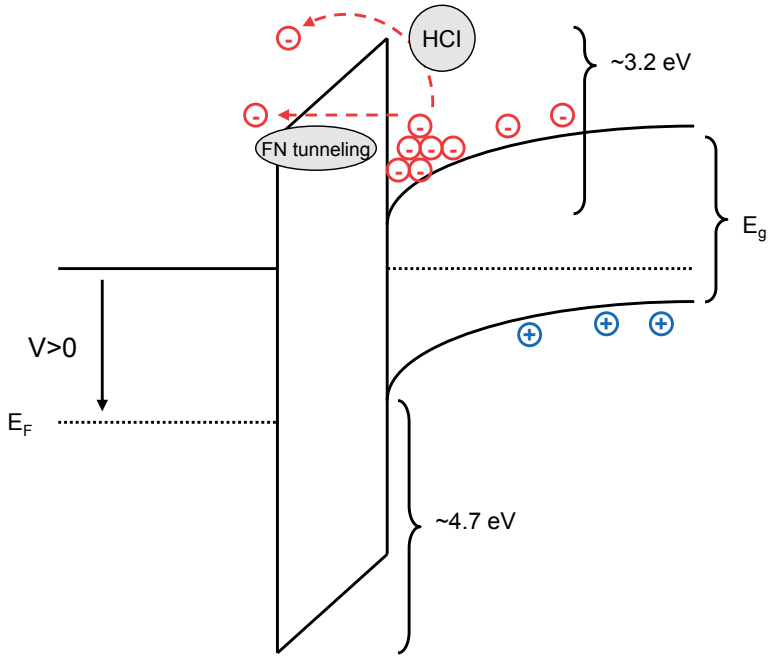

Figure 7. Energy-band diagram of the p-type substrate, the gate oxide and the gate electrode in the condition of inversion.

Over time, the transistor performance will degrade due to the damage caused by stress mechanisms where transistor parameters will be affected in different ways and some may not be affected at all. The drift behavior over a time period of a certain transistor parameter can be extrapolated and the amount of degradation during e.g. 10 years can then be predicted. It is important to remember that the oxide has a limit on the amount of charge that can pass through it before failure, the charge-to-breakdown (QBD) [42]. By integrating the injected current over time until breakdown, the QBD can be

obtained. Since the QBD is field dependent, i.e. a higher applied field equals a lower QBD [42], it is difficult to accurately estimate the life time of the gate oxide in a transistor and only a worst case scenario can be presented.

Stress mechanisms were investigated by measuring the amount of gate current at various DC bias points for our LDMOS in **Paper III** in which the gate oxide also was characterized by QBD measurements. The DC stress gives an understanding of the qualitative difference in stress effects between different operating regions of the transistor. For a power amplifier the ageing effects may look different due to the swing of applied voltage and this was investigated in **Paper II**.

2.4 Small-signal

In addition to the large-signal case, the small-signal model in Figure 8 can give insight in to how the transistor power performance can be increased and also what the limits are. The same theory applies here; to increase properties like output power, efficiency and gain in power amplifier applications, the output impedance of the transistor has to be high. The total output impedance is affected by any parasitic elements which can originate both from the transistor structure itself (intrinsic) and surrounding elements (extrinsic) at high frequencies. The small-signal drain current is modeled by a current source equal to $g_m \cdot v_g$, see Figure 8. The amount of current is affected by the output impedance of the intrinsic transistor and related to the small-signal channel behavior. The output impedance is represented by a resistance (R_{ds}) and capacitance (C_{ds}) in parallel. Many parasitic elements can be relevant in a transistor, here a few are considered for easier interpretation of the importance of high output impedance.

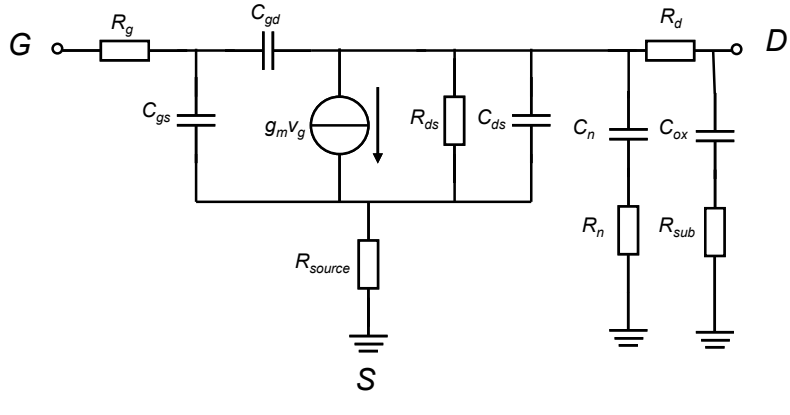

Figure 8. Small-signal model of a transistor. R_{ds} and C_{ds} represent the channel output impedance, C_n and R_n represent the n-well coupling to the substrate and C_{ox} and R_{sub} represent the extrinsic metal coupling to the substrate.

For example, parasitics representing the n-well coupling to the substrate can be found in the model in Figure 8 and are named C_n and R_n.

Extrinsic parasitics include how e.g. extrinsic metal couples to the substrate and are described by C_{ox} and R_{sub} representing the oxide capacitance and the substrate resistivity respectively. In ON-state, to achieve high current delivered to a load connected to the drain and minimize the RF losses, $R_{ds}/R_n/R_{sub}$ have to be high and $C_{ds}/C_n/C_{ox}$ have to be low. This is also the requirement to achieve the highest operation frequency possible. Furthermore, as seen in the small signal model in Figure 8, R_d (part of R_{ON}) has to be low to ensure maximum power transfer. In OFF-state, R_n/R_{sub} and C_n/C_{ox} will have large impact on the efficiency in power amplifier applications [43], because current can still flow due to these parasitics at high frequencies. For simplicity, the losses due to substrate coupling in OFF-state are combined and modeled by a capacitance C_S and resistance R_S in series which is seen by the drain node, shown in Figure 9a. The source resistance R_{source} will not be relevant in OFF-state. Therefore, the series equivalent circuit can be remodeled into equivalent parallel circuit and be included in the parallel circuit consisting of R_{ds} and C_{ds}. The total output impedance is then in the simplest way modeled as a capacitance C_P and resistance R_P in parallel, see Figure 9b, and includes both intrinsic and extrinsic parasitics such as the substrate coupling. The output resistance R_P should be high and the output capacitance C_P should be low to ensure low substrate losses and high efficiency. The relationship between the two equivalent circuits in Figure 9a and b can be calculated and R_P and C_P become:

$$R_P = \frac{1}{R_S \omega^2 C_S^2} + R_S \qquad [3]$$

$$C_P = \frac{C_S}{1 + R_S^2 \omega^2 C_S^2} \qquad [4]$$

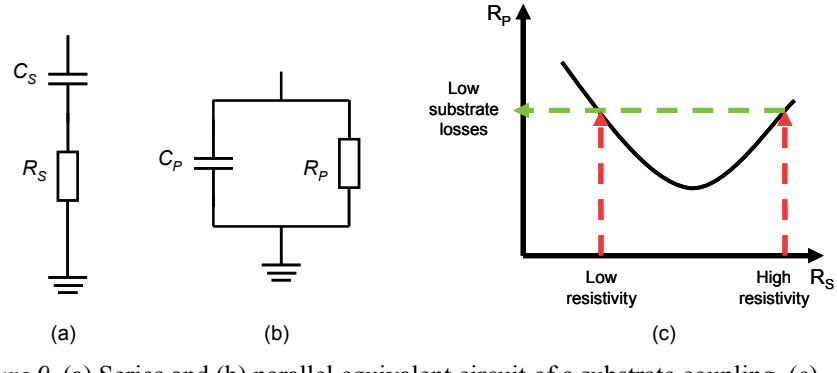

Figure 9. (a) Series and (b) parallel equivalent circuit of a substrate coupling. (c) Output resistance and equivalent series resistance dependence. Both high and low series resistance translates into a high output resistance.

2.5 Substrate influence on RF performance

Substrate engineering is one way to decrease the substrate coupling and accordingly increase the RF performance. SOI substrates have a buried oxide that reduces the capacitance to the substrate C_S and thereby the substrate losses. A thicker buried oxide implies a lower parasitic capacitance and therefore lower losses. A drawback with a thick oxide is however increased device self-heating due to the low thermal conductivity of the buried oxide. In **Paper IV-V**, a Si-on-poly-SiC hybrid substrate is presented, which consists of a thick poly-SiC substrate underneath the silicon device layer. The thick semi-insulating poly-SiC contributes with a very low C_S. The intrinsic coupling to the substrate would for example only consist of a small C_n and an insignificant R_n in Figure 8. If the extrinsic metal would be deposited directly on top of the poly-SiC, as illustrated in Figure 1d, the total amount of RF losses would be reduced even further. Furthermore, the poly-SiC exhibits a high thermal conductivity, decreasing the effect of self-heating compared to SOI (investigated in **Paper IV** and discussed in more detail in the Section 3.2.2).

If only the substrate contribution to the RF losses of a device is to be found, open-pad structures can be measured on top of the substrate and the relationship between substrate resistivity and minimum losses can be evaluated with the help of Equation 3 and 4. The relationship in Equation 3 is plotted illustratively in Figure 9c. The substrate resistivity is related to the equivalent series resistance R_S and the graph in Figure 9c shows that a both a high and a low R_S would result in a high equivalent parallel resistance R_P, which indicates low substrate losses. HR-SOI utilizes high resistivity silicon underneath the buried oxide to increase R_S and thereby also the output impedance. In the same way is the output impedance increased with LR-SOI where the silicon underneath the buried oxide is instead of very low resistivity. Consequently and in line with the behavior plotted in Figure 9c, medium resistivity silicon would be the least favorable in terms of low substrate losses.

The equivalent R_P could be measured by using an open-pad structure and a network vector analyzer (NVA) or a HF (high frequency) impedance analyzer. The HF properties of the substrate can also be characterized using crosstalk structures together with the NVA, where the propagation of the signal in the substrate is measured. Typical measurement structures can be seen in Figure 10. The NVA measures S-parameters (scattering) which can be converted to admittance parameters (Y-parameters), e.g. S_{11} to Y_{11}:

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0 \qquad [5]$$

where Y_0 is the termination on the port that is not measured. From Y_{11}, R_P and C_P can be extracted and crosstalk is extracted from S_{21} as:

$$R_P = \frac{1}{\mathrm{Re}[Y_{11}]} \quad [6]$$

$$C_P = \frac{\mathrm{Im}[Y_{11}]}{2\pi f} \quad [7]$$

$$crosstalk = dB(S_{21}) = 20 \cdot \log(|S_{21}|) \quad [8]$$

Figure 10. Measurement structures for measuring (a) equivalent R_P and (b) crosstalk. The structures are not shown in the same scale.

Paper VI includes characterization and modeling of different substrates intended for high frequency power applications, such as poly-SiC, SiC, HR-SOI and LR-SOI. If the assigned equivalent model described by Equation 3 and 4 is correct, constant R_s and C_s values corresponding to the material properties are found. If the extracted parameter values are not constant with frequency, the model is either wrong for the measured structure, or the parameter values are in fact varying with frequency. Frequency dependent behavior is addressed in the next section.

Not only coupling to the substrate of a single device is of importance for the overall system performance at high frequencies. Noise transmitted from one circuit to another, i.e. crosstalk, is especially of concern as digital blocks and RF circuits get integrated on to the same chip, i.e. mixed-signal. The analog transistor is especially sensitive to nearby digital switching noise which can propagate in the substrate and interfere with the analog amplifier [44]. This would for example have to be considered for the integrated PA in **Paper I-II**.

The coupling in the substrate between different blocks can be measured using the crosstalk structure in Figure 10b and can be extracted from S-parameters with Equation 8. The amount of crosstalk is obviously also dependent on the resistive and capacitive behavior of the substrate. To overcome crosstalk issues in bulk CMOS, several techniques are available, such as PN junctions with a triple-well process or guard rings which shunt signals

to ground [45]. These techniques add more complexity and cost to the fabrication process. Moreover, designing for low crosstalk gets more difficult as operating frequencies are increasing, since signals are more easily coupled via parasitic capacitances (impedance decreases with frequency as $Z=1/j2\pi fC$). With SOI it is easier to decrease the amount of crosstalk due to the isolating oxide underneath the devices [46], but as mentioned, the crosstalk will increase at higher operating frequencies. To enhance SOI, HR-SOI has demonstrated better RF performance where the high resistivity silicon underneath the buried oxide prevents the signals from transmitting as easily [47]. Also LR-SOI reduces crosstalk substantially, since the signals transmitting in the substrate shunts to ground efficiently in the same way as guard rings due to the very low resistivity silicon [19]. Also GP-SOI (ground plane-SOI) shows similar behavior as LR-SOI [48].

2.6 Frequency dependence

Parasitic capacitances are dependent on the relative permittivity ε_r (dielectric constant) of the material. The dielectric constant is based on how an external field interacts with the polarization mechanisms in the material. The polarization which creates an internal electric field can arise from e.g. ions, dipoles, grain boundaries, interfaces and valence electrons in the atoms. If the external field is applied with an AC signal, the various polarization mechanisms in the material respond to the electric field based on how fast the switching occurs. Consequently, the amount of polarization and hence the dielectric constant of the material becomes frequency dependent [49].

The time it takes for the system to reach equilibrium after some sort of perturbation is referred to as the dielectric relaxation time τ. Eventually, the rate, or the frequency, of which the perturbation takes place, is high enough that the rate of relaxation can not follow, and there are no polarization mechanisms left to respond in the material. This information suggests that different types of materials due to their structural composition can act very differently at high frequencies, e.g. poly-SiC or doped silicon.

In silicon, the majority carriers response time is very short and the time to return to electrostatic equilibrium is strongly dependent on the silicon resistivity as $\tau=\rho\cdot\varepsilon$ [38] where ρ is the resistivity and ε is the permittivity ($\varepsilon=\varepsilon_r\cdot\varepsilon_0$ where ε_0 is the vacuum permittivity). Consequently, silicon will "relax" at a certain high frequency and behave completely capacitive like a dielectric. For example, a medium resistivity substrate, e.g. MR-SOI of ρ=10 Ωcm relaxes at around 100 GHz while a high resistivity substrate, e.g. HR-SOI of ρ=1 kΩcm relaxes at around 1 GHz. This relaxation of silicon is seen in **Paper VI** and is discussed in Section 3.2.3.

Small-signal S-parameter measurements across the frequency band are important when investigating the RF properties of a substrate. Trying to ex-

pand the explanation of the substrate losses further, impedance spectroscopy (dielectric spectroscopy) [50] can be utilized where impedance at frequencies ranging from mHz up to MHz can be measured. This can give more understanding of the processes occurring in the material that may vary with frequency and in the end may influence the amount of substrate losses. The relaxation mechanisms will show up as transitional peaks in a spectrum of dielectric constant versus frequency. As the frequency increases, fewer processes will respond and the dielectric constant decreases. Simple relaxation mechanisms, as dipole or ionic polarization, can be modeled by the Debye relaxation model [51]. In **Paper VI**, it was seen that single crystalline SiC showed no relaxation peak across the frequency spectra, indicating no change in polarization at the measured frequencies. However, in **Paper VI** it was seen that poly-SiC revealed a complex and broad transition in relaxation mechanisms. Considering the permittivity over a wide frequency spectrum, the permittivity is a complex quantity. One way to describe the permittivity as a function of frequency for a material with the broad transitions as in poly-SiC is using the Havriliak Negami relaxation model [51]:

$$\hat{\varepsilon}(\omega) = \varepsilon'(\omega) + \varepsilon''(\omega) = \varepsilon_\infty + \frac{\varepsilon_s - \varepsilon_\infty}{\left(1 + (i\omega\tau)^\alpha\right)^\beta} \qquad [9]$$

where ε_∞ is the dielectric constant at high frequencies, ε_s is the static low frequency dielectric constant, τ is the relaxation time and α and β are constants describing the broadness and asymmetry of the transitions. The real part of $\hat{\varepsilon}(\omega)$ is related to the energy stored in the material (the dielectric constant) while the imaginary part is related to the losses in the material. The relaxation mechanisms of the poly-SiC material are further discussed in Section 3.2.3.

3. Results and discussion

This chapter focuses on the most important findings, explaining how challenges have been overcome and how the outcomes can be used in practice. The chapter is divided into two main sections with sub-sections. The first section concerns results and discussion of the integrated PA and related observations regarding electrical and thermal stress. In the second section, the Si-on-poly-SiC hybrid substrate is discussed, with a brief interlude about the material characterization followed by a more in depth discussion about electrical characterization and RF losses.

3.1 Integrated PA

For high power WLAN applications, cascode MOSFET is the solution for integrated 65 nm CMOS chips today. There is a need to decrease size and cost of WLAN PA which implies requirements for an integrated PA. When integrating RF devices in CMOS, additional mask or process steps are preferably avoided to maintain cost-effectiveness and avoid changes to existing device parameters. However, it can be challenging to achieve optimal performance when not adding extra masks or process steps to a CMOS process since it is usually adapted for low-power/voltage applications. In **Paper I**, LDMOS transistors were designed and manufactured at foundry in a 65 nm CMOS process without adding extra process steps or masks.

A test chip was fabricated with several transistor sizes and a schematic cross-section of a fabricated LDMOS can be seen in Figure 3b. The largest transistor, a 2x14 unit cell with W/L=200/0.35 µm and a total gate width of 5.6 mm was bonded to a PCB testboard, together with impedance matching components at the input and output. A photo of the testchip and the PA testboard can be seen in Figure 11. The output characteristics of a ten-finger LDMOS with W/L=200/0.35 µm, can be seen in Figure 12 where the saturation current reaches 750 mA/mm at V_g=5 V. Dynamic IV-sweeps are also presented in the same graph and are discussed in Section 3.1.1.

It is essential for a PA to have a high breakdown voltage and low R_{ON}, however, a high breakdown voltage is not a common feature for low-voltage CMOS. By correctly designing the n^+ drift-region length while applying the RESURF concept, R_{ON} was kept small, around 2.4 Ωmm, and a 10 V breakdown voltage was obtained, limited by the n-well/p-well junction. The 65

nm CMOS process brings a supply voltage of 3.3 V, but with the 10 V breakdown voltage, a 5 V supply voltage can also be used. On-chip RF measurements with a network vector analyzer were performed and de-embedded S-parameters were used to extract f_T=20 GHz and f_{max}=18 GHz, which is well enough for the intended application.

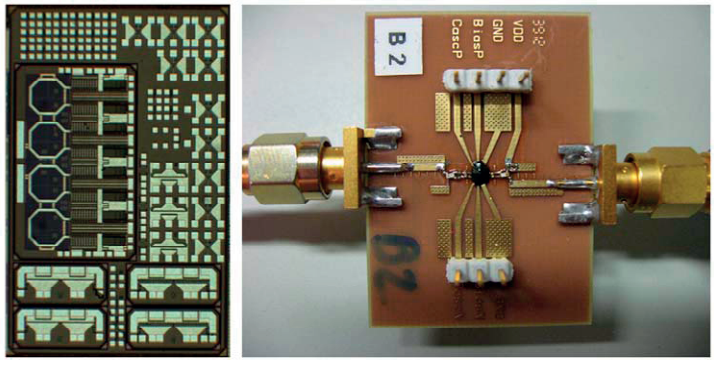

Figure 11. Photo of (a) the processed testchip. Chip size is 2.5 mm x 4 mm. The four large structures at the bottom of the chip are the LDMOS transistors with a 5.6 mm gate width (2x14 unit cells with W/L=200/0.35 µm). (b) The PA testboard with a 5.6 mm LDMOS transistor. [**Paper I**]

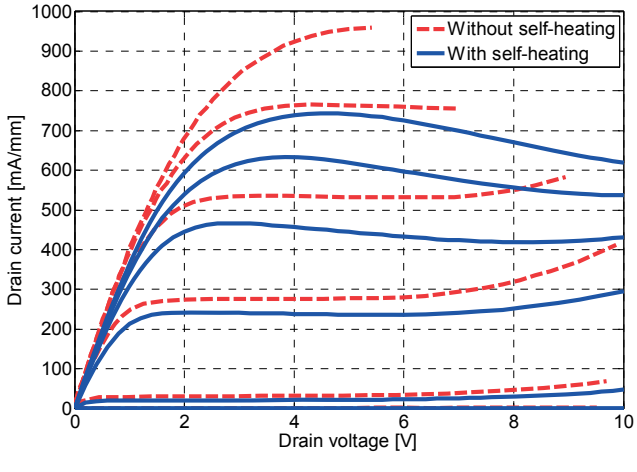

Figure 12. Output characteristics of the W/L=200/0.35 µm LDMOS with and without self-heating effects. V_g= 0, 1, 2, 3, 4, 5 V. A pulse length of 0.2 µs was used for the dynamic sweep. [**Paper II**]

By performing load-pull measurements, the performance at 2.45 GHz as well as 5.8 GHz with a 14 x (W/L=200/0.35 µm) transistor (total gate width of 2.8 mm) at both a supply voltage of 3.3 V and 5 V were investigated.

High output power capacity was demonstrated at both frequencies, above 30 dBm at 2.45 GHz and V_{dd}=5 V at ~3 dB compression. The device could not be driven to full saturation at 5.8 GHz due to limits in input power.

Performance of WLAN PA at 2.412 GHz (lowest channel in 2.45 GHz WLAN band) was demonstrated with the PA test board and 32.8 dBm output power (P_{OUT}) was delivered at 1 dB compression, the highest reported value using this technology to the author's knowledge, with power added efficiency (PAE) of 50% and 8 dB gain.

A reference design using PA cascode with two 3.3 V MOSFETs on a testboard was also investigated and showed similar results, demonstrating the feasibility of the fabricated LDMOS.

The small-signal measurements indicated that considerable gain could also be achieved at higher frequencies than 5 GHz. At X-band, there are no reports on integrated LDMOS in 65 nm CMOS without process steps or masks added. Thus, load-pull measurements were performed at 8 GHz, demonstrated in **Paper II**. At higher frequencies and large transistor sizes, the real part of the impedance appears closer to the edge in a Smith chart and accordingly, impedance matching with the tuners was difficult to achieve. To be able to tune the input and output impedances at 8 GHz, a transistor size of W/L=200/0.35 µm was chosen for evaluation. The results showed over 300 mW/mm output power density and 22% PAE at a supply voltage of 5 V and 4 dB compression, see power sweep in Figure 13.

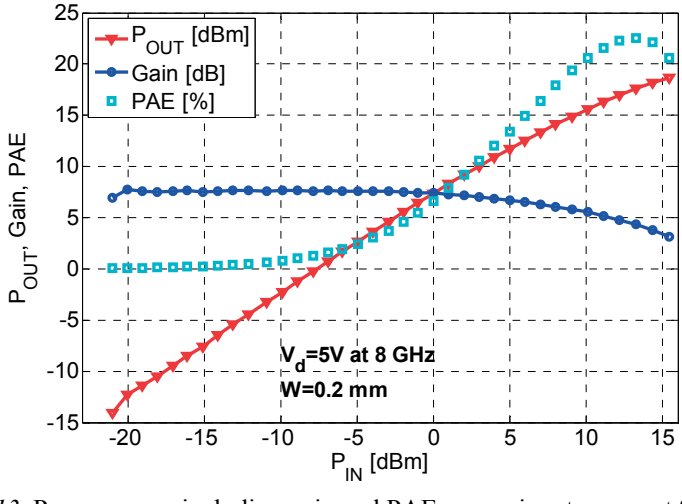

Figure 13. Power sweep including gain and PAE versus input power at 8 GHz and V_d=5 V for a LDMOS with W/L=200/0.35 µm. [**Paper II**]

The performance demonstrates the benefits of the device for switching applications where high power is of primary importance and linearity is secondary. Furthermore, the device can also be expected to be useful as an integrated driver for GaN-based switch-mode PAs [14, 52]. Another version of the LDMOS was also fabricated with a more aggressive design and a channel length of L=0.28 μm. These transistors have higher g_m and on-current than the one with L=0.35 μm. Due to the shorter channel, f_T and f_{max} increased to 25 GHz and 29 GHz respectively. Power measurements at 3.3 V showed correspondingly higher output power. However, operation at 5 V was not reliable due to a lower ON-state breakdown.

3.1.1 Degradation effects

Performance of any device can degrade over time i.e. the device life time can shorten and unwanted effects in device parameters can appear. In a power transistor, high fields combined with the thin gate oxide add to the stress induced mechanisms affecting the device reliability. The transistor performance is especially vulnerable when operating at a high level of compression and close to breakdown. For example, when operating the LDMOS at a supply voltage of 5 V, the output voltage can easily reach twice the supply or more depending on type of operation, and therefore reach close to the breakdown voltage of 10 V. Since the gate oxide plays an important role in transistor reliability, the amount of gate current can be related to any leakage current through the gate oxide which depends on some of the induced stress mechanisms [53, 54]. In other words, the gate current constitutes charges caused by various stress mechanisms which moreover causes defects in the oxide such as trapped charges and interface states. In **Paper III**, an Agilent E5288A Atto Sense Unit connected to an Agilent B1500A parameter analyzer was used to monitor very low gate currents in the LDMOS. The gate current was measured at the same time as a drain current-sweep was performed, and the gate current versus drain voltage and gate voltage could be plotted as in Figure 14. As seen in the graph, the gate current shows distinct characteristics related to the various stress mechanisms. It is observed that the gate current is very dependent on the gate voltage as well as the drain voltage in certain operation areas. In order to understand the gate current behavior, different bias points in Figure 14 were chosen for long-term DC stress and drift of transistor parameters were monitored. A combination of the gate current behavior in Figure 14 and the theory of stress mechanisms such as FN tunneling and hot-carrier injection were applied for understanding and evaluation.

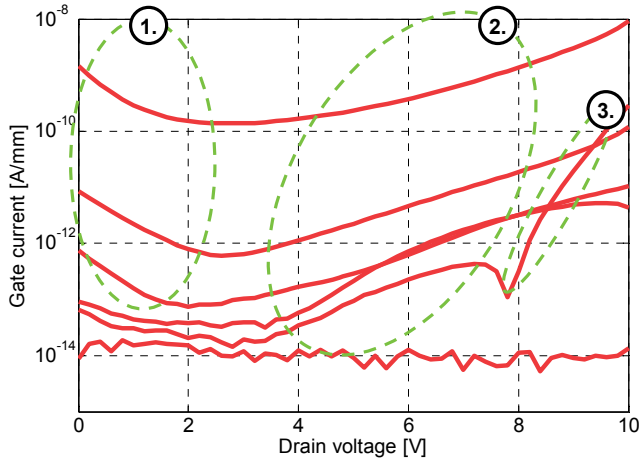

Figure 14. Gate current versus drain voltage for the W/L=200/0.35 µm LDMOS. V_g= 0, 1, 2, 3, 4, 5 V from bottom to top curve. Gate current is negative beyond ~8 V for V_g=1 V. [**Paper III**]

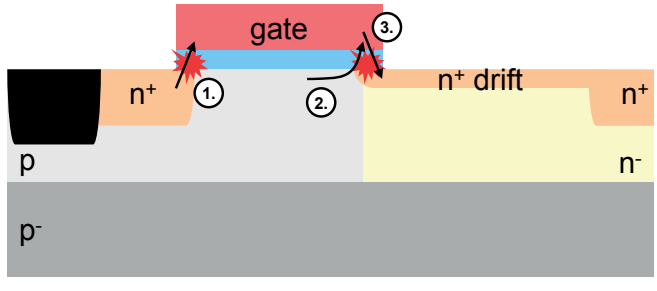

Figure 15. Schematic cross-section of the W/L=200/0.35 µm LDMOS showing the different stress mechanisms. (1) Fowler Nordheim tunneling and (2) hot-carrier injection at high gate voltage and high drain voltage. Fowler Nordheim tunneling is also present at low drain voltage but evenly across the whole gate oxide. (2) Hot-carrier injection due to high drain voltage. (3) FN tunneling from gate to drain at a low gate voltage and high drain voltage.

As seen in Figure 14, the gate current increases exponentially with gate voltage at zero drain bias. This behavior corresponds to FN tunneling, evenly distributed over the gate oxide. As the drain voltage increases, the FN tunneling decreases at the drain-edge due to the lower field and most of the FN tunneling is located at the source-edge, illustrated in Figure 14 and 15 with (1). The field over the drain-edge increases as the drain voltage is increased, promoting hot-carrier injection (2) and the gate current increases. At a high drain voltage and low gate voltage, it is moreover observed in Figure 14 that at e.g. V_g=1 V, the gate current starts to decrease around V_d=7 V and even

reverse its polarity. This is FN tunneling from the gate to the drain edge due to the beneficial field direction at that point (3).

Stress damages the gate oxide in different ways which causes degradation and drift of various transistor parameters. The DC-stress results in **Paper III** indicated that FN tunneling induces interface states and only a small amount of trapped oxide charge, supported by that thin oxides has negligible electron trapping since the electrons tunnel directly to the gate electrode [42]. This degradation is observed as an increased subthreshold swing and threshold voltage due to electrons occupying the interface states. When hot-carrier injection dominates, the threshold shift was low and the induced defects are mainly located at the gate-drain overlap region. This stress mechanism resulted in an increased R_{ON} due to reduced mobility by the build-up of negative charge from interface states/trapped electrons [41].

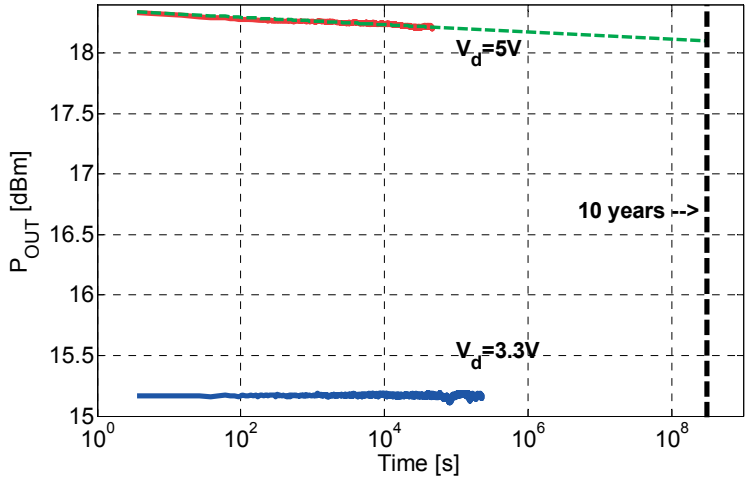

Figure 16. RF-stress measurements with output power versus time at supply voltage V_d=5 V and 3.3 V. The data for V_d=5 V is extrapolated to 10 years. [**Paper II**]

The DC-stress describes the effects at static bias over time in a quiescent point and can help in the understanding of stress mechanisms. But for a transistor operating as a power amplifier, not only the quiescent point is of importance, but the whole bias region which the load line covers, see Figure 5. In **Paper II**, long term large-signal stress was performed by continuously feeding power to the amplifier while measuring the output power and other system parameters. It could be observed that the threshold voltage was unaffected; supporting that FN tunneling is not significant. Meanwhile, a drift in R_{ON} was seen suggesting hot-carrier injection located at the gate-drain overlap. The output power drift was extracted at both 3.3 V and 5 V supply voltage. The drift of output power was insignificant at 3.3 V as shown in Figure

16. At 5 V, the output power was extrapolated to 10 years, showing a ~5% degradation as seen in Figure 16. From Figure 14 it can be concluded that the low gate currents make stress mechanisms insignificant when operating at a supply voltage of 3.3 V. However, when operating at 5 V, gate currents are higher, and stress mechanisms such as FN tunneling and hot-carriers play a larger role which can affect the transistor performance.

The magnitudes of power densities dissipating through the transistor and substrate have an impact on the device performance which makes temperature a critical parameter especially when dealing with RF-PA [22]. When comparing the effects of DC stress to RF stress in a quiescent class AB point, one can argue if the RF case may show larger amount of degradation since the load line covers a larger variety of biases, both high gate and drain voltages, compared to the DC case. However, a low efficiency of the transistor translates into heat and the high temperature decreases the mobility, which, on the other hand, may decrease the amount of hot-carriers due to a lower current [55].

Measuring output characteristics with dynamic bias, where voltage is applied with a pulse length of 0.2 μs, eliminates self-heating and can then be compared to a static DC measurement to evaluate the extent of thermal effects. Output characteristics of the LDMOS with and without self-heating are shown in Figure 12. It is evident from Figure 12 that the temperature in the transistor at steady-state condition is high, and can be estimated to over 100 ºC using the thermal resistivity of silicon and considering the transistor as a point source [21]. Thermal dissipation through the substrate controls the device self-heating and a high conductivity material underneath the device layer may help decrease the self-heating effects. In **Paper IV**, the Si-on-poly-SiC hybrid substrate is demonstrated which utilizes the higher thermal conductivity of the poly-SiC to reduce self-heating. At the same time, RF losses can be decreased since poly-SiC is semi-insulating which improves power performance.

3.2 Si-on-poly-SiC hybrid substrate

Si-on-poly-SiC hybrid substrates were fabricated using 150 mm high resistivity (~6 MΩcm) poly-SiC wafers together with commercial SOI wafers. The whole fabrication process is explained in detail in **Paper IV** and an illustration of the fabrication process can be seen in Figure 17.

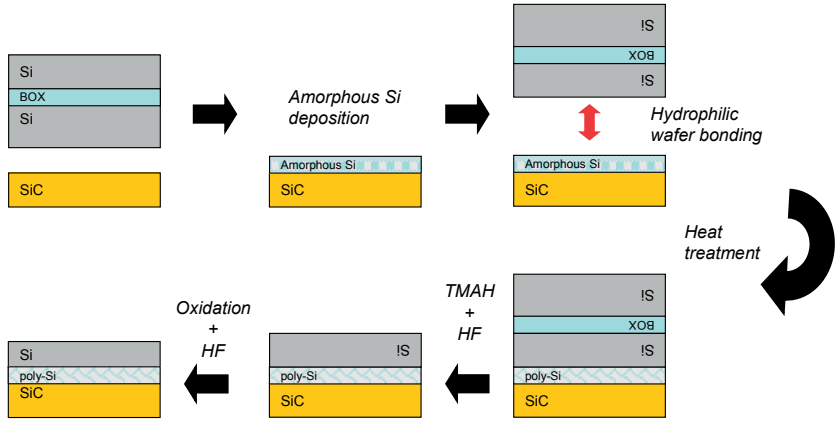

Figure 17. A brief illustration and schematic cross-sections of the Si-on-poly-SiC hybrid substrate fabrication. Layer thicknesses are not according to scale.

The fabrication of the hybrid substrate is based on hydrophilic bonding of the poly-SiC wafer and the SOI substrate. Several difficulties can be encountered when performing this type of bond, especially with larger wafer sizes. The surfaces need to have low surface roughness for a successful bond and any contamination before bonding can cause voids in the interface, decreasing the chip yield. The root-mean-square roughness (rms) was 180 nm of the as-received poly-SiC surface which was improved to 10 nm after mechanical lapping. To achieve a sufficiently smooth surface for wafer bonding, 1 µm amorphous silicon (α-Si) was deposited on top of the poly-SiC, see Figure 17, followed by chemical mechanical polishing (CMP). The rms was improved to 0.17 nm after CMP of the α-Si. The α-Si layer also provides another benefit, acting as a gettering layer [56]. Furthermore, it shields the device layer from the poly-SiC interface where extensive surface recombination can take place. To decrease the amount of voids and avoid cracking from the bonding process, a rapid thermal treatment was performed before the following furnace anneal. During the heat treatment, the amorphous silicon re-crystallized into polycrystalline silicon (poly-Si), verified by transmission electron microscopy (TEM). The TEM micrograph in Figure 18 presents the whole stack of the hybrid substrate with two interfaces and it is moreover observed that the bond interface seems to be free from defects.

The high temperature anneal can cause stress in the material which would make the substrate difficult to handle in following process steps and provide undesirable effects in electrical properties. It was confirmed by Raman and XRD-measurements that the silicon layer was stress free. Photographs of a final void free hybrid wafer together with another processed hybrid wafer are shown in Figure 19.

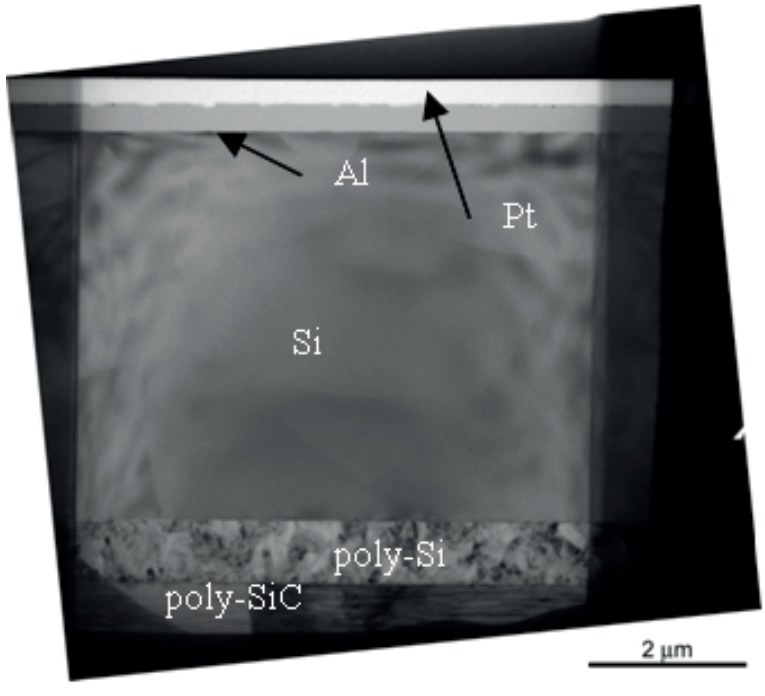

Figure 18. TEM micrograph of cross-sectional overview of the Si-on-poly-SiC hybrid substrate. [**Paper IV**]

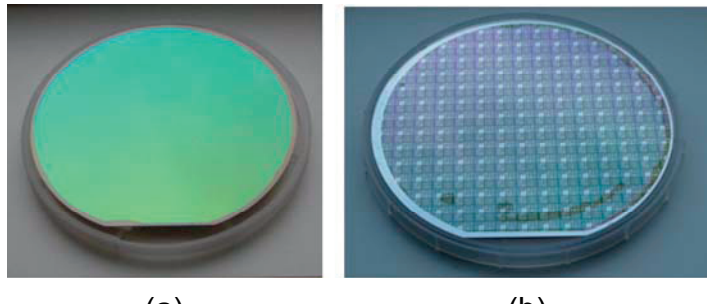

Figure 19. Photographs of (a) a stress free 150 mm Si-on-poly-SiC hybrid substrate with no visible voids or defects and (b) a fully processed hybrid wafer. [**Paper IV**]

3.2.1 Electrical behavior

To verify the electrical performance of the hybrid substrate, several electrical devices and test structures were processed on the hybrid substrate as well as on a LR-SOI substrate for comparison. A fully processed hybrid substrate can be seen in Figure 19b. Capacitor and charge-to-breakdown measurements showed that the gate oxide was almost equal on both the hybrid substrate and the SOI reference and that the targeted oxide thickness was reached. No increase of interface states or oxide charge was observed. The top-silicon device layer was characterized by circular diodes consisting of an n^+-diffused region in the p-device layer. Both the hybrid substrate and the SOI reference showed some non-ideal characteristics indicating generation/recombination in the device layer. Nonetheless, successful LDMOS transistors were fabricated and demonstrated for the first time on this type of hybrid substrate in **Paper V**, showing better or similar performance compared to the SOI reference. Output characteristics of LDMOS transistors with W/L=50/2 µm can be seen in Figure 20 for both types of substrates. Since both the hybrid substrate and the SOI reference followed the same device fabrication process and transistor performance is surface dependent, similar performance was expected. Any difference could arise from gate lithography and p-base surface doping. From all the device measurements it can be concluded that there is no degradation going from SOI to the Si-on-poly-SiC hybrid substrate.

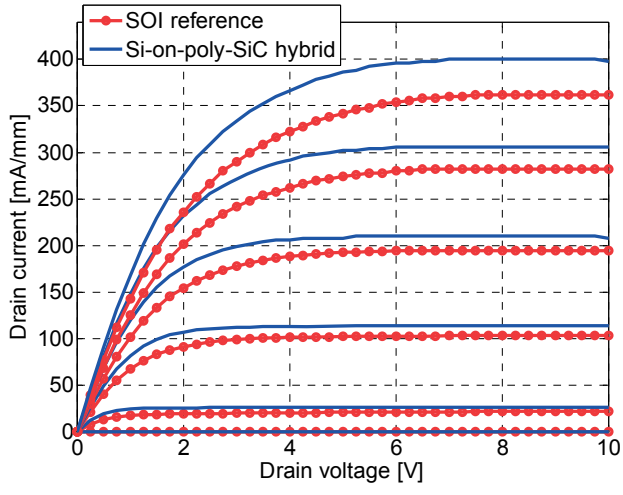

Figure 20. Static output characteristics of W/L=50/2 µm LDMOS transistors on the Si-on-poly-SiC hybrid substrate and the SOI reference respectively. V_g=0-10 V, 2 V/step and the hybrid substrate is compensated for the same (V_g-V_t) with +1 V. [**Paper V**]

A distinct difference between the hybrid substrate and the SOI reference is the potential distribution through the material as demonstrated in **Paper V**. The SOI substrate has the low resistivity silicon substrate that acts as a ground plane directly underneath the buried oxide, helping to deplete the n-well from beneath, aiding a high breakdown voltage. The hybrid substrate has on the other hand a potential distribution through the whole substrate since it acts as an insulator, implying that the depletion of the n-well is not as effective and the breakdown voltage is not as high. To overcome this it is possible to for example place a deep p^+ implant underneath the n-well. This p^+-layer could be obtained by doping the poly-Si layer itself.

3.2.2 Thermal behavior

The heat dissipation in the substrates was evaluated by measurements on calibrated resistors where the calibration was performed on a hot chuck at low power densities. Four-point probe IV-measurements were performed to get the temperature rise versus applied power density from which the thermal resistance could be extracted. The total thermal resistance is represented by all the layers and their respective thermal conductivity. The thermal conductivity of silicon and silicon dioxide are well-known, 1.6 $Wcm^{-1}K^{-1}$ and 0.014 $Wcm^{-1}K^{-1}$ respectively [57]. These values clarify how the buried oxide in SOI can cause problems with self-heating. Regarding 6H-SiC, the thermal conductivity has been reported as 4.9 $Wcm^{-1}K^{-1}$ [26] but the 6H-SiC used in these measurements has a thermal conductivity of 3.5 $Wcm^{-1}K^{-1}$ [58]. Due to grain boundaries, the poly-SiC has a lower value, here 2.8 $Wcm^{-1}K^{-1}$ [58]. In **Paper IV**, the total thermal resistance of the hybrid substrate was shown to be reduced, 2.5 times lower compared to the SOI reference. Considering the large differences in thermal conductivity of the materials in each of the substrates, the measured difference in thermal resistance was expected to be higher. The heat dissipation through a substrate consisting of several layers is complex and a possible explanation is added thermal resistance from layer interfaces and parasitic layers such as thin oxides. In [58], 2D electrothermal simulations showed that the poly-Si layer could represent up to one third of the total thermal resistance. This emphasizes the importance of this layer being as thin as possible.

3.2.3 High frequency behavior

Even though the DC measurements showed successful results, RF performance has to be studied on devices on the hybrid substrate. As mentioned in Section 2.4, at high frequencies, the total amount of RF losses are determined by both intrinsic and extrinsic losses. Extrinsic losses are related to the losses in the substrate and the equivalent parallel resistance R_P should be high while the equivalent parallel capacitance C_P should be low to minimize

those losses. Moreover, the substrate will not affect or degrade R_{OUT} of a transistor in ON-state and enhances the RF performance in OFF-state. Also crosstalk is of importance and here investigated since it describes the transmitted noise through the substrate between components.

High frequency properties of poly-SiC are not as commonly reported as those of single crystalline SiC (6H-SiC), hence, to get a relevant comparison of poly-SiC and 6H-SiC to SOI, silicon substrates of various resistivity as well as poly-SiC and 6H-SiC were studied regarding RF properties in **Paper VI**. Test structures for RF measurements were fabricated on five different substrates, 6H-SiC (~10^{10} Ωcm), poly-SiC (~10^{7} Ωcm), HR-Si (~1 kΩcm), MR-Si (~10 Ωcm) and LR-Si (~1 mΩcm). The test structures included designs for measuring an equivalent R_P and crosstalk with a 1-port and 2-port setup respectively, with the structures lying directly on a grown oxide on the silicon substrates. The measurements were performed with a network vector analyzer and high frequency probes using SOLT calibration. The NVA provided measured S-parameters where R_P was extracted as $1/\mathrm{real}(Y_{11})$ and crosstalk in dB as $20\cdot\log(|S_{21}|)$.

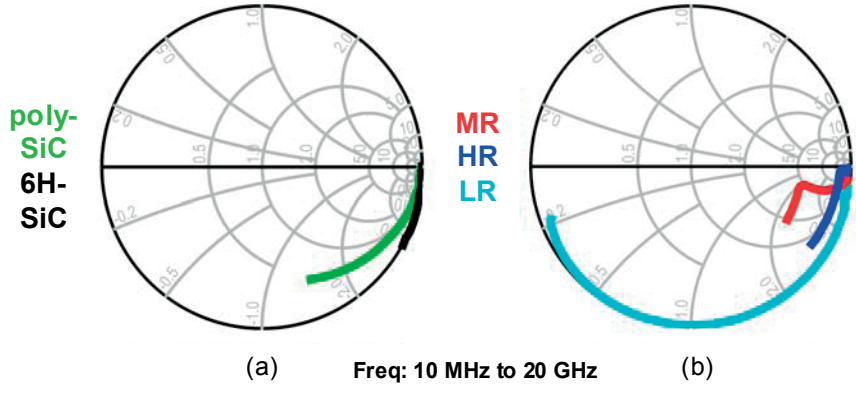

Figure 21. Smith charts with measured parameter S_{11} for (a) the silicon substrates and (b) the SiC substrates. [**Paper VI**]

Silicon carbide is semi-insulating implying that it behaves capacitive; hence a thick SiC substrate would contribute with a very low substrate capacitance in e.g. a power transistor. Moreover, SiC is highly resistive which results in a high equivalent parallel resistance R_P, i.e. it does not reduce the output impedance of e.g. a power transistor. The S_{11}-parameters were measured using a 1-port setup and are shown in Smith charts in Figure 21. It is observed that 6H-SiC shows only capacitive behavior with very high impedance, lying in the edge of the Smith chart, see Figure 21a. However, the poly-SiC, which also shows capacitive behavior, has an additional resistive component. The silicon substrates behave according to Equation 3 and to their substrate resistivity. The two parts of their respective curve relates to

the two parts of Equation 3, where the first part relates to the oxide and the second part relates to the bulk resistivity. At a certain frequency, the second part will begin to dominate over the first one, correlating to the behavior seen in Figure 21b.

In Figure 22, R_P is extracted and plotted versus frequency. Due to semi-insulating properties, 6H-SiC measured very high impedance, and R_P is therefore difficult to extract and results in a noisy curve. The poly-SiC curve shows a frequency dependent behavior for the equivalent model used, with a slope proportional to $1/\omega$. LR substrate has a slope proportional to $1/\omega^2$ according to Equation 3 and due to the low substrate resistivity. This behavior for the LR substrate can be seen in Figure 22 with difficulties measuring at lower frequencies. Furthermore, the HR and MR substrates have a frequency dependent part at lower frequencies and level out at R_S at higher frequencies according to Equation 3, which is also observed in Figure 22.

The crosstalk, expressed in dB, is plotted in Figure 23 for all the substrates. Both SiC substrates show capacitive behavior due to their insulating properties with frequency dependence across the whole frequency range. This implies that the crosstalk is very low at low frequencies but increases at higher frequencies. The HR substrate shows lower crosstalk compared to the MR substrate since the high resistivity makes it more difficult for the signals to propagate through the substrate. The LR substrate shows the lowest crosstalk due to its very low substrate resistivity which shunts the signals to ground.

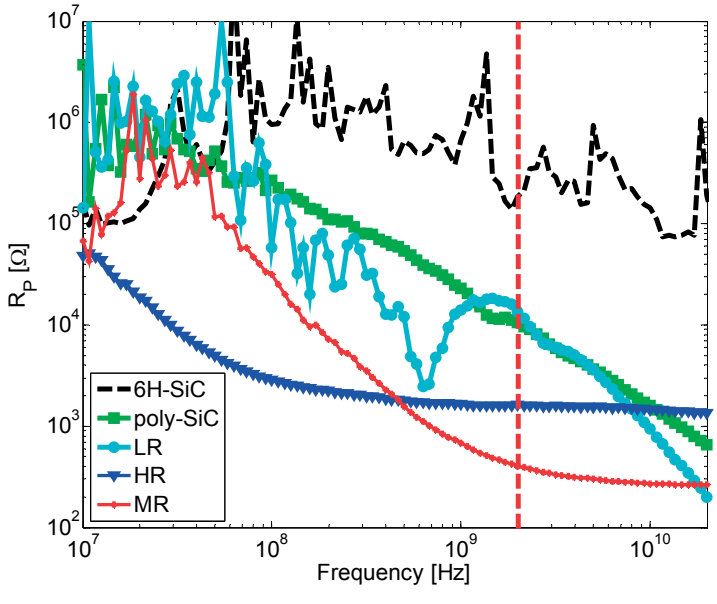

Figure 22. Extracted R_P versus frequency for the different substrates. Dashed line shows 2 GHz. [**Paper VI**]

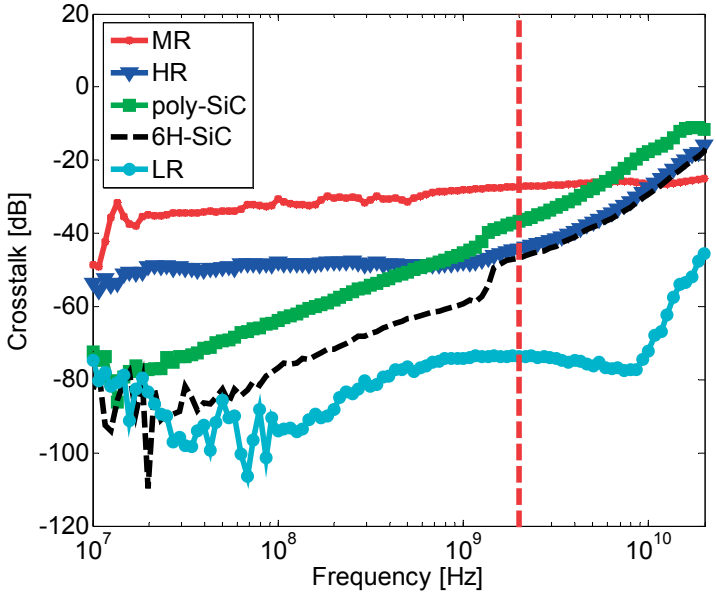

Figure 23. Extracted crosstalk versus frequency for the different substrates. Dashed line shows 2 GHz. [**Paper VI**]

From these RF measurements it is possible to benchmark the different substrates at a common operating frequency, e.g. 2 GHz. This frequency is shown in Figure 22 and 23 with a red dashed line. In terms of parallel equivalent resistance R_P, 6H-SiC has an outstanding high value compared to the other substrates. The silicon substrates behave as expected according to Equation 3 where the MR substrate has the lowest R_P. An increasing substrate resistivity (R_S) increases R_P, however, minimizing R_S also increases R_P. Here the LR substrate has an R_P even higher than the HR substrate. The poly-SiC substrate has an R_P at a level of the LR substrate. These differences in R_P correspond to any differences in RF properties for a transistor such as output power and efficiency. Both SiC substrates show capacitive behavior where a thick substrate would contribute with a low substrate capacitance which is beneficial in RF power applications.

Furthermore, simulations were performed in **Paper VI** in 3D with a numerical device simulator on all the substrates except the poly-SiC because of lack of material parameters due to complex material structure. The simulation results verified and supported the substrate RF behavior seen in the measurements.

Paper VI also includes modeling [16, 43] of the substrates to get further understanding of the RF behavior. Results indicated that the model parameters of poly-SiC were frequency dependent in contrary to 6H-SiC where model parameters behaved constant with frequency. As mentioned in Sec-

tion 2.5, this could indicate that the model is either wrong for the measured structure, or the parameter values are in fact varying with frequency.

One reason for frequency dependence can be explained by the dielectric properties, which are frequency dependent and correspond to any polarization behavior. Dielectric properties were measured up to 1 MHz in poly-SiC by impedance spectroscopy, revealing complex and broad transitions in the relaxation mechanisms. These are probably a result of defects or grain boundaries in the polycrystalline material and can possibly explain the frequency dependent behavior. Relaxation processes were also observed at high frequencies for HR silicon as the relationship $\tau=\rho\varepsilon$ conveys that the relaxation time for the majority carriers is strongly dependent on the silicon resistivity. This implies that a HR silicon substrate of 1 kΩcm has a dielectric relaxation time of ~1 ns corresponding to a relaxation frequency of 1 GHz. This frequency coincides with common operating frequencies for various wireless communication applications and means that e.g. HR-SOI relaxes at high operating frequencies, showing a capacitive behavior. This may be good concerning a possible high R_P (low losses) but would be of disadvantage in terms of crosstalk especially at higher frequencies. This is observed in Figure 23 where the HR-SOI crosstalk transitions to being frequency dependent at ~1 GHz. MR-SOI and LR-SOI exhibits a relaxation frequency much higher in the frequency spectrum and was not therefore observed in the measurements.

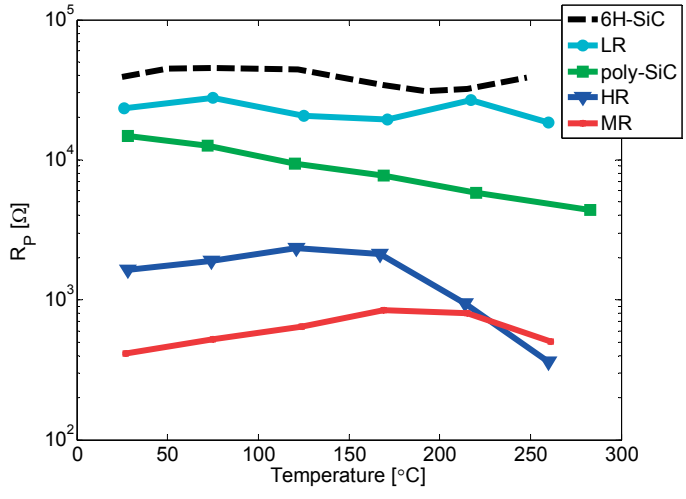

Figure 24. Equivalent R_P versus temperature for different substrates at 2 GHz. [**Paper VI**]

Furthermore, the substrates were investigated regarding RF losses at higher temperatures up to ~280 ºC. With increased temperature there was no affect on crosstalk in the poly-SiC substrate while a slight decrease was seen

in R_P with temperature, see Figure 24, where R_P is plotted versus temperature at 2 GHz. The LR silicon substrate showed no temperature effect due to the high doping concentration. The MR and HR substrate exhibits an increased resistivity as the temperature increases, caused by increased carrier-lattice scattering [59], i.e. decreased mobility. As the temperature increases, thermally generated carriers will contribute to the free carrier concentration and will be comparable to the ionized doping concentration. This causes the resistivity to decrease again even if the mobility reduces further. This effect is most noticeable for the HR silicon due to its lower doping concentration.

4. Summary

To achieve state-of-the-art wireless RF circuits, integration is important to save on cost and size while demands are high on operating frequencies and performance. As the CMOS technology is continuously downscaled combined with low supply voltages to reduce consumed power, it can be challenging for the integrated RF PA to deliver high operating voltages and maintain high reliability.

In **Paper I**, an integrated LDMOS transistor is presented, that utilizes the process steps from a 65 nm CMOS process to achieve high breakdown voltage and low R_{ON}. High output power is demonstrated both at WLAN and X-band frequencies in **Paper I-II**. For example is outstanding performance with 32.8 dBm output power shown for an integrated WLAN-PA design with this LDMOS transistor and the feasibility of the concept X-band is demonstrated for the first time. The developed LDMOS could also have an advantage as a driver for GaN switch mode PA, where high output power is required but linearity is not as demanding. High compression and operating close to breakdown make oxide integrity and transistor reliability important, especially with the thin oxide used in a 65 nm CMOS process. **Paper III** investigates how different stress mechanisms can be present and cause different parameters to drift depending on the bias conditions.

As operation frequencies increase, losses in the substrate and crosstalk are more pronounced problems. To overcome these problems, SOI is more and more accepted by the CMOS industry since it can provide high performance, lower RF losses and improved integration. Even if SOI provides high frequency benefits, the buried oxide can be a drawback. Self-heating may not be a problem for low voltage SOI devices but when high power devices are concerned, self-heating can be substantial.

Paper IV presents the design and fabrication of a novel 150 mm Si-on-poly-SiC hybrid substrate. The hybrid substrate utilizes the high thermal conductivity of poly-SiC to reduce self-heating and its semi-insulating properties to enhance RF performance. This is the first time this type of hybrid substrate is fabricated in 150 mm, where the large size is important for possible processing at foundries. Furthermore, successful LDMOS transistors were fabricated on the hybrid substrate in **Paper V**. The measurements demonstrated excellent electrical properties and that there is no degradation in terms of electrical performance going from SOI to the Si-on-poly-SiC hybrid substrate. Substantial improvement of 2.5 times in thermal conductivity was

also demonstrated with the new hybrid substrate compared to a SOI reference. **Paper VI** presents how the choice of substrate greatly affects RF performance. The hybrid substrate with the thick poly-SiC underneath the device layer has benefits in a high equivalent parallel resistance which translates to low substrate losses. In a transistor this implies better efficiency and output power. Compared to common substrates such as bulk Si and SOI, the equivalent parallel resistance was many orders higher.

The properties of the Si-on-poly-SiC substrate show benefits in reduced high frequency losses which is an evident advantage for e.g. RF-transistors. Advantages could also be seen for CMOS in the future, since the hybrid substrate provides a reduced thermal resistance which contributes with higher tolerance of the amount of dissipated power. The hybrid substrate is also cost-effective since it can be fabricated in large wafer sizes and due to the availability of poly-SiC. Furthermore, the hybrid substrate opens up for heterogeneous integration ("More than Moore") where e.g. GaN can be grown in etched silicon trenches in the device layer. This provides the opportunity to integrate high power devices with low voltage CMOS and new functionality in circuit architecture, which has not been possible before.

5. Svensk sammanfattning

I dagens moderna samhälle förlitar vi oss alltmer på trådlös kommunikation. Man vill kunna surfa var som helst på sin mobiltelefon eller laptop och de ska vara lätta och billiga. Basstationer måste leverera effekt för det allt större utnyttjandet av trådlösa enheter och hantera stora mängder data. För att kunna tillgodose utvecklingen behöver komponenter arbeta på högre frekvenser för att leverera mer data under kortare tid och prestanda ska helst förbättras utan att det blir dyrare för industrin att tillverka.

Halvledarindustrin vill ha billiga lösningar som kan utnyttjas i stor skala för att tillverka sin elektronik. Idag är CMOS-teknologin det vanligaste valet hos fabriker eftersom att den är väl etablerad och har möjliggjort det förhållandevis lätt att skala ner komponenter. CMOS, med MOS-transistorer som byggstenar, används för det mesta för logiska kretsar så som mikroprocessorer och minnen men också till digitala och analoga förstärkare. För att höja prestandan forskas det fram nya lösningar, andra material ersätter kisel och nya substrat introduceras. Men så länge CMOS kan leverera det som efterfrågas kommer det att fortsätta vara valet av teknologi.

I sökandet av högre effekt och när högre frekvenser började tas i bruk introducerades LDMOS-transistorn på 90-talet. Eftersom att LDMOS-transistorn kan arbeta vid höga frekvenser och leverera hög effekt med hög genombrotts-spänning blev den ett självklart val för basstationer och radarsystem. Den är en efterföljare till MOS-transistorn som är byggstenen i CMOS och LDMOS har följaktligen fördelen att tillverkas med samma processer som i CMOS men tåla högre spänningar. Detta gör integration av högeffektstransistorer i CMOS ett hett ämne som skulle bidra med många fördelar. Utmaningen i detta är prestandan i förstärkare för den applikation man vill använda. Hög effekt, hög verkningsgrad och linjäritet är bara några av de krav som ställs. I dagens mest förekommande processer finns t.ex. inte integrerade högeffektstransistorer utan dessa tillverkas i separata egna processer. För att integrationen ska vara attraktiv för industrin ska helst inte nya processteg introduceras i tillverkningen för att undvika högre kostnad och ändringar i existerande komponentparametrar.

I **Papper I** demonstreras en LDMOS integrerad i en 65 nm CMOS process utan ytterligare process-steg designad för WLAN (2.45-5.8 GHz) effektförstärkare med god prestanda. I **Papper II** demonstreras för första gången denna typ av LDMOS i X-band vid 8 GHz vilket används för radar och kommunikationssystem. Där visade den sig också leverera god prestan-

da med över 0.3 W/mm uteffekt. Den här transistorn kan arbeta nära genombrott och med hög kompression vilket innebär att riskerna är stora för läckströmmar i oxiden pga. stressrelaterade effekter som påverkar komponentens tillförlitlighet med tiden. Detta undersöks i **Papper III** där läckströmmen kopplas till spänning och var i LDMOS transistorn stresseffekterna äger rum.

Med ökad integration skulle det innebära att digitala och analoga kretsar samsas på ett chip, och speciellt i detta fall måste problem som crosstalk (överhörning) vara kontrollerat. Man kan isolera komponenter från varandra med diken gjorda av kiseldioxid men signaler kan fortfarande propagera i resten av substratet. För att få bukt med crosstalk och andra substratförluster där högfrekventa signaler försvinner i substratet kan man designa om substratet. SOI är ett exempel där ett isolerande skikt av kiseldioxid finns under komponentlagret och därmed bidrar med den extra isolationen underifrån. SOI har också fördelen att visa hög prestanda för väldigt nerskalade CMOS-komponenter för snabba låg-spännings-tillämpningar. Nackdelen med SOI är den låga värmeledningsförmågan hos kiseldioxiden som kan skapa självuppvärmning av komponenterna. Genom att byta ut detta material mot ett material med högre värmeledningsförmåga som samtidigt är praktiskt genomförbart skulle högeffektsprestanda förbättras.

Med målet att nå hög prestanda för högeffekts- och högfrekvenskomponenter beskriver den här avhandlingen även framtagandet av ett till ändamålet anpassat hybridsubstrat. Det bygger på att genom sammanfoga material ta fram ett substrat i kiselkarbid med ett komponentlager i kisel. Kiselkarbiden har högre värmeledningsförmåga än kisel vilket förbättrar högeffektsegenskaperna genom att utvecklad värme leds bort från komponenten. Kiselkarbiden har också materialegenskaper som lämpar sig för högfrekvensbruk då förluster av signaler i substratet minskas. Genom hybridsubstratet tas fördelar från både kisel och kiselkarbid tillvara. För första gången tillverkas ett substrat av denna typ i 150 mm diameter, för att påvisa möjligheten av storskalig tillverkning. **Papper IV** beskriver design och tillverkning samt utvärdering av hybridsubstratet med lyckade resultat. Även för första gången tillverkas och demonstreras LDMOS-transistorer på detta substrat i **Papper V.** Prestandan jämfördes med identiska transistorer på SOI och liknande eller bättre resultat uppnåddes. Eftersom att hybridsubstratet är ett outforskat material så utvärderas hybridsubstratets högfrekvensegenskaper i **Papper VI** och jämförs med olika typer av SOI.

Slutligen så ges möjligheten till heterogen integration med hybridsubstratet. Kislet kan etsas och exempelvis galliumnitrid kan gros i dess ställe för anpassade högeffektskomponenter. Då kan digitala kretsar och förstärkare i kisel samsas med transistorer i andra material på ett enda chip och dra fördel av hybridsubstratets egenskaper vid höga temperaturer och höga frekvenser.

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