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Fabrication and Characterization of Si-on-SiC Hybrid Substrates

LING-GUANG LI

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Abstract

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In this thesis, we are making a new approach to fabricate silicon on insulator (SOI). By replacing the buried silicon dioxide and the silicon handling wafer with silicon carbide through hydrophilic wafer bonding, we have achieved silicon on crystalline silicon carbide for the first time and silicon on polycrystalline silicon carbide substrates at 150 mm wafer size. The conditions for the wafer bonding are studied and the surface and bond interface are characterized. Stress free and interfacial defect free hybrid wafer bonding has been achieved.

The thermally unfavourable interfacial oxide that originates from the hydrophilic treatment has been removed through high temperature annealing, denoted as Ox-away. Based on the experimental observations, a model to explain the dynamics of this process has been proposed. Ox-away together with spheroidization are found to be the responsible theories for the behaviour. The activation energy for this process is estimated as 6.4 eV.

Wafer bonding of Si and polycrystalline SiC has been realised by an intermediate layer of amorphous Si. This layer recrystallizes to some extent during heat treatment.

Electronic and thermal testing structures have been fabricated on the 150 mm silicon on polycrystalline silicon carbide hybrid substrate and on the SOI reference substrate. It is shown that our hybrid substrates have similar or improved electrical performance and 2.5 times better thermal conductivity than their SOI counterpart. 2D simulations together with the experimental measurements have been carried out to extract the thermal conductivity of polycrystalline silicon carbide as $\kappa_{pSiC} = 2.7\ WK^{-1}cm^{-1}$.

The realised Si-on-SiC hybrid wafer has been shown to be thermally and electrically superior to conventional SOI and opens up for hybrid integration of silicon and wide band gap material as SiC and GaN.

Keywords: hydrophilic wafer bonding, silicon on silicon carbide, hybrid substrate, oxygen out-diffusion

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To Emelie with whom this thesis has been pushed one year later; the one without name yet in my belly who experiences the writing process together with me and Alexander

List of Papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I Li L. –G., Vallin Ö., Lu J. Smith U. Norström H. Olsson J. (2008) Oxide-Free Silicon to Silicon Carbide Heterobond. *ECS Transactions,* 16(8):377-383

II Li L. –G., Vallin Ö., Lu J. Smith U. Norström H. Olsson J. (2010) Oxygen out-diffusion from buried layers in SOI and SiC-SOI. *Sold-State Electronics,* 54:153-157

III Lotfi S., Li L. –G., Vallin Ö., Norström H. Olsson J. (2012) Fabrication and Characterization of 150-mm Silicon-on-Polycrystalline Silicon Carbide Substrates. *Journal of Electronic Materials,* 41(2):480-487

IV Li L. –G., Rubino S., Vallin Ö., Olsson J. Dynamics of SiO_2 Buried Layer Removal from $Si/SiO_2/Si$ and $Si/SiO_2/SiC$ Bonded Substrates by Annealing in Ar. Accepted by *Journal of Electronic Materials*

V Li L. –G., Lotfi S., Vallin Ö., Olsson J. Thermal characterization of polycrystalline SiC. Submitted to *Journal of Electronic Materials*

Description of my contribution

I. Planning of paper subject and content with essential input from coworkers in terms of theoretic brain-storming discussion. Majority of experiments and oxidizing experiment and AFM measurements together with Vallin Ö. Strain calculation done together with Smith U. All of the writing.

II. Planning of paper subject and content. Oxygen out-diffusion experiments together with Vallin Ö and TEM experiments by Lu J. All of the writing.

III. Characterization of Raman and XRD together with Vallin Ö. AFM experiments. Participation in the component fabrication and the explanation of the material analysis.

IV. Planning of the paper subject and content. Most of the FIB preparation and the TEM experiments except in the beginning learned with Rubino S. EELs experiments by Rubino S. Simulation of the ellipsometry. Writing and figure modification together with Vallin Ö.

V. Planning of paper subject and content and evaluation. Fabrication together with Lotfi S. Simulation by Olsson J.

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Contents

Abbreviations

CMOS	complementary metal oxide semiconductor
SOI	silicon-on-insulator
BOX	buried oxide
PMOS	p-type metal oxide semiconductor
NMOS	n-type metal oxide semiconductor
RF	radio frequency
pSiC	polycrystalline silicon carbide
Ox-away	oxygen out-diffusion
IR	infra-red
O_i	oxygen interstitials
TCR	temperature coefficient of resistance
CZ	Czochralski
FZ	float zone
rms	root-mean-square roughness
CMP	chemical mechanical polishing
AFM	atomic force microscopy
TEM	transmission electron microscopy
XPS	X-ray photoelectron microscopy
FIB	focused ion beam
XRD	X-ray diffraction
XRR	X-ray reflection
EELs	electron energy loss spectroscopy
SIMS	secondary ion mass spectroscopy
Thermistor	thermal resistor
CVP	chemical vapor deposition

1. Introduction

Electronic circuits and components, for computers, communication, medical applications, automotives, home entertainment etc. play an important role in our modern life. The desire of faster, cheaper, less energy consuming, more reliable and multifunction products is driving the rapid development. Of all these circuits and components, both for digital and analog, most are based on bulk Si CMOS technology. Though the bulk Si technology dominates in the electronic world, there do exists alternative technologies, which can provide better performance for some applications: the silicon-on-insulator (SOI) technology may provide higher frequency and lower power consumption, and overall better performance.

The SOI technology is very similar to the bulk-Si technology. Basically the main difference is that the bulk-Si substrate is replaced by an SOI substrate. The most common SOI substrate, or wafer, consists of a stack of Si-SiO_2-Si that forms the substrate, i.e. a thin layer of silicon is isolated from the thick silicon substrate by forming or inserting a buried SiO_2 layer (BOX) in-between. To differ from the conventional bulk Si substrates-based semiconductors, the electrical insulation layer in SOI may reduce the parasitic capacitance to the substrate, and also within the device itself, remarkably. Take the PMOS as an example (NMOS is comparable), with its cross-section on both bulk Si and SOI wafers illustrated in Figure 1. The parasitic capacitance between the source/drain and the Si substrate are reduced in the SOI technology. If the BOX is made thicker the coupling to the substrate decreases and can ultimately be almost eliminated. This change in structure allows SOI-based circuits to operate at higher speed and with lower leakage currents, i.e. lower standby power consumption. Alternatively SOI can operate at a lower supply voltage, which reduces the overall chip/system power consumption. For instance, IBM has demonstrated that comparing with the bulk CMOS technology, the SOI technology can enhance 30% performance and reduce 40% power consumption [1].

Moreover, as can been seen in Figure 1, unlike the bulk Si technology which has to isolate devices (PMOS in this case) with SiO_2 trenches, isolation becomes easier using the SOI technology. This enables a denser design and more reliable circuits with SOI technology. Thus SOI technology is an attractive alternative for high-performance-driven products to replace the bulk Si technology. However, there is a main disadvantage to prevent the SOI technology to replace the bulk technology: the higher cost of SOI.

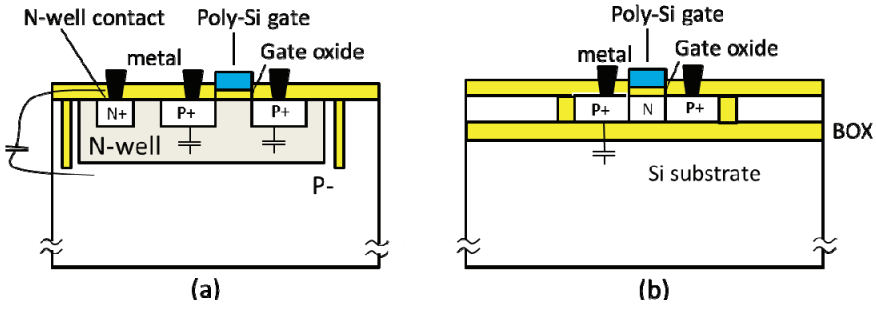


Figure 1 Illustration of cross-section of a PMOS on (a) bulk Si and (b) SOI substrate

Since the SOI technique became mature at 1990s, a hot debate has been on-going about if the SOI technique would replace the bulk Si technique and if so when would it happen. The SOI supporters argued that when the CMOS dimension shrinks, instead of going to 3D Tri-gate structure, SOI technique can achieve the same performance using the traditional planar structure [2].

As the dimension continues shrinking, the cost gap between the bulk technology and the SOI technology decreases. Added in the process cost, the 28 nm node technology based on the SOI technology costs roughly 7% higher than the bulk Si technology. In a prediction by the International Business Strategies at 2012, when the dimension shrinks to 20 nm node, the SOI technology will be economically preferable with 8%-18% cheaper than the bulk Si technology [3]. Recently, Intel and IBM reported the realization of the 22 nm node technology on 3-D Tri-gate bulk Si and SOI respectively [2]. Yet the costs are still unknown. It seems that bulk Si technique can always find a way (so far) to overcome the obstacles, and consequently the SOI era to replace the bulk Si technique will may never come.

Even though the SOI technique is not widely used in the main stream electronics, it has a market. The price non-sensitive products like XBOX and PlayStation are based on SOI technique. Another application of SOI technology is the graphic cards and microprocessors of AMD in use of PC, etc. [4]. There are also many other niche products that benefit from the advantage of the SOI technology, e.g. in automotive electronics [5].

There are two main methods to achieve economical and ready-to-use quality SOI wafers: Separation by IMplantation of OXygen (SIMOX) and wafer bonding. The former way is to create a buried SiO_2 layer through oxygen ion beam implantation followed by high temperature annealing during which a buried oxide layer is formed [6]. Of the other method, one prominent example is the *Smart-Cut* technology [7], in where a high dose of hydrogen or helium is implanted into a silicon wafer that subsequently is bonded to an oxidized wafer and finally split during an annealing step. *Smart-Cut* SOI wafers are today dominating, and can be obtained with almost arbitrary silicon thickness and buried oxide thickness.

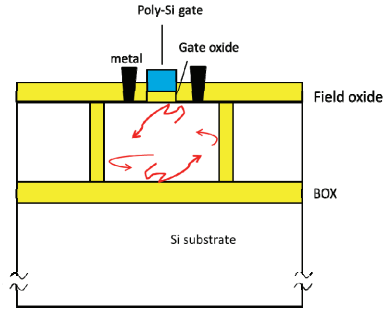


Figure 2 Illustration of the self-heating effect in SOI substrate-based PMOS transistor

In this study we use the *Smart-Cut* SOI wafers to transfer the thin device Si layers in our wafer bonding process, which will be described in detail later in the experimental part.

Providing its various advantages: compatible to bulk Si process, easy to grow, electrical insulating and so on, SiO_2 has an unavoidable drawback: its thermal conductivity is very low. The thermal conductivity of SiO_2 κ_{SiO2} is about two orders of magnitude less than that of the bulk Si with $\kappa_{Si} = 1.5$ $Wcm^{-1}K^{-1}$ [8, 9].This will cause very inefficient heat dissipation in SOI substrates where SiO_2 is forming the buried insulator. As can be seen in Figure 2, the device (PMOS in this case) is surrounded by SiO_2, and the only way for the heat to "escape" is through the metal contacts or through the inefficient substrate. Adding one μm of SiO_2 to the BOX is like adding 100 μm of silicon, thus increasing the overall thermal resistance. Actually in reality it is even worse, since the heat may spread in 3D in the silicon substrate, but not significantly so in a comparably thin BOX. Consequently, the poor thermal conductivity of SiO_2 will may result in self-heating effects of the device as illustrated in Figure 2.

As the temperature increases with the self-heating effect, the performance will decrease. One way to reduce this problem is through packaging at a system level, which is in use in productions, for instance the metal sinks and the cooling fan in the computer. Another way is by manipulating the SOI substrate itself, through replacing SiO_2 by better thermal conductive materials such as sapphire [10], diamond [11-13], Al_2O_3 [14] and AlN [15].

In this thesis, we are making a new approach by replacing the SiO_2 and the handling wafer by SiC. There are plenty of good reasons to replace SiO_2 with SiC. Firstly, SiC has much higher thermal conductivity of κ_{SiC} at 4.9 $Wcm^{-1}K^{-1}$ [16], which is three times higher than that of Si and 300 times higher than that of SiO_2. A Si-SiC hybrid wafer would solve the self-heating problem, and even offer better thermal performance than bulk-Si.

Secondly, SiC has SiO_2 as its native oxide and a Si-SiC hybrid wafer is compatible with the mainstream Si process. Also, undoped SiC is electrically semi-insulating and we can keep the benefits of SOI wafers as described

above. It will have similar performances as a high resistivity SOI substrate, where the silicon substrate has very high resistivity (>1-5 kΩcm) [17, 18], but without the thermal problems related to the BOX [19].

Thirdly, SiC is a wide band gap semiconductor, which is used in microwave applications [9]. The Si-SiC hybrid substrate would make it possible to develop Si devices and SiC devices on the same chip. A potential application would be radio frequency (RF) power transistors in mobiles, devices for harsh environment like high temperature electronics, and radiation-hardened electronics [20].

Last but not least, SiC crystal has comparable lattice parameters as GaN [21] chapters 1 and 5. Thus a hybrid Si/SiC/GaN hybrid substrate could integrate GaN devices including power low-noise microwave applications as well as light-emitting diodes with Si-based devices. The concept is illustrated in Figure 3.

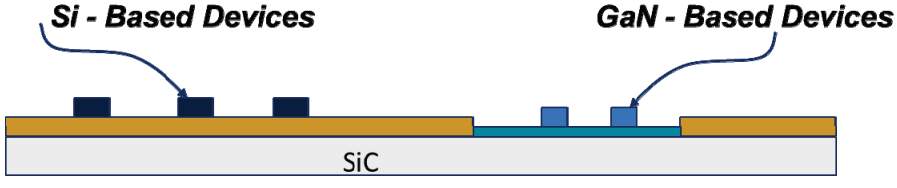


Figure 3 Illustration of the concept to integrate Si-, SiC- and GaN-based devices in one chip

The work in this thesis is therefore focused on the forming, and related studies, of a hybrid substrate consisting of silicon-on-silicon carbide. The main advantages are the better thermal properties and that SiC can be semi-insulating, thus enabling e.g. enhanced performance for silicon RF-power technologies.

Although crystalline SiC has many advantages as just described, it is a very expensive material and the size is limited to 4 inch wafers while the Si industry is on its 12 inch era. Instead of single-crystalline SiC, polycrystalline SiC (pSiC) wafers can be used. They are both much cheaper and available in larger scale wafer size. PicoGiga has fabricated “SopSiC” wafers in 3 inch and 4 inch sizes [22]. It includes a thick Si device layer, an oxide interfacial layer and pSiC semi-insulating layer. As mentioned above, the interfacial oxide layer would behave as a hinder for thermal dissipation in the high power devices.

As it is two different materials that should form the substrate, there are a few challenges of how to make them “stick” together. Will there be interface defects due to the difference of lattice parameters for Si and SiC? Will strain be generated during the thermal treatment and how significant is the thermal

mismatch owing to the different thermal expansion coefficients? Furthermore, how will fabricated devices perform on this new substrate material?

In this thesis, we will demonstrate an approach to achieve a Si-SiC hybrid substrate with minor stress and defect free interfaces. Furthermore, a method denoted Ox-away, to reduce or eliminate an interface oxide is studied in-depth. Finally, hybrid substrates developed and fabricated are used for manufacturing of different test structures to evaluate the electrical and thermal properties of the substrates.

2. Theory

2.1 Hydrophilic wafer bonding

Hydrophilic wafer bonding is a mature technique to fabricate SOI substrates [23]. There are three pre-requisites for a successful hydrophilic wafer bond: 1) two wafers have mirror-polished surfaces, 2) both wafers have clean hydrophilic surfaces and 3) both wafers have global flatness. With all these three pre-requisites fulfilled, when being placed face to face close to each other, the contact area of the two wafers will spread and adhere together at room temperature without any applying force.

It is proposed that there are up to three H_2O molecular layers on each hydrophilic wafer surface. When they are getting close enough, hydrogen bond will be formed as illustrated in Figure 4.

The H_2O molecules will fill in the micro voids. The critical local roughness should be no more than 0.5 nm for a successful wafer bonding [23].

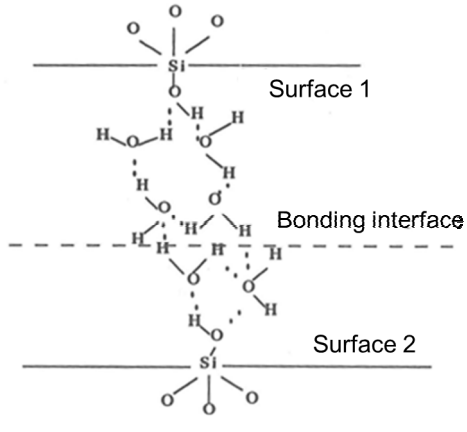


Figure 4 Postulated interface chemical structures of hydrophilic Si/Si pairs immediately after RT contacting at an isolated silanol site (cited from [23]Fig. 4.27 (b))

The initial room temperature bonding is a reversal process. Though the bond strength is strong enough to survive some characterization, for instance Infrared (IR) monitoring, bond anneal is necessary to achieve a stronger bond strength for the successive device fabrication and perhaps destructive

characterization. The bond strength increases with the anneal temperature up to 1000 °C [23].

There are two temperature intervals in this range concerning the bond quality: 1) from the room temperature to 300 °C, voids defect will appear during bond anneal. These voids originate from the H_2O collection during anneal. 2) Between 300 °C and 800 °C, the H_2O will dissolve into the SiO_2 or react with the neighboring Si to form SiO_2 and the bubble voids will disappear.

A void free bond interface is of course preferred. For the Si-Si wafer bonding, void formation has been intensively studied. Different methods have been tested to diminish or eliminate the voids. For example: surface plasma treatment prior to bonding at room temperature at the ambient air [24, 25], low-vacuum wafer bonding [26], thermally grown thin layers of oxide on the Si surface prior to bonding [27], changing the surface cleaning chemical solutions [28] and so on.

Understanding the origin of the voids would help us to analyze if and how effective the above mentioned methods are for the void elimination [29]: 1) The oxygen plasma would result in surface defects and these surface defects will collect the excess of the bonding reaction products at the interface (water, hydrogen) and form voids. Therefore the plasma exposure time should be optimized for a better bond interface with fewer voids. 2) Low vacuum will only postpone the annealing voids; however, it doesn't eliminate them. 3) A layer of oxide on the Si layer would absorb extra water and hydrogen and thus prevent void formation. The effectiveness depends greatly on the thickness and above to 500 nm would be thick enough for the bonding reaction byproducts to be absorbed [27]. 4) Warm nitric acid surface treatment prior to bonding is a good way to avoid contamination.

It is worth to mention that one should also consider the relationship between the bond strength and the void formation: with higher bond anneal temperature, the bond strength increases quickly to a high level; therefore water or chemicals may have no time to diffuse out laterally. They segregate and trapped in the interface and form voids. Thus a relatively longer anneal time at stepped increasing anneal temperature would help to release some kind of voids. Moreover, for the voids originate from the H_2O molecular collection, high temperature anneal would help the H_2O to diffuse into the SiO_2 or Si and thus minimize/eliminate the voids.

The void free Si-Si bond is quite easy to achieve, but it may be difficult to obtain void free Si-SiC bond. One reason is the solubility of the H_2O into SiC is very small and the SiC is much more difficult to be oxidized by the bubbles [30]. Therefore high temperature anneal may not help to minimize/eliminate voids for the Si-SiC bond. One solution was to deliberately introduce a thin oxide layer on the SiC surface prior to bond. This would solve part of the void formation but also resulted in an unwanted oxide at the bond interface.

2.2 Oxygen out-diffusion

The introduction of SiO_2 will enable the hydrophilic wafer bonding of Si to SiC. However, after wafer bonding, we would like to remove the thermally unfavorable SiO_2. By thermal anneal the as bonded Si-SiO_2-SiC wafer at inert gas (Ar gas in our study, it would work in H_2 too) at high temperatures (1100 °C, 1150 °C and 1200 °C), the sandwiched SiO_2 could diffuse through the top Si crystal and out to the inert gas. We denote this method to Oxygen out-diffusion (Ox-away).

This method originates from Sullivan et al. [31]. They bonded Si (0 0 1)/Si (1 1 0) wafer with a very thin SiO_2 interface. The Si (0 0 1) has higher electron mobility and Si (1 1 0) has higher hole mobility. They would like to achieve both high electron and hole mobility in the same chip. Afterwards, they removed the SiO_2 by Ox-away to achieve atom sharp Si-Si interface.

The Ox-away is illustrated as in Figure 5.

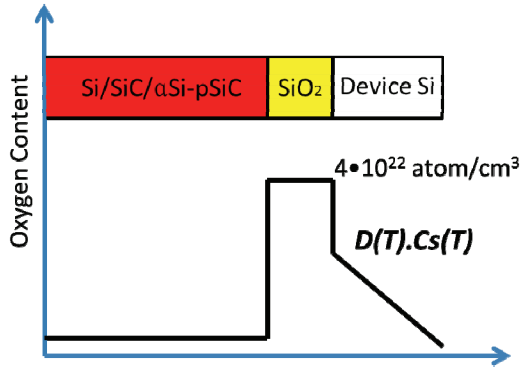


Figure 5 Illustration of Oxygen out-diffusion

The SiO_2 layer is oxygen pool. At the interface of SiO_2/Si, the oxygen concentration is the product of the solubility of oxygen C_s *(T)* in Si and the diffusion coefficient *D (T)* of oxygen in Si. C_s *(T)* and *D (T)* are temperature dependent. The oxygen flux F_{ox} *(T)* is the number of oxygen atoms that pass through the top Si layer in terms of area and time. It is a function of the diffusion coefficient of oxygen in Si, the solubility of oxygen in Si and top Si thickness (d_{si}) as in equation (1).

$$F_{ox}(T) = \frac{D(T) \cdot C_s(T) - 0}{d_{Si}} = \frac{1.183 \cdot 10^{22} \cdot \mathrm{e}^{-4.1\mathrm{eV}/kT}}{d_{Si}} (\mathrm{cm}^{-2}\mathrm{s}^{-1}) \quad (1)$$

$$D(T) = 0.13 \cdot \mathrm{e}^{-2.53\mathrm{eV}/kT} (\mathrm{cm}^2\mathrm{s}^{-1}) \quad (2)$$

$$C_s(T) = 9.1 \cdot 10^{22} (\mathrm{cm}^{-3}) \cdot \mathrm{e}^{-1.57\mathrm{eV}/kT} \quad (3)$$

D (T) was derived from Secondary Ion Mass Spectroscopy (SIMS) measurements of in-diffusion of oxygen during oxidation of float zone Si in a large range of temperature up to 1240 °C [32]. *Cs (T)* was derived from SIMS measurements of the in-diffusion oxygen in bulk float zone Si wafer in inert or oxidizing atmosphere at 900-1250 °C [33]. *k* is the Boltzmann constant.

From equation (1) we can see that the higher the temperature and the thinner the top Si layer is, the faster the Ox-away would be. Assuming the oxide diffuse out homogeneously layer by layer, the time needed t = Oxygen dose/ $F_{ox}(T)$. The oxygen dose is the product of the oxygen concentration in the oxide and the thickness of the oxide. For example, for the stoichiometry of the oxide as SiO_2, the oxygen concentration is $4 \cdot 10^{22}$ cm^{-3}.

The mechanism of the oxygen out-diffusion is another interesting physical phenomenon: in which form does oxygen diffuse out?

Mechanism of dopant diffusion in silicon has been studied for a long time and the interstitial theory was favored since 1989 [34-36]. Some groups adopted the interstitial theory in the Si/oxygen system, including Gösele et al. [37] and Devine et al. [38].

Gösele's group has bonded Si wafers with sandwiched oxide. They then annealed them at 1100 °C and 1150 °C [37]. A bulk diffusion model was built to explain the phenomenon of the growth and shrinkage of the interfacial oxide. They believed that the oxygen atoms diffused in or out of the interface in the form of interstitials (O_i). The driving force was the oxygen concentration difference and the oxygen solubility at such temperatures (1100 °C and 1150 °C). However, no information of the Si wafer thickness was mentioned in their report. Later on, Gösele's group conducted experiments concerning the Si/SiO_2 interface and they believed the formation of SiO during thermal anneal [39].

Devine's group[38] studied the polycrystalline Si/430 nm SiO_2/crystalline Si degradation process at 1200 °C /1275 °C under inert gas (Ar), and at 1320 °C under weakly oxidizing atmosphere (Ar/1% O_2). The interstitial theory was applied to explain the oxygen behavior in the Si/SiO_2 interface: the oxygen atoms break the Si-O bonds in the SiO_2 structure and diffuse into the Si

crystal space. There they bond with two broken Si atoms and it results in a non-linear Si-O-Si structure. Although the oxygen interstitial atoms don't occupy Si positions in the Si crystal, they are not free to move.
Note that the silicon dioxide is in contact with silicon layers. During the annealing process, it might react with silicon as in equation (4):

$$SiO_2 + Si \rightarrow 2SiO \qquad (4)$$

During the decomposition process of SiO_2, as described in equation 4, the neighboring Si atom may bond to an oxygen atom and form a SiO molecule. The Ox-away process consists of two steps: 1: decomposition of SiO_2 by the reaction in equation 4, and 2: volatile SiO diffuses out of the top Si crystal.

Many researchers have observed the decomposition of SiO_2 phenomenon while studying the inorganic chemistry reaction between Si and SiO_2, mostly in the powder form [40-45]. In [44] the Gibbs free energies of SiO formation from Si + SiO_2 are discussed. In [43], SiO_2 and polycrystalline Si were heat treated at 1415 °C− 1490 °C followed by quenching into cold water, to study the oxygen solubility in the molten silicon. They concluded that SiO exists at high temperature and that it converts to SiO_2 and Si during the cooling process. Eq. 4 moves to the right hand side at temperatures above 1200 °C [40]. In [45] literature about the vapor pressure of Si + SiO_2 mixture and SiO is summarized. According to [41, 44, 46], SiO exists at temperatures as low as 1000 °C.

Schnurre et al. summarized literature concerning the thermodynamics and phase stability in the Si – O system and made theoretical calculation and experimental studies [47], and the results show that between 227 and 1414 °C, the Si + SiO (amorphous) system is stable.

Gösele and colleges modeled the Si/SiO_2 interface at 1150, 1200 and 1250 °C to explain the Si diffusion into SiO_2 which they observed experimentally [39]. They believe the reaction of Eq.4 happens and the exchange of Si atom between the SiO molecules and the Si crystal contributes to the enhancement of the Si diffusion rate into SiO_2. The diffusion coefficient of SiO into SiO_2 is temperature dependent and at 1150 °C it is $\sim 2 \cdot 10^{-16}$ cm^2/s. If SiO is generated in the Si/SiO_2 interface can diffuse into SiO_2, it could also diffuse into Si as well.

Doremus [48] criticized the above process by considering the activation energy for the bond breaking and formation and the steric hindrance during the oxygen diffusion. He built a model to illustrate this feasibility [48]. In his model, the SiO molecules dissolve in the biggest space in Si, i.e. the (1 1 1) orientation. His model consists well with the earlier experimental observation by infrared spectra and dichroism.

2.3 Strain in the Si-SiC bond interface

Stress is an issue the Si-SiC bonding needs to consider. The thermal expansion coefficients α for Si and SiC are temperature dependent [49, 50].

$$\partial(\mathrm{Si}) = \left[3.75 \times \left(1 - \mathrm{e}^{-5.88\times10^{-3}\times(T-124)}\right) + 5.548\times10^{-4}\times T\right]\times10^{-6}$$

$$\partial(\mathrm{SiC}) = 3.09\times10^{-6} + 2.63\times10^{-9}\times(T-273.2) - 1.08\times10^{-12}\times(T-273.2)^2$$

When the bond pairs with SiO_2 interfacial layer is annealed at over 1000 °C, the SiO_2 behaves as lubrication layer. After Ox-away, the Si contacts directly with SiC and during the cooling process there might generate stress in the bond interface. By integrating the thermal expansion coefficients from 1250 °C to room temperature, we can get the planar strain εx and εy for the Si-SiC interface plane (x-y).

$$\varepsilon x = \varepsilon y = \int_{1523}^{300} [\partial(SiC) - \partial(Si)]dT = -1.8\times10^{-4}$$

The minus symbol indicates the Si layer is under the compressive stress. 1.8 x 10^{-4} is a very low level strain and it is below the yield stress and thus protected from brittle fracture. The integration of the difference in thermal expansion coefficient between SiC and Si, over the cool-down temperature range, is illustrated in Figure 4 in attached paper I.

2.4 Spheroidization theory

Reference [37] studied when two bulk Si wafers were bonded together with a thin layer of chemical oxide layer, this oxide layer would either grow thicker or decrease thinner with anneal at high temperature, depending on the oxygen content in the Si wafers and the anneal atmosphere: with high oxygen concentration (higher than the oxygen solubility in the Si under the annealing temperature) in the Si wafer and/or under oxidizing atmosphere, the SiO_2 layer will grow. Otherwise it will disintegrate and spherize.

With thin enough device Si layer above, as the SiO_2 thickness decreases with high temperature anneal under inert gas atmosphere, besides the Ox-away theory, spheroidization may occur. For example, when SiO_2 becomes less than 3 nm, the SiO_2 will not decrease evenly. There is an energy demanding for the SiO_2 to spherize to minimize the surface energy. The spheroidization of an oxide layer is illustrated in Figure 6 as cited from [37] Fig. 3a-c. When the oxide layer becomes thin enough (<3 nm), non-homogeneous Ox-away would occur. First is the disintegration. The oxides become dis-continuous "islands". Then these islands prefer to spherize to minimize the surface energy. This is the spheroidization. The disintegration is an energetic cost process and the spheroidization is an energetic save process. But the complete process of their combination costs energy: 3.5 eV is needed for 2 nm SiO_2 to spherize and 8 eV for 3 nm SiO_2 to spherize.

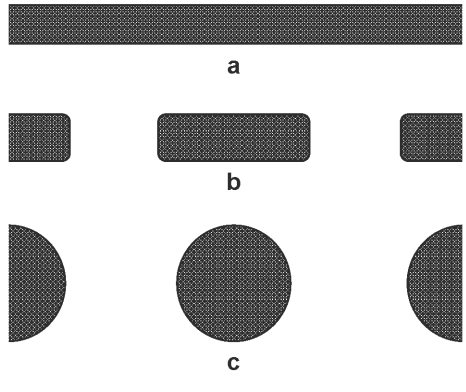


Figure 6 Schmetic diagrams of the spheroidization of an oxide layer: a starting oxide layer, b disintegration, and c spheroidization (cited from [37] Fig. 3a-c)

2.5 Thermal dissipation simulation and the experimental realization by thermistor concept

As discussed in the introduction part, one of the advantages to replace SiO_2 and Si handling wafer by SiC is SiC's good thermal conductivity. To characterize the thermal property and compare the difference between Si and SiC, thermal dissipation simulation has been done and thermistors are fabricated on thin SiO_2 (25 nm) on Si, pSiC and SiC substrates to compare with the simulation results.

There are two dimensional simulation (2D) and three dimensional (3D) simulations to examine the thermal dissipation property of substrates. For the 2D simulation, a line heat source is generated on the device and it dissipates through the cross section area. For the 3D simulation, a point heat source is generated on the device and it dissipates in all directions. In Figure 7, 2D simulation of SOI with 1 µm BOX and Si-on-SiC substrates are shown to demonstrate this concept. It can be seen that for the SOI substrate, the device on SOI becomes much warmer than that on SiC. The heat dissipates mainly laterally on the SOI substrate and the on the Si-on-SiC substrate, the heat dissipates both laterally and vertically.

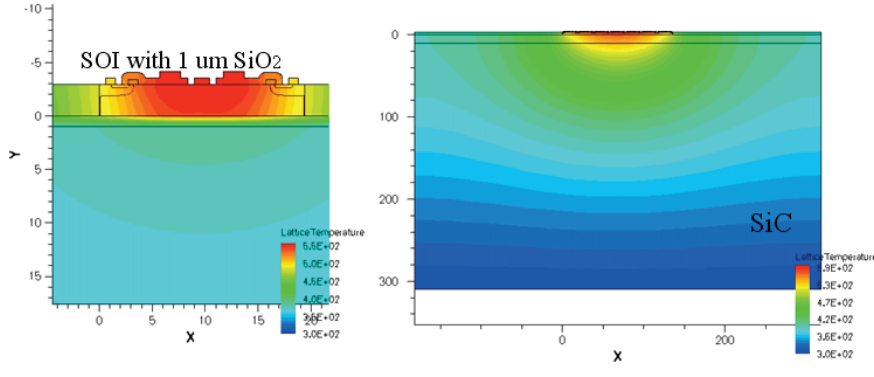


Figure 7 2D simulation of SOI with 1 um BOX and Si-on-SiC substrates

Thermistors can be fabricated on the substrates to verify the thermal properties. Thermistor is the short form of thermal resistor, which is a resistor with high thermal sensitivity. The resistance varies with the temperature. The simplest thermistor has the first order approximation which means that the resistance depends on the temperature linearly as in Eq. 8.

$$\Delta R = K \cdot \Delta T \tag{8}$$

K/R_0 is the temperature coefficient of resistance (TCR).

By calibrating the thermistor under controlled temperature, the K value can be extracted. Then the thermistor may be placed under the unknown temperature to measure the resistance. The temperature can be calculated out.

3. Experimental

3.1 Hydrophilic wafer bonding

In this thesis, we have bonded Si-SiO_2-Si, Si-SiO_2-SiC and Si-αSi-pSiC by hydrophilic wafer bonding. The main steps of the bond process are illustrated in Figure 8. All the bonding experiments are carried out in a class 100 clean room.

The SOI wafers were purchased from Soitec™. They were made using a smart cut technique. The reason we bond SOI is that we need thin Si layer for the later Ox-away process. For the resulting bond pair (a) in Figure 8, even though we did not introduce the SiO_2 before bonding, after bond anneal at 1000 °C in N_2, a very thin layer of SiO_2 will appear between the device Si layer and the substrate Si layer. It originates from the H_2O from the Si hydrophilic surfaces. We denote this SiO_2 as chemical SiO_2.

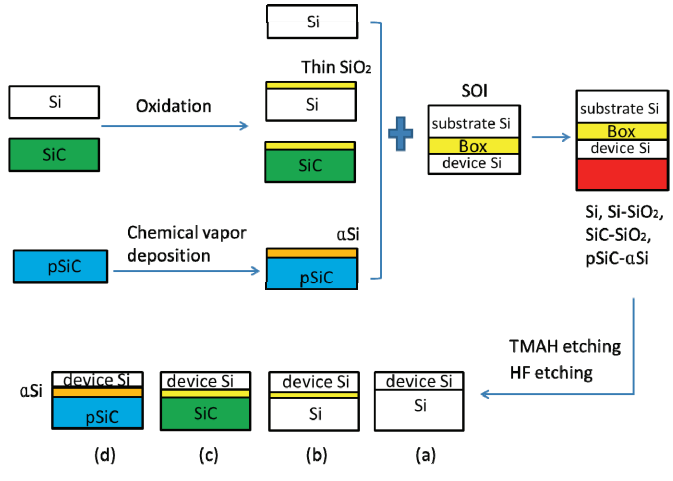


Figure 8 Main steps of the hydrophilic wafer bonding process flow to achieve Si-Si, thin BOX SOI, Si-SiO_2-SiC and Si-αSi-pSiC substrates

To differ from (a) in Figure 8, (b) has a thermally grown SiO_2 layer between the device Si layer and the substrate Si layer. The thicknesses of the thermal SiO_2 layers are ~10 nm and ~20 nm. The substrate is float zone (FZ) Si since it contains much less oxygen than Czochralski Si (~10^{18} cm^{-3}). The oxygen content of FZ Si is less than $2.5 \cdot 10^{16}$ cm^{-3}. This is important for the Ox-away process that demands negligible substrate oxygen content.

To achieve Si-SiO_2-SiC bond pair, (c) in Figure 8, 2-inch Si faced 6H-SiC wafer is used.

To achieve the Si-αSi-pSiC bond pairs, 6 inch pSiC was used.

The resulted bond pairs are listed in Table 1.

Samples	Intermediate oxide thickness (nm)	Oxide type
Soitec SOI	410	Chemical oxide
Device Si on Si	2.3-2.6	Chemical oxide
Si-SiO_2-Si	19.3	Thermal oxide
Si-SiO_2-SiC	7, 10.8, 19.6	Thermal oxide
Si-αSi-pSiC	2, between Si-αSi	Chemical oxide

Table 1 Detail of the bonding results

3.2 Oxygen out-diffusion

Oxygen out-diffusion (Ox-away) has been studied based on Device Si on Si, Si-SiO_2-Si and Si-SiO_2-SiC wafers. The Ox-away experiments are carried out in a Koyo Thermo Systems' vertical furnace. The highest temperature is limited to 1300 °C. In this thesis, samples have been annealed at 1100 °C, 1150 °C, 1200 °C and 1250 °C for a series of time setting to study the dynamics of the Ox-away process. The samples are diced to 1 cm x 1 cm pieces and uploaded under the N_2 flow. Then wait under N_2 flow for the temperature to be elevated to the annealing temperature. During the Ox-away the sample are under the Ar flow. After Ox-away the samples are cooled down to the standby temperature (400 °C) and downloaded in N_2. The purities of N_2 and Ar are 99.998% and 99.9997 % respectively.

The device Si layers transferred from Soitec SOI have a thickness of ~350 nm.

The temperature and the time for Ox-away are listed in Table 2.

Sample No.	Related to table 1	Anneal temperature (°C)	Anneal time (min)
Si-1	Device Si on Si	1100	203
Si-2		1150	30
Si-3			60
Si-4			90
Si-5			120
Si-6			600
Si-7		1200	20
Si-8	Si-SiO_2-Si	1250	150
Si-9	Soitec SOI	1250	150

Table 2 List of the oxygen out-diffusion condition for device Si on Si and Si-SiO_2-Si

Sample No.	Related to table 1	Anneal temperature (°C)	Anneal time (min)
SiC-1	Si-SiO_2-SiC with 7 nm oxide	1150	120
SiC-2	Si-SiO_2-SiC with 10.8 nm oxide	1250	150
SiC-3	Si-SiO_2-SiC with 19.6 nm oxide	1250	150

Table 3 List of the oxygen out-diffusion condition for Si-SiO_2-SiC

We have more Ox-away samples for device Si on Si and Si-SiO_2-Si than Si-SiO_2-SiC because it is much easier for sample preparation for the analysis.

3.3 Material analysis methods and sample preparation

Several analysis equipments have been used for the bonding and the Ox-away results, as summarized in Figure 9.

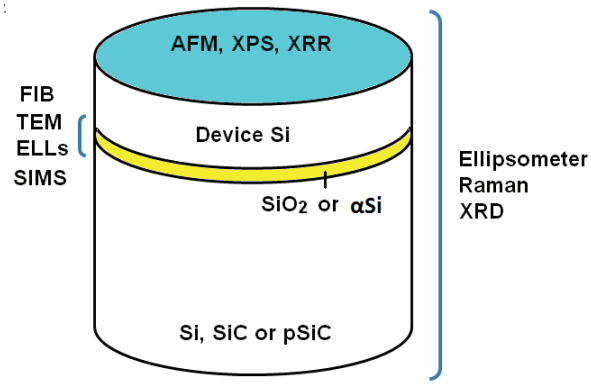


Figure 9 Summary of the analysis methods and preparation tools used

A PSIA XE150 Atomic force microscopy (AFM) is used to characterize the surface roughness of the wafer. Non-contact mode was used. The AFM measurement of the wafer surfaces tells us if the wafer has smooth enough surface for bonding. It also provides information of the roughness of the surfaces of the bond stacks surface before and after Ox-away.

A Quantum 2000 PHI X-ray photoelectron spectroscopy (XPS) is applied to check the element and the stoichiometry of the surfaces of the bond pairs after Ox-away. To compare the difference before and after Ox-away, a pure CZ Si wafer dipped into HF solution prior to measurement was measured as the reference.

X-ray reflection (XRR) was used to find out the composition of the surface after Ox-away by modeling the density of the very thin surface layer. The incidence angle was chosen to be 0.5°.

Raman spectroscopy and X-ray diffraction were used to analyze if there is stress in the bonding interface by comparing the Raman and X-ray shift with pure Si reference wafer.

A FEI F30 Tecnai TEM and the attached EELs were used to analyze the cross-section of the bond interfaces, before and after Ox-away.

Two methods were used to prepare cross-section TEM samples: Focused ion beam (FIB) and mechanical method.

Before FIB preparation, thin layers of aluminium (Al) were sputtered on the device Si surfaces. During the FIB preparation, two additional Platinum (Pt) cap layers were deposited before milling, by using electron beam and ion beam induced deposition. The Pt deposition has a dimension of 25 μm x 5 μm and a total thickness of 1 μm. During the thinning process, the Ga+ ion

voltage was fixed to 30 keV. The samples were thinned to ~3.5 μm under a current of 1000 pA, followed by a continuing thinning process to ~2 μm under 300 pA and to ~1 μm under 100 pA. The final thinning step was under 10-50 pA and the final thickness of the TEM specimens were 50-100 nm. It is very important to decrease the ion current to lower than 50 pA in order to minimize the thickness of the surface amorphous layer that is formed on the lamella surface due to ion beam damage. All the samples except for Si-7 were prepared by the FIB method.

Si-7 was instead prepared by the mechanical method, where dimple grinding and ion milling devices were utilized. Since the bonding interface is of the most importance, two small pieces of the sample were clamped into a Titanium-ring face to face with the help of the epoxy glue. Then it was polished coarsely from both sides to around 80 μm by SiC paper. A Gatan Dimple Grinder model 656 was utilized to thin the specimen down to 5 − 30 μm. The specimen was finally thinned by a Gatan Precision Ion Polishing System (PIPS™) model 691 with 3 − 5 keV Ar ions. The final specimen had a small hole in the middle to guarantee that the thinnest part was electron transparent. The final thinning parameters were 3 keV and ~12 μA.

SIMS equipped with a Cameca ims 4f micro-analyser was used to investigate the oxygen and the silicon concentration in the bond interfaces before and after Ox-away. The primary beam is Cs+.

An UVISEL ER HORIBA ellipsometer was used for the measurements of the interfacial oxide thickness to compensate the TEM results. The measurements are performed for a spectrum ranging from 800 nm to 2100 nm of wavelength at 70° incident angle.

3.4 Components fabrication on Si-αSi-pSiC hybrid substrates

Various electronic devices and test structures including diodes, transistors and finger thermal structures are fabricated on the SOI reference substrates and the Si-pSiC hybrid substrates using the standard MOS processing. The finger thermal structures are in the same dimension as the TiN thermistors, which will be described in details next part. The difference is that here the thermistors are polycrystalline Si and they are based on multi-layer substrates: SOI and Si-αSi-pSiC substrates. More details of the components dimension etc. can refer to the description of attached paper III.

3.5 Thermistors for the thermal characterization

Si wafers were thermally grown with a 25 nm SiO_2 layer for electrical passivation. Since the 2 inch 6H-SiC and the 4 inch poly-SiC substrate are electrically semi-isolating, the TiN was deposited directly onto the substrate, thus no intentional interface layer exists. The Si, pSiC and SiC wafers were 520 µm, 538 µm and 354 µm.

TiN was sputtered by a magnetron sputter under the pressure of $2 \cdot 10^{-3}$ Torr, the power was 1000 W and the frequency was 250 MHz. The flow of N_2 and Ar were 45 and 20 sccm respectively for 60 s to give a 30 nm thick TiN. The sheet resistance was measured by a four point probe as 20 Ohm/sq. to make optimum use of the current/voltage range of the parameter analyzer in order to get the highest possible power dissipated in the resistors.

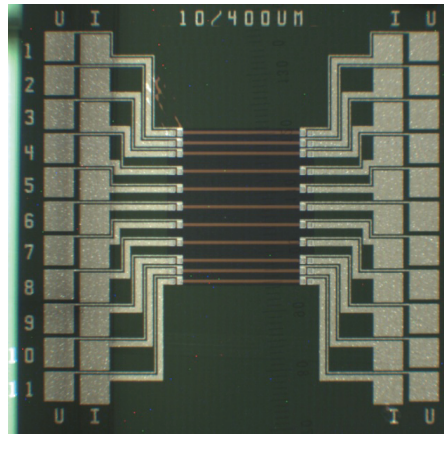


Figure 10 Top view of the finger structure of the thermistors

The patterning of the TiN thermistors was realized by lithography and plasma etching. 100 µm x 100 µm aluminium (Al) contact pads were fabricated by sputtering and plasma etching for the measurement later. The top view of the resulting finger structures are shown in Figure 10.

The backsides of the wafers were deposited with a thin layer of Al for a good thermal transmission. The TiN thermistor behaves as heating source as well. Before measuring the self-heating effect in TiN thermistor on Si and SiC wafers, we calibrate the temperature − resistance curve of TiN thermistors. Terminals 1 to 4 were defined as in Figure 11. Terminal 2 was grounded and terminal 1 was biased with ramped voltage of 0 − 1 V. Such a low voltage was chosen to avoid the self-heating effect for the calibration. The voltage drops from terminal 3 to terminal 4 were measured and defined as ΔV. The current I_1 in terminal 1 were measured and the resistance was given

by $R = \Delta V/I_1$. By measuring ΔV and I_1 under controlled temperatures (25 °C − 50 °C for SiC wafer and 25 °C − 75 °C for Si wafer with 5 °C as an interval) on a hot chuck, the calibrated temperature vs. power density curve can be plotted.

After calibration, the metal hot chuck was removed and terminal 1 was biased with a ramped voltage of 0 − 40 v, as illustrated in Figure 11. ΔV and I_1 were measured and the power density (P/A) was calculated. $P = \Delta V \times I_1$ and A is the area of the TiN from terminal 3 to 4. Then the temperature against power density curve can be obtained.

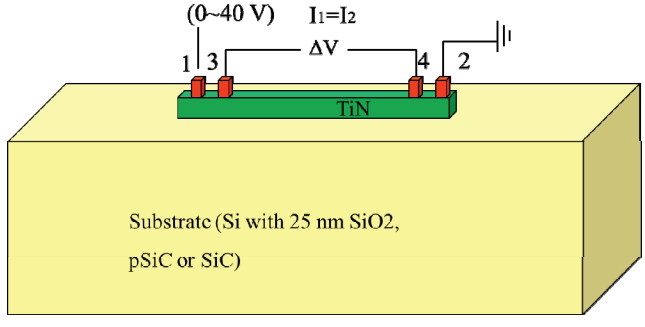


Figure 11 Illustration of one of the thermistors and the biasing illustration

4. Results and discussions

4.1 Si-Si bond

The surface roughness was analyzed by AFM. For Si-Si bond, the FZ Si surface, the oxidized FZ Si surface and to be transferred SOI device Si surfaces have a very smooth surface, in the dimension of root-mean-square (rms) roughness of 0.05 nm, which is well under the critical roughness condition for bonding.

After room temperature bonding and after bond anneal, the IR camera monitors the bond quality of the substrates. Figure 12 shows that after bond anneal for the Si-Si bond, the majority area is void free. The few dark areas on the edge are impurity induced non-bonded areas.

The IR images, complemented with optical microscopy, showed no visible cracks.

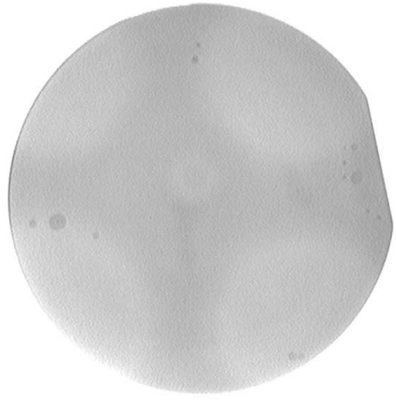


Figure 12 Infrared image of substrate of Si-Si bonding (device Si on Si in Table 1 after bond anneal

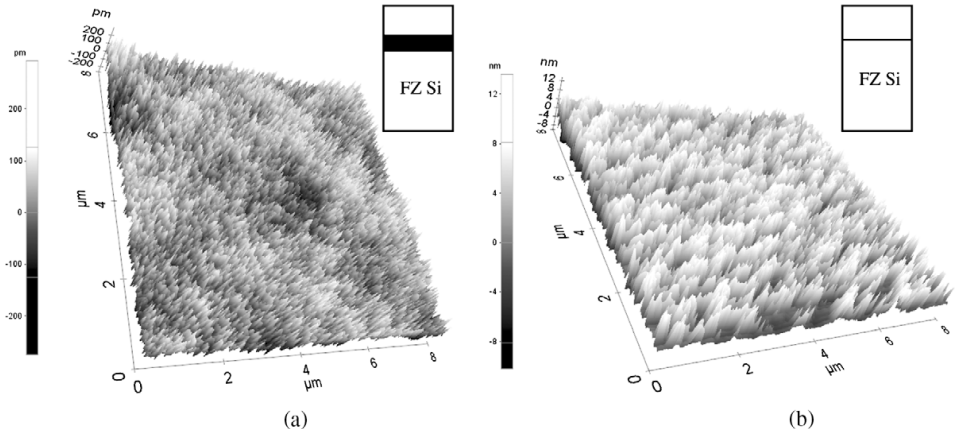


Figure 13 3D AFM images of the device Si surfaces from the Si-SiO_2-Si substrate in table 1, (a) before Ox-away and (b) after Ox-away. Note the roughness scale bar differences, in (a) with a unit of pm and (b) nm

The device Si surface roughness was measured before and after Ox-away, as shown in Figure 13. Before Ox-away the RMS roughness was 0.06 nm and after Ox-away 4.13 nm. We have studied the Ox-away anneal influence on the blank CZ Si wafer and the as-received SOI wafer. They show the same effect: 1250 °C 2.5 h anneal in Ar gas results the surface roughness. Note that both CZ and the SOI substrate have high oxygen content.

One possible explanation behind the surface roughening phenomenon is the erosion effect of the oxygen out-diffusion: when the oxygen diffuses out the device Si surface, it oxidizes the surface before it leave the surface. In literature, it has been observed that the small amount of oxygen in the inert gas would result in the surface roughening [51]. In our case, there is no oxidizing gas in the anneal gas; however, the out-coming oxygen would behave as the oxidizing resource. We have also observed that there appears a thin amorphous layer in the dimension of 20-40 nm on the surface after Ox-away, shown in Figure 14. This layer has been analysed by EELs in the silicon edges (90-120 eV and 1800-1850 eV) and oxygen K-edge (500-600 eV). No oxygen signal was detected. The X-ray photoelectron spectroscopy analysis has proved the EELs measurements. Hereby, we conclude that this amorphous layer is amorphous Si.

As explained in the theory part, SiO may be formed during the Ox-away process. One possible reason for the formation of the amorphous Si is the decomposition of the SiO to Si and oxygen on the very surface of the device Si before it leaves the Si surface to the Ar gas.

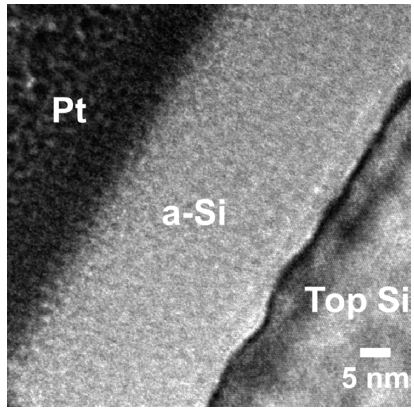


Figure 14 HRXTEM image of Si-4, the surface of the device Si after Ox-away

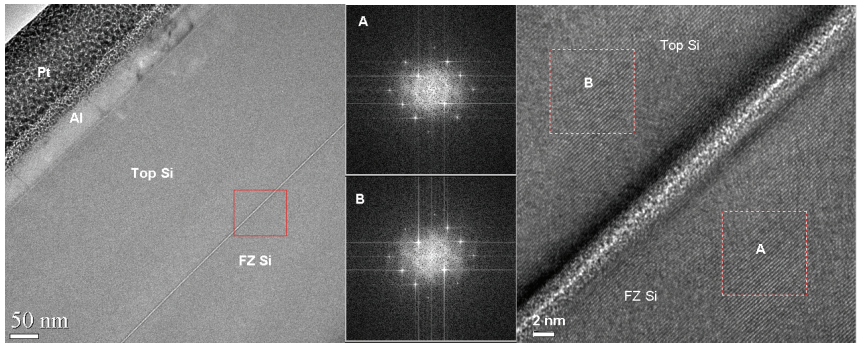


Figure 15 TEM images of Si-0 from table 2. To the left: the bonding stacks, the red square marks the region from where the magnified bond interface comes from and to the right: the bond interface. A and B marks the regions where the Fourier transform calculated

For Si-0 sample, as shown in Figure 15, the intermediate oxide layer is continuous and uniform. It is clear that in the middle of the oxide layer, the bright part is amorphous, while the vicinity starts to crystallize. The diffraction pattern in the top Si layer and the FZ Si layer show the same crystalline orientation. This indicates a good alignment when bonding the top Si (1 0 0) to the FZ Si (1 0 0) wafer. Also the diffraction patterns show that both top device Si and the FZ Si have good crystalline quality.

For Si-1 shown in Figure 16 annealed at 1100 °C for 203 min, the intermediate oxide after Ox-away becomes discontinuous. The remaining oxide thickness is 2 nm, which is thinner than the oxide thickness of the Si-0 reference. Comparing with the result from Ahn et al. for thin oxide sandwiched between two bulk Si wafers [37], dis-integration occurs, however, no thickening was observed.

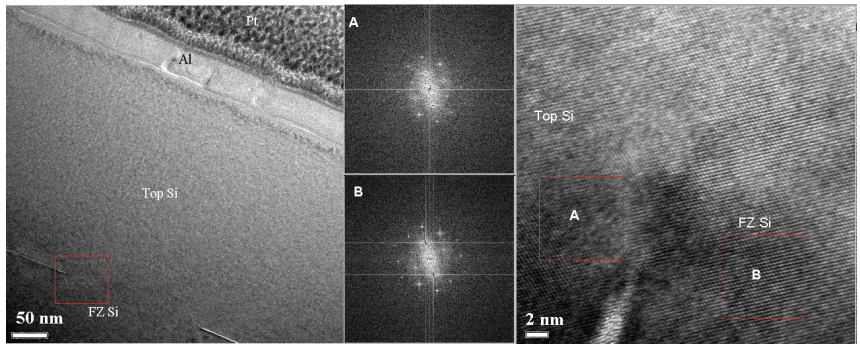


Figure 16 Cross section TEM images of Si-1 annealed at 1100 °C for 203 min. To the left: overview of the bonding stack. To the right: the bonding interface

Si-2 to Si-5 is annealed at 1150 °C with increasing annealing time. The intermediate oxide layer is continuous and uniform for Si-2. It becomes discontinuous for Si-3 and Si-4, similar to Si-1 in Figure 16. The oxide thicknesses are thinner, as listed in Table 4. For Si-5 and Si-6, the intermediate oxide is removed completely, without any traces of oxide islands and it is hard to identify the bonding interface. The diffraction patterns show a good Si crystalline structure and it is free of defects.

Comparing the experimental results with the oxygen out-diffusion theory results, we can see that at 1100 °C, the experimental results show weaker Ox-away effect than the theory prediction. While at 1150 °C and 1200 °C, the experimental results have stronger Ox-away effect than the theory prediction. Comparing our present study with the earlier similar studies we can see that with thicker SiO_2, the experiments follow the theory well: 20 nm SiO_2 in reference [52] and 5 nm SiO_x in reference [53]. Note that in reference [53] the underneath Si is Czochralski (CZ) type which supplies oxygen during the Ox-away process.

Ahn et al. built a model to explain the dis-integration of the thin interfacial SiO_2 sandwiched by two bulk Si wafers in terms of surface energy [37]. It costs energy for the SiO_2 to disintegrate and afterwards it gains energy to spherise: about 3.5 eV is needed for 2 nm SiO_2 to spherise and 8 eV is needed for 3 nm SiO_2 to spherise, which is an unlikely process.

Considering the dis-integration of the 2.4 nm SiO_2 observed under TEM, it agrees with the local out-diffusion theory proposed by Ahn et al [37]. However, no thickening occurs in our case. This is because in our case, oxygen diffuses through the thin top Si layer at the same time it dis-integrates. From the Arrhenius plot (1/T vs. oxide consumption) for the samples in Table 1, we extract the activation energy of the Ox-away process as $E_a \approx 6.4$ eV. Pure oxygen out-diffusion would lead to activation energy of 4.1 eV as in equation 1. The higher activation energy in this study indicates that the dis-integration costs additional energy, which agrees with Ahn et al.

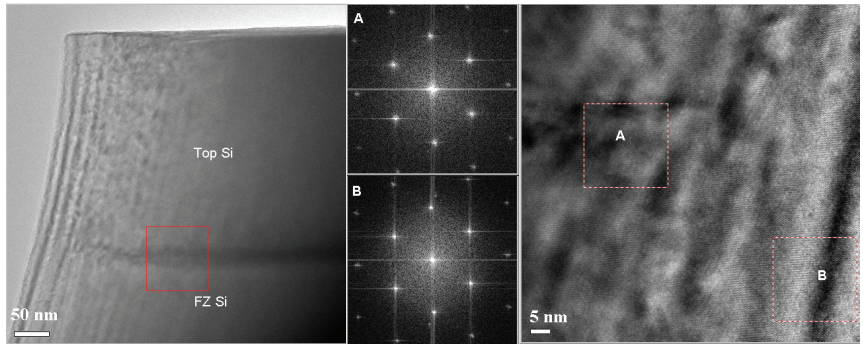


Figure 17 Cross section TEM images of Si-5 annealed at 1150 °C for 120 min. To the left: overview of the bonding stack. To the right: the bonding interface

After Ox-away at 1150 °C for 120 min, shown Figure 17, there is no intermediate oxide interface. The Si crystal meets the SiC crystal directly. No dislocation or stress observed in the Si/SiC interface under the TEM investigation. The EELs results show no detectable oxygen element in the interface region.

The TEM measurement provides a straightforward method to view the remaining oxide thickness. However, for the dis-continuous oxide samples, it lacks information of percentage of the remaining oxide. The modeling from the ellipsometric measurements can provide this information.

A multi-layer model was built to model the top Si and the interface oxide thicknesses: an amorphous Si layer on a crystalline Si layer on a SiO_2 layer mixed with polycrystalline Si layer with either fine grain or large grain on a crystalline Si substrate. The amorphous and the crystalline Si layers are tuned according to the TEM result. The SiO_2 layer thickness and the percentage of the SiO_2 are the fitting numbers. We use the product of the discontinuous oxide thickness and the percentage of the remaining oxide as the ellipsometric measurement of the oxide thickness.

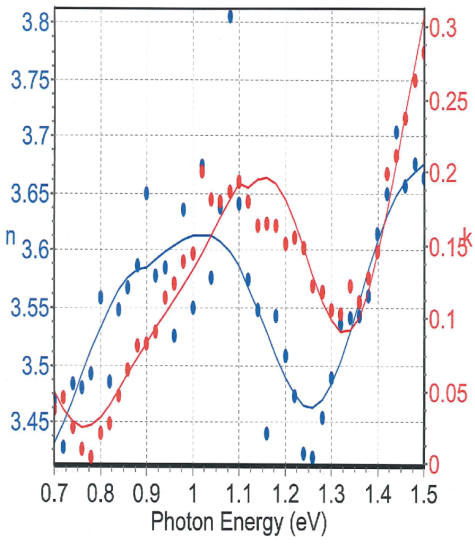


Figure 18 Simulation result of ellipsometry measurement of Si-0. Det dots are ellipsometric measurement result and the solid lines are the simulation results by the multi-layer-model

The thicknesses of the top Si layers and the intermediate oxide layers before and after Ox-away are listed in Table 4. The top Si layer thickness in this study varies from 300 nm to 334 nm is in the range of the batch specification intervals 330 ± 27 nm. We could therefore hardly draw any conclusion of the top Si thickness change due to the Ox-away effect. The remaining oxide thicknesses calculated according to equation 1 uses the ellipsometric measurements of the top Si layer thickness.

The SIMS results of the silicon and oxygen concentration for Si-0 and Si-5 are shown in Figure 19. The Si signals are included to mark the position of the interface. At the interface of Si-0, a maximum oxygen concentration is $1 \cdot 10^{22}$ cm^{-3}, and it agrees well with the oxygen level from the hydrophilic bonded interface [54]. After Ox-away at 1150 °C for 120 min, the maximum oxygen concentration is $5 \cdot 10^{20}$ cm^{-3}. It is comparable to the oxygen level from the hydrophobic bonded interface [54], representing approximately one monolayer of oxygen. The oxygen concentration is about a factor of 20 lower than that of the as-bonded pair.

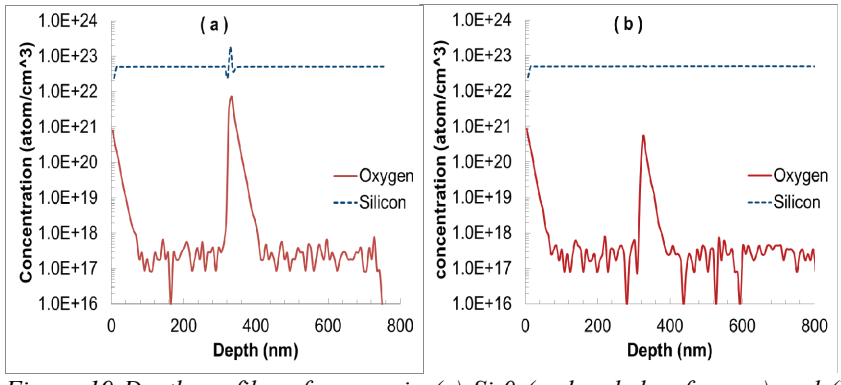


Figure 19 Depth profiles of oxygen in (a) Si-0 (as bonded, reference) and (b) Si-5 (Ox-away at 1150 °C for 120 min) by SIMS analysis. The bonding interfaces are located at ~320 nm.

Sample No.	Annealing Temperature (°C)	Annealing Time (min)	Top Si Layer Thickness (nm) TEM/Ellipsometer	Remaining Oxide Thickness (nm) TEM*/Ellipsometer/Calculated by Equation 1
Si-0	-	-	313/320	2.3−2.6/2.4/2.4
Si-1	1100	203	323/316	2/1.8/1.38
Si-2	1150	30	327/314	1−1.4/1.7/1.89
Si-3		60	323/334	1.2/0.9/1.44
Si-4		90	307/307	0.9/0.6/0.83
Si-5		120	300/318	0/0.1/0.38
Si-6	1200	20	309/-	0/0/1.32

* Repeated results. No deviation within the resolution limit of 0.1 nm.

Table 4, results of Ox-away for Si-SiO_2-Si

To sum up the removal of SiO_2 through top Si by annealing at 1150 °C in Ar, three steps can be distinguished as illustrated Figure 20: a) the bulk diffusion phase is when the oxide is thick that only oxygen out-diffusion through top Si crystals occurs; b) the void formation phase starts when the oxide is under 2.4 nm and it separates and becomes dis-continuous, and the "voids" are Si. In this phase the activation energy is higher than the former phase; c) dis-integration phase will earn energy comparing with the former two phases and in this phase the oxide diffuses out faster than expected by

equation (1). Note that since the measuring points are not enough dense, the boundaries in time are estimated in the illustration figure.

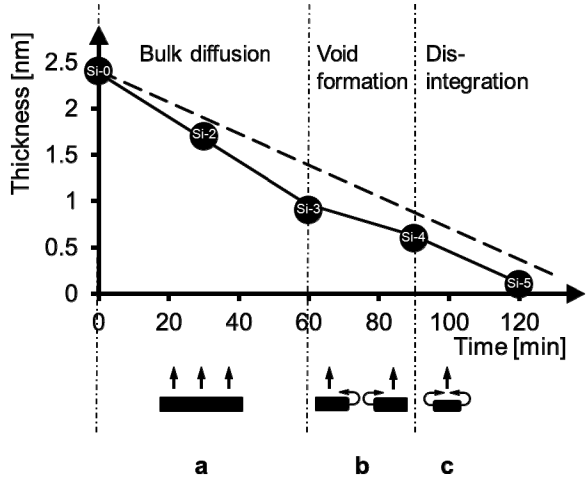


Figure 20 Schematic diagrams of three steps of oxygen out-diffusion at 1150 °C: a bulk diffusion, b void formation and c dis-integration. The dash line is drawn from equation (1)

4.2 Si-SiC bond

The as-received SiC has a flat surface. It has an rms value of 0.34 nm. There are micro-hole defects on the SiC surfaces, as marked in circles in the AFM image in Figure 21 (a). SiC has hydrophobic face. Fortunately, SiC has hydrophilic SiO_2 as its native oxide. We thermally oxidize SiC with a very thin layer of SiO_2 prior to bond it to Si in order to enable the hydrophilic wafer bonding. After oxidation, the rms is reduced to 0.19 nm and the micro-hole voids are filled too, see Figure 21 (b). Note that the differences of the roughness bar in (a) and (b) in Figure 21.

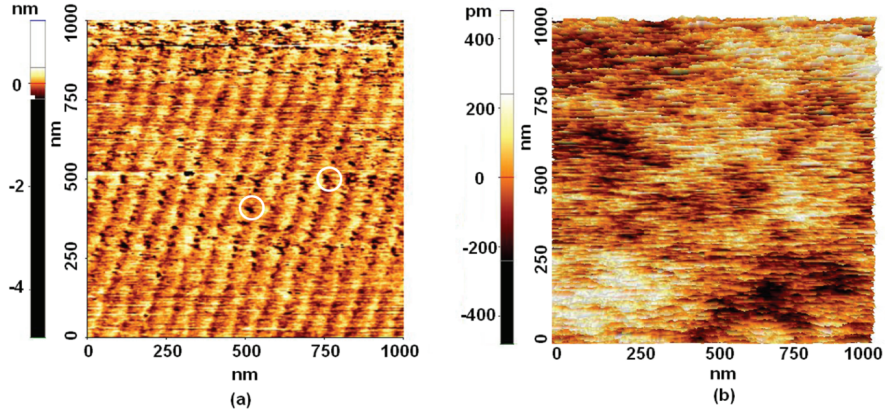


Figure 21 AFM micrograph of (a) as-received SiC and (b) SiC with thermal SiO_2

Figure 22 shows for the Si-SiC bond, the dark area is the bonded area and the light parts are the non-bonded area. Even with 19.3 nm SiO_2 in between, there is still a big non-bonded area.

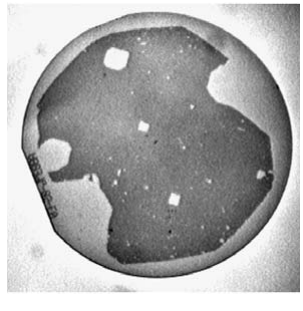


Figure 22 Infrared image of Si-SiC bond (Si-SiO_2-SiC with SiO_2 19.3 nm in Table 1) after bond anneal

Looking closer in this non-bonded area under microscope, shown in Figure 23, we can see that the as bonded Si-SiO_2-SiC pair has voids in the dimension of tens of micrometers times a hundred micrometers. They are bubble collections. During the bond anneal at 1000 °C, the bubbles evaporate

and try to escape. However, it is impossible to diffuse away during the bond anneal, since the bonding energy increases quickly. It ends up with breaking the device Si layer.

During the bond anneal, the bubble gas oxidize the neighbor device Si. Comparing the SiO_2 thickness under TEM in the void free area and the edge of the void, shown in Figure 24, we can see that the SiO_2 grows ~5 nm thicker with the wet oxidization of the Si under bond anneal. It can be seen that the top few nanometer of the SiO_2 is not homogeneous comparing with the underneath part. It is because the re-growth oxide is not as dense as the thermal oxide, and since the bubble vapor tries to "escape" there remains a "struggling hint", as shown in the optical microscopy image in Figure 23 (b).

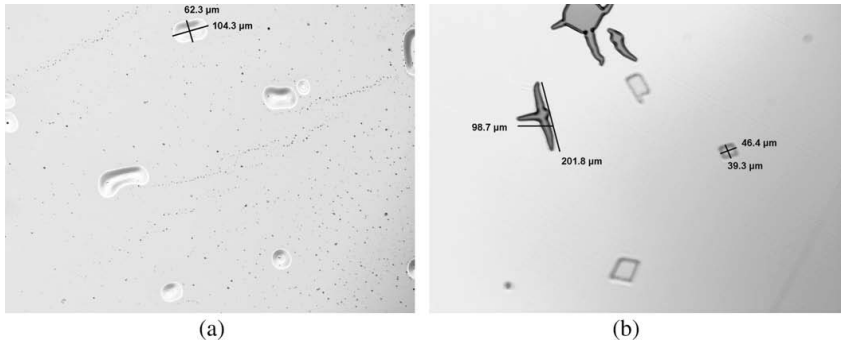


Figure 23 Optical microscopy images of Si-SiO_2-SiC bond (SiC-3 in table 2) (a) as bonded at room temperature and (b) after bond anneal

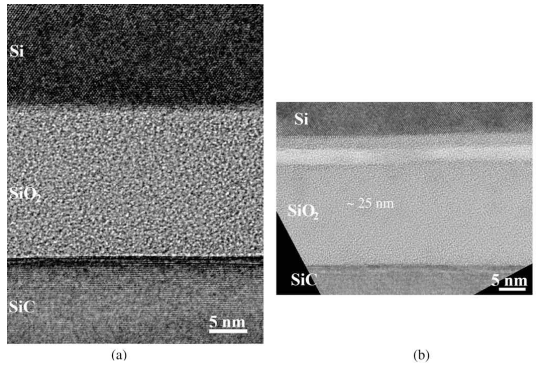


Figure 24 TEM images of Si-SiO_2-SiC (SiC-3 in table 2) after bond anneal (a) the void free area and (b) vicinity of the void

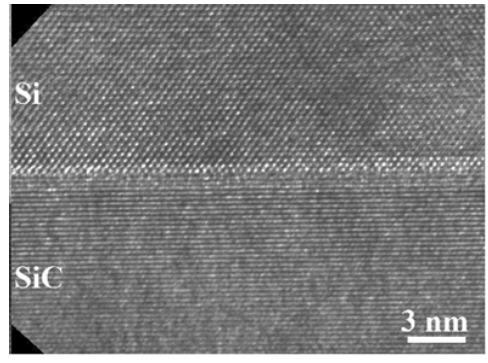


Figure 25 HRXTEM image of Si-SiC interface after Ox-away

The HRXTEM image of Si-SiC bond after Ox-away at 1250 °C for 2.5 h is shown in Figure 25. It can be seen that the Si atoms contact directly with SiC atoms without remaining oxygen atoms. It is structurally sharp and defect free in the atomic level. The Ox-away experiments are repeatable for Si-7 nm SiO_2-SiC (SiC-1 in Table 3) and it is verified by both TEM and EELs (please refer to attached paper IV).

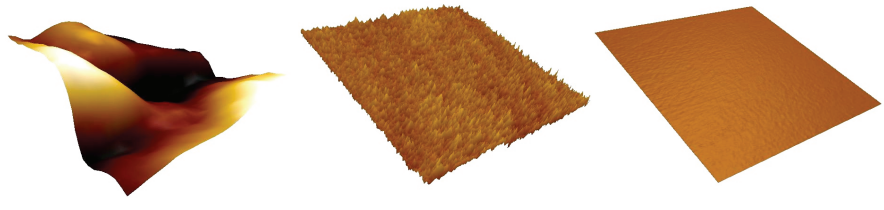
The dynamics of Ox-away with Si-SiC bond goes faster than calculated by equation 1. This is similar to the Si-SiC bond at higher temperatures (1150 °C and 1200 °C). However, there lacks more detail samples for the Si-SiC bond. Therefore we cannot draw conclusion how fast it is for the Si-SiC case.

4.3 Si-pSiC bond

As described in the introduction part, the pSiC wafer is both much cheaper than the SiC wafer and available in larger sizes, which makes it a good alternative to replace the SiC wafer. However, the surface roughness of pSiC is far above the critical bondable condition. Therefore we deposited a layer of amorphous Si (αSi) on it prior to bonding, which we have explained in the experimental part.

The as-purchased pSiC has a root-mean-square roughness (rms) of 180 nm. After chemical vapor deposition (CVP) we can improve the rms to 10 nm. The local rms can be improved to 0.17 nm by chemical mechanical polishing (CMP). It is under the critical roughness for bonding. The CMP even planarize the amorphous Si globally, which is one of the three pre-requisites for wafer bonding. The rms values here are from noncontact mode by measuring the area of 1 um x 1 um samples. The AFM results are shown in Figure 26 with an isotropic scale to show the obvious difference in roughness.

Figure 27 (a) shows photograph of bonded 6 inch Si-αSi-pSiC wafer. No voids in the bond area under the optical microscopy, or under the IR image. This has been verified by the defect etch [55]. The bare edge circle is due to the size difference between the pSiC wafer and the device Si layer from the as-received SOI wafer, which is transferred to the pSiC. We then fabricated components on these substrates, as shown in Figure 27 (b) and characterized both electrical and thermal properties of these components.



(a) *(b)* *(c)*

Figure 26 AFM measurement of (a) as-purchased pSiC, (b) CVP of αSi on pSiC and (c) CMP treatment of αSi. The images depicts 1x1μm with an isotropic scale

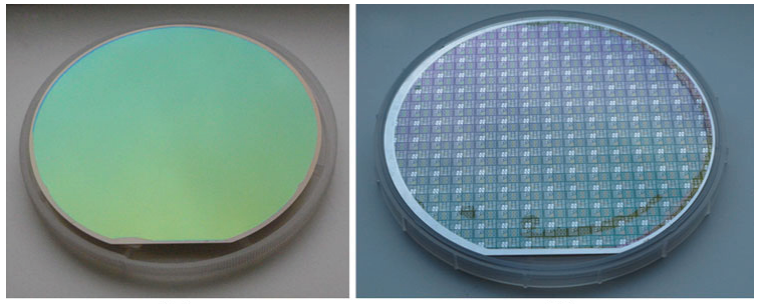


Figure 27 Photograph of (a) 6 inch bonded Si-αSi-pSiC substrate and (b) a fully processed wafer based on the hybrid Si-αSi-pSiC substrate

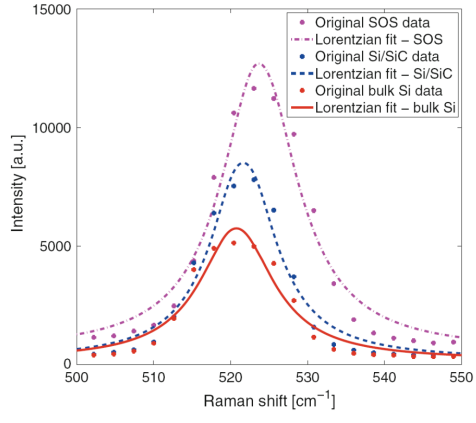


Figure 28 Raman spectroscopy of Si-on-sapphire (SOS), Si-pSiC and bulk Si. The SOS curve presents a reference of compressive stress induced Raman shift

The bonding interface stress is analyzed by Raman spectroscopy and XRD. Figure 28 shows that comparing with the bulk Si wafer, there is no Raman shift for the Si-αSi-pSiC. A SOS wafer with known compressive stress was used as the reference wafer [56]. This means the stress on the device Si layer is under the detection of Raman spectroscopy. It can be seen in the XRD measurement that, shown in Figure 29, the peak locates at around 69.13 ˚ as the (4 0 0) planes of Si (1 0 0) has no peak shift due to stress. Hereby we conclude that we have achieved stress-free hybrid Si-αSi-pSiC bond in 6 inch dimension.

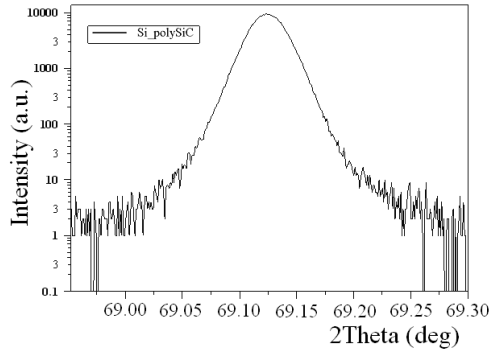


Figure 29 XRD measurement of Si-αSi-pSiC

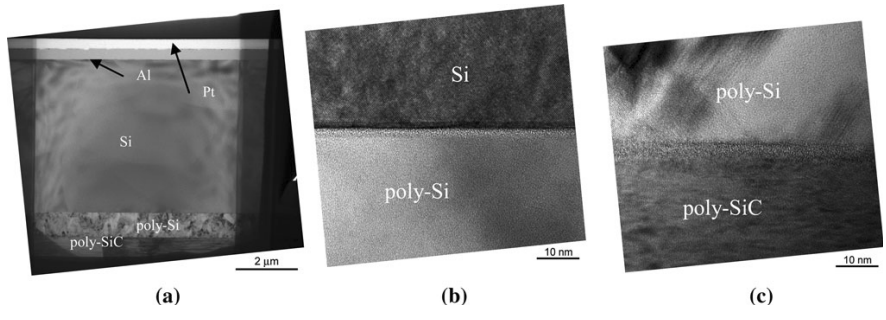


Figure 30 TEM images of (a) the overview of the Si-αSi-pSiC substrate, (b) the bond interface between Si and αSi and (c) the interface between recrystallized αSi and pSiC

The TEM images of the bond pairs including HRXTEM image of Si-αSi-pSiC are shown in Figure 30. Image (b) shows that there is a ~2nm amorphous layer in the Si-pSi interface. It is SiO_2 and it is from the hydrophilic wafer bonding and bond anneal, similar to the Si-Si bond. In the interface of αSi-pSiC, a thin oxide layer appeared too, in the dimension of 5 nm. This could mean that the pSiC was oxidized unintentionally prior to the αSi deposition.

Note that when deposited on the pSiC, the Si is amorphous and the resulting bond pair has polycrystalline Si (poly-Si in the TEM image) instead. That is because during the bond anneal at 1000 °C, the amorphous Si recrystallize in some extent to polycrystalline Si. αSi was chosen be deposited on pSiC since it is much easier for chemical mechanical polishing. After its recrystallization, the polycrystalline Si has better thermal conductivity than the αSi.

4.4 Electrical measurements of Si-pSiC hybrid substrate

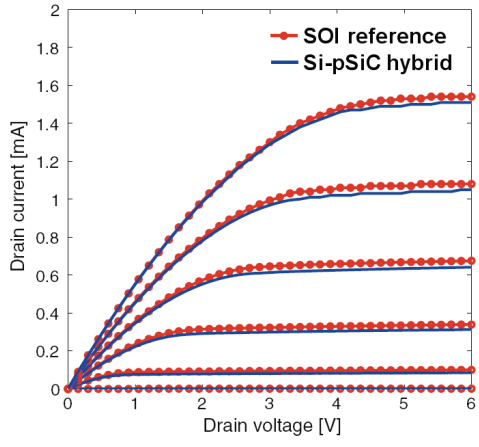


Figure 31 MOSFET output characteristics for the SOI reference and the Si-pSiC hybrid substrate

The I-V measurements, Figure 31, based on the diodes and MOSFET structures show that comparing with its SOI counterpart, the Si-pSiC hybrid substrate has no degradation in electrical behavior, so as the C-V measurement (not shown here, please refer to attached paper III). The thermal characterization based on the finger structured thermistors show that the Si-pSiC hybrid substrate has 2.5 times lower thermal resistance than the SOI substrate (attached paper III). This is slightly less than what was expected due to the intrinsically good thermal conductivity of pSiC. It can be explained by the interfacial layer as discussed in 4.5 and in the discussion of introduction part (in attached paper I) from literature study.

It was also found that both SOI and Si-pSiC hybrid substrate have same behavior in carrier life time, as measured by junction leakage. Furthermore, gate oxide integrity seems to be even slightly better on the hybrid substrate (refer to attached paper III).

4.5 Thermistor

The calibration curves of four point probe for Si, pSiC and SiC wafers are of good linearity (please refer to attached paper V).

The temperature − power density curves for all of the three wafers are shown in Figure 32. At the same power density, TiN thermistor on Si wafer increases more temperature than that of on SiC wafer. This is caused by the worse thermal conductivity of Si wafer. The temperature coefficient of the power density, i.e. the slope of the temperature − power density curve, indicates the temperature increases with the power density. This value of TiN on Si wafer is three times of TiN on SiC wafer. This agrees with the difference of the thermal conductivity between Si wafer and SiC wafer.

At same power density, take 30000 W/cm^2 as an example, T_{Si} = 73 °C; T_{pSiC} =52 °C and T_{SiC} = 43 °C.

ΔT/ Δ(P/A) ratio for Si/pSiC = 0.0015/0.0009 = 1.6 and Si/SiC = 2.5. This is comparable to the ratio of thermal conductivity Si/SiC = 4.9/1.5 = 3.2.

Electro-thermal simulation was carried out to extract the thermal conductivity of Si, pSiC and SiC using a 2D device simulator Dessis from Synopsys. Details can be referred to the attached paper V. Thermal conductivity for these three materials can be extracted comparing the experimental results and the simulation. κ_{Si} = 1.5 WK^{-1}cm^{-1}, which is in good agreement as widely reported in literatures. κ_{SiC} = 3.5 WK^{-1}cm^{-1}, which is slightly lower than the reported value of 4.9 WK^{-1}cm^{-1}.

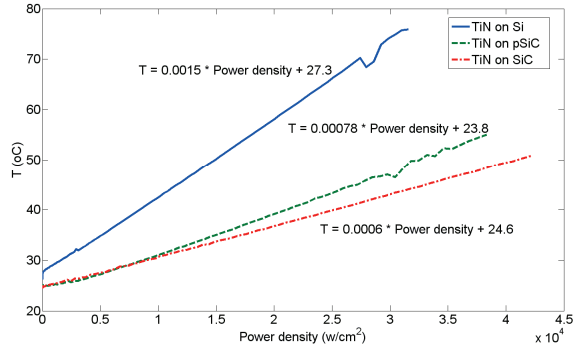


Figure 32 Temperature dependence of power density for TiN on Si, pSiC and SiC

κ_{pSiC} depends on many factors, for instance the poly-types, grain sizes etc. In this work and our former multi-layer Si-αSi-pSiC hybrid substrates we can extract the $\kappa_{pSiC} = 2.7$ $WK^{-1}cm^{-1}$. It is smaller than the thermal conductivity of the crystalline SiC, however, much higher than that of the SiO_2.

Comparing the electro-thermal simulation done by Si-αSi-pSiC and SOI substrates (attached paper IV) we can extract the thermal conductivity of oxide and αSi as $\kappa_{SiO2} = 0.018$ $WK^{-1}cm^{-1}$, which is close to the well accepted value of 0.014 $WK^{-1}cm^{-1}$ and $\kappa_{\alpha Si} = 0.12$ $WK^{-1}cm^{-1}$. Therefore to get a better thermal dissipation, it is important to keep the interfacial oxide layer as thin as possible in the Si-SiC hybrid substrate.

Summary and Outlook

We have achieved Si-SiC hybrid substrates through hydrophilic wafer bonding for the first time. It is measured that there is very little strain in the bonding interface. Ox-away results in oxide-free Si-SiC structurally sharp bond interface. The quality of the device Si is as high as it was before bonded. A thin layer of amorphous Si appeared during the Ox-away process. The formation of it has been discussed. It can be polished prior to further component fabrication. Voids originates from the hydrophilic surface treatment prior to room temperature bond is still an issue after bond anneal. A few methods can be applied to try to get rid of it: 1) through oxidizing the SiC a thicker layer prior to hydrophilic wafer bonding; 2) long time lower temperature bond anneal to leave the water vapor to oxidize the Si layer or "escape" through the low energy bond interface [57]; 3) vacuum treatment prior to wafer bonding.

The Ox-away dynamics has been studied based on the Si-Si bonded substrates. It is found that both oxygen out-diffusion and spheroidization are behind the behavior for the thin interfacial oxide removal (<2.4 nm). The activation energy is estimated to be 6.4 eV. At higher temperatures (1150 °C, 1200 °C and 1250 °C) the Ox-away is faster than the prediction by equation 1. New equations extracted through denser experimental samples would be helpful to describe the temperature/time dependence of the Ox-away. And it would be useful for the economical way to achieve oxide-free wafer bonding.

Components based on the Si-pSiC hybrid substrates has been fabricated and characterized. The electrical properties of the components in the Si-pSiC hybrid substrates are as good as or better than those based on the SOI reference. But the thermal dissipation of the Si-pSiC based components show a factor of 2.5 times better than their SOI based counterparts. It would be interesting to include the oxide-free Si-SiC substrates based components, especially the RF behaviors.

TiN thermistors have been fabricated and measured to compare the thermal dissipation property for Si, pSiC and SiC substrates. It shows similar relationship of the thermal properties as the literature. The 2D electro-thermal simulation together with the experimental results has extracted the thermal conductivity for Si, SiC and pSiC materials. Combining the 2D simulation for the Si-pSi-pSiC hybrid substrate and SOI substrate, we have also extracted the thermal conductivity for SiO_2 and αSi. It proves our assump-

tion: the importance to keep the oxide layer as thin as possible in the Si-SiC hybrid substrates for a better thermal dissipation.

Sammanfattning på svenska

Den speciella typ av kiselskivor som den här avhandlingen behandlar, *silicon on insulator* (SOI) (svenska: kisel på isolator) återfinns till exempel i hemelektronik så som XBOX och PlayStation. SOI-skivorna medger högre frekvens, lägre strömförbrukning och allmänt bättre prestanda för de integrerade kretsarna jämfört med vanliga kiselskivor. Den här typen av skivor gör det också möjligt att packa kretsarna tätare. De vanligaste SOI-skivorna är uppbyggda av ett tunt kiselskikt, där elektroniken tillverkas, ovanpå ett tunt kiseldioxidskikt som isolerar elektriskt från en tjockare bärarskiva. Bärarskivan behövs för att ge stadga. Tyvärr har kiseldioxid dålig värmeledningsförmåga vilket leder till att de elektroniska komponenterna inte kan användas vid hög effekt utan att prestanda blir lidande.

Vi har bytt ut det isolerande kiseldioxidskiktet och bärarskivan mot semiisolerande kiselkarbid och därmed blivit först med att tillverka Si–SiC-hybridsubstrat. Materialen har sammanfogats med så kallad *wafer bonding*. Vi har vidare utvecklat en metod för att använda polykristallin kiselkarbid, pSiC, som ersättning för den betydligt kostsammare en-kristallina varianten. Genom att deponera och polera amorft kisel på pSiC har *wafer bonding* kunnat användas.

Med en efterföljande värmebehandling som vi kallar *Ox-away* har kvarvarande kiseldioxid i gränsytan mellan kisel och kiselkarbid kunnat avlägsnas. Dynamiken hos förloppet vid *Ox-away* har studerats med *wafer bonding* av kiselsubstrat till kiselsubstrat. Vi har funnit att två mekanismer samverkar vid avlägsnandet av det tunna kiseldioxidskiktet: diffusion av syreprecipitat och sfärbildning. Aktiveringsenergin uppskattas till 6,4 eV.

Elektroniska komponenter har tillverkats och karakteriserats på Si–pSiC-hybridsubstraten. De elektriska egenskaperna hos komponenterna har funnits lika bra som de som baseras på SOI referenser. Dessutom var värmeavledning på hybridsubstraten är 2,5 gånger bättre än på de konventionella SOI-skivorna.

Värmeledningsegenskaperna hos kisel och kristallin- och polykristallin kiselkarbid har undersökts genom att termistorer av TiN har tillverkats och karakteriserats på substraten. De erhållna resultaten är i paritet med tidigare publicerade arbeten. Genom att anpassa tvådimensionella elektrotermiska simuleringar med de experimentella resultaten har värmeledningsförmågan för Si, SiC och polykristallin SiC bestämts. I jämförelse med tidigare mätningar på hybridsubstrat såväl som på SOI-substrat har också den termiska

ledningsförmågan för kiseldioxid och amorft kisel bestämts. Det står klart att det är viktigt att hålla oxidskiktet så tunt som möjligt i Si–SiC-hybridsubstraten för en optimal värmeavledning.

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